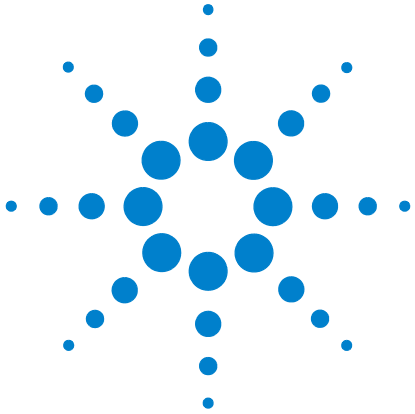

Agilent N5393C PCI Express Automated Test Application

Compliance Testing Methods of Implementation

Agilent Technologies

Notices

Manual Part Number

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PCI Express Automated Testing—At A Glance

The Agilent N5393C PCI Express Automated Test Application helps you verify PCI Express device under test (DUT) compliance to specifications with the Agilent 90000X Infiniium digital storage oscilloscope. The PCI Express Automated Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE The tests performed by the PCI Express Automated Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

Required Equipment and Software

In order to run the PCI Express automated tests, you need the following equipment and software:

- N5393C PCI Express Automated Test Application software.
- 90000X series Infiniium Digital Storage Oscilloscope
- E2688A Serial Data Analysis and Clock Recovery software.
- Probes and/or test fixtures. For more information on the specific probes and test fixtures required, refer to the chapters that describe tests.
- N5380A Hi-BW differential SMA probe heads.
- Keyboard, qty = 1, (provided with the Agilent 90000X oscilloscope).
- Mouse, qty = 1, (provided with the Agilent 90000X oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, qty = 2 (provided with the Agilent 90000X oscilloscope).
- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG-316/U or similar, qty = 2, matched length.

In This Book

This manual describes the tests that are performed by the PCI Express Automated Test Application in more detail; it contains information from (and refers to) the Base Specification, Card Electromechanical Specification, and ExpressCard Standard, and it describes how the tests are performed.

This manual is divided to several sections:

- Part I, "Introduction" covers the software and license installation and test preparation guide.
- Part II, "PCI Express Version 1.0a" covers the tests and Method of Implementation of PCI Express version 1.0a.
- Part III, "PCI Express Version 1.1" covers the tests and Method of Implementation of PCI Express version 1.1.
- Part IV, "2.5 GT/s PCI Express Version 2.0" covers the tests and Method of Implementation of 2.5 GT/s PCI Express version 2.0.
- Part V, "5.0 GT/s PCI Express Version 2.0" covers the tests and Method of Implementation of 5.0 GT/s PCI Express version 2.0.
- Part VI, "PCI Express Version 3.0" covers the tests and Method of Implementation of ExpressCard version 1.0.
- Part VIII, "Appendices" covers oscilloscope calibration, channel de-skew calibration and probe information.

The chapters in this book are:

- Chapter 1, "Installing the PCI Express Automated Test Application" shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, "Preparing to Take Measurements" shows how to start the PCI Express Automated Test Application and gives a brief overview of how it is used.
- Chapter 3, "Transmitter (Tx) Tests, PCI-E 1.0a, Full Power" contains more information on the PCI Express version 1.0a transmitter tests.
- Chapter 4, "Transmitter (Tx) Tests, PCI-E 1.0a, Low Power" contains more information on the PCI Express version 1.0a transmitter tests.
- Chapter 5, "Receiver (Rx) Tests, PCI-E 1.0a" contains more information on the PCI Express version 1.0a receiver tests.
- Chapter 6, "Add-In Card (Tx) Tests, PCI-E 1.0a" contains more information on the PCI Express version 1.0a add-in card tests.
- Chapter 7, "System Board (Tx) Tests, PCI-E 1.0a" contains more information on the PCI Express version 1.0a system board tests.
- Chapter 8, "Transmitter (Tx) Tests, PCI-E 1.1, Full Power" contains more information on the PCI Express version 1.1 transmitter tests.

- Chapter 9, “Transmitter (Tx) Tests, PCI-E 1.1, Low Power” contains more information on the PCI Express version 1.1 transmitter tests.
- Chapter 10, “Receiver (Rx) Tests, PCI-E 1.1” contains more information on the PCI Express version 1.1 receiver tests.
- Chapter 11, “Add-In Card (Tx) Tests, PCI-E 1.1” contains more information on the PCI Express version 1.1 add-in card tests.
- Chapter 12, “System Board (Tx) Tests, PCI-E 1.1” contains more information on the PCI Express version 1.1 system board tests.
- Chapter 13, “Reference Clock Tests, PCI-E 1.1” contains more information on the PCI Express version 1.1 reference clock tests.
- Chapter 14, “Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 2.0, Full Power” contains more information on the PCI Express version 2.0, 2.5 GT/s transmitter tests.
- Chapter 15, “Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 2.0, Low Power” contains more information on the PCI Express version 2.0, 2.5 GT/s transmitter tests.
- Chapter 16, “Receiver (Rx) Tests, 2.5 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 2.5 GT/s receiver tests.
- Chapter 17, “Add-In Card (Tx) Tests, 2.5 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 2.5 GT/s add-in card tests.
- Chapter 18, “System Board (Tx) Tests, 2.5 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 2.5 GT/s system board tests.
- Chapter 19, “Transmitter (Tx) Tests, 5.0 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 5.0 GT/s transmitter tests.
- Chapter 20, “Receiver (Rx) Tests, 5.0 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 5.0 GT/s receiver tests.
- Chapter 21, “Add-In Card (Tx) Tests, 5.0 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 5.0 GT/s add-in card tests.
- Chapter 22, “System Board (Tx) Tests, 5.0 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 5.0 GT/s system board tests.
- Chapter 23, “Reference Clock Tests, 5.0 GT/s, PCI-E 2.0” contains more information on the PCI Express version 2.0, 5.0 GT/s reference clock tests.
- Chapter 24, “Transmitter (Tx) Tests, PCI-E 3.0” contains more information on the PCI Express version 3.0 transmitter tests.
- Chapter 25, “Add-In Card (Tx) Tests, 8.0 GT/s, PCI-E 3.0” contains more information on the PCI Express version 3.0 add-in card tests.
- Chapter 26, “System Board (Tx) Tests, PCI-E 3.0” contains more information on the PCI Express version 3.0 system board tests.

- Chapter 27, “Reference Clock Tests, PCI-E 3.0” contains more information on the PCI Express version 3.0 reference clock tests.
- Appendix A, “Calibrating the Digital Storage Oscilloscope” describes how to calibrate the oscilloscope in preparation for running the PCI Express automated tests.
- Appendix B, “InfiniiMax Probing Options” describes the probe amplifier and probe head recommendations for PCI Express testing.
- Appendix C, “INF_SMA_Deskew.set Setup File Details” describes a setup used when performing channel de-skew calibration.

See Also The PCI Express Automated Test Application’s online help, which describes:

- Starting the PCI Express Automated Test Application.
- Creating or Opening a Test Project.
- Setting up the Test Environment.
- Selecting Tests.
- Configuring Tests.
- Connecting the Oscilloscope to the DUT.
- Running Tests.
- Viewing Results.
- Viewing/Exporting/Printing the report.
- Saving Test Projects.
- Controlling the Application via a Remote PC.
- Using a Second Monitor

Contents

Part I
Introduction

Agilent Technologies

Part I

1 Installing the PCI Express Automated Test Application

If you purchased the N5393C PCI Express Automated Test Application separately, you need to install the software and license key.

Installing the Software

1 To obtain the PCI Express Automated Test Application, go to Agilent website: http://www.agilent.com/find/N5393C

2 The link for PCI Express Automated Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

Be sure to accept the installation of the .NET Framework software; it is required in order to run the PCI Express Automated Test Application.

Installing the License Key

1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

You will need the oscillocope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog.

2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application software to complete the license installation.

2 Preparing to Take Measurements

Before running the PCI Express automated tests, you should calibrate the oscilloscope. After the oscilloscope has been calibrated, you are ready to start the PCI Express Automated Test Application and perform measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope, see Appendix A, "Calibrating the Digital Storage Oscilloscope".

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration and channel de-skew calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel they were calibrated for.

Starting the PCI Express Automated Test Application

1 From the Infiniium oscilloscope's main menu, choose Analyze>Automated Test Apps>PCI Express.

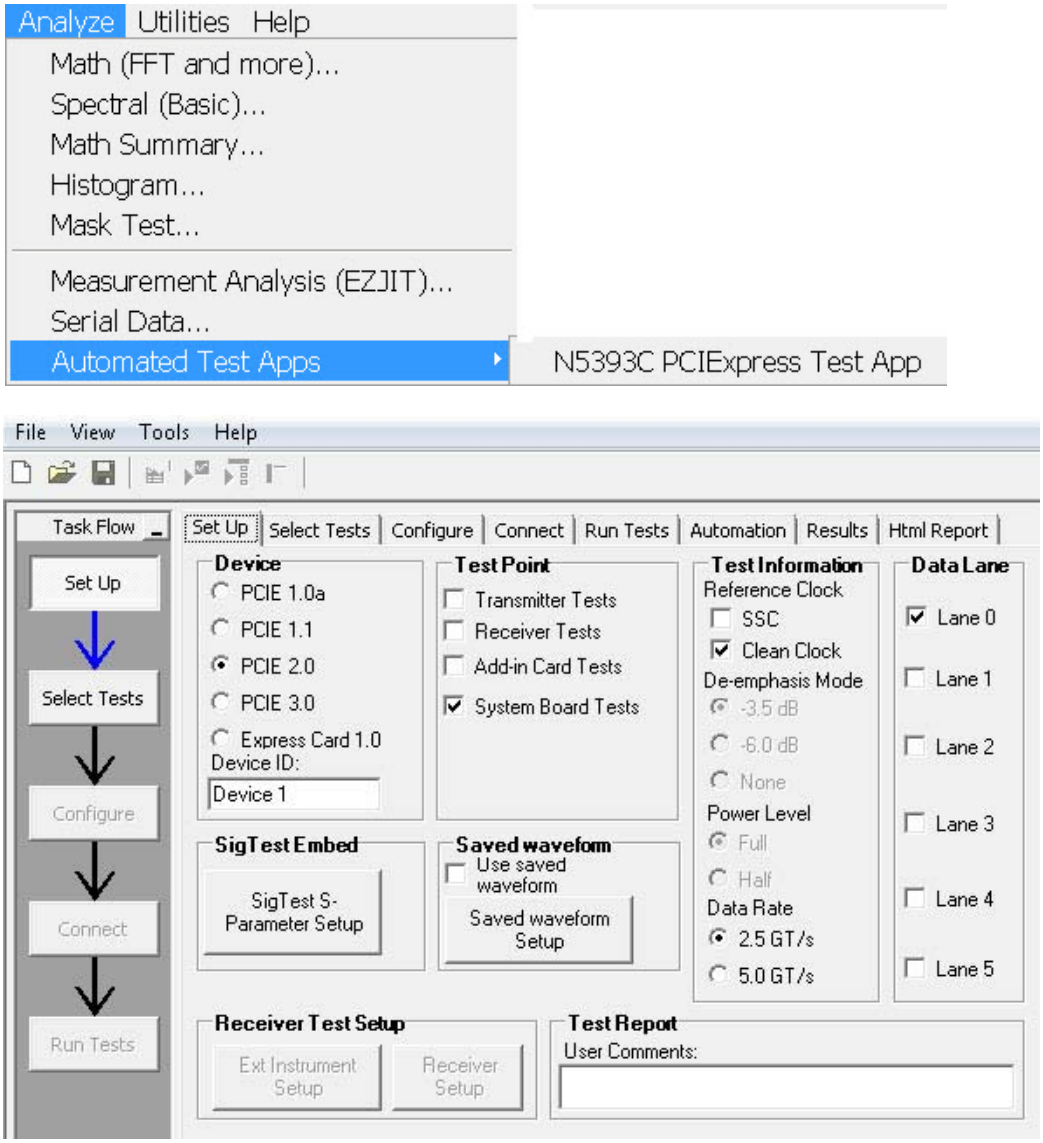

Figure 1 The PCI Express Automated Test Application

NOTE If PCI Express does not appear in the Automated Test Apps menu, the PCI Express Automated Test Application has not been installed (see Chapter 1, "Installing the PCI Express Automated Test Application").

Figure 1 shows the PCI Express Automated Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you identify and set up the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure the test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

Online Help Topics

For information on using the PCI Express Automated Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The PCI Express Automated Test Application's online help describes:

- Starting the PCI Express Automated Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up the test environment.
  - To set up InfiniiSim.
  - To load saved waveforms.

- Selecting tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running tests.
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  - To run multiple times.
  - To send email on pauses or stops.
  - To specify the event.
  - To set the display preferences.
  - To set the run preferences.
- Viewing test results.
  - To delete trials from the results.
  - To show reference images and flash mask hits.
  - To change margin thresholds.
  - To change the test display order.
  - To set trial display preferences.
- Viewing/exporting/printing the HTML test report.
  - To export the report.
  - To print the report.
- Saving test projects.
  - To set AutoRecovery preferences.
- Controlling the application via a remote PC.
  - To check for the App Remote license.
  - To identify the remote interface version.
  - To enable the remote interface.
  - To enable remote interface hints.
- Using a second monitor.

Clock Recovery and Analysis (Applicable to PCI Express 1.0a Only)

As described in Section 4.3.3.1 of the Base Specification, the following methodology is used to define the data set for all PCI Express eye and jitter measurements.

- The clock recovery window is 3500 consecutive Unit Intervals and the Mean of the UIs is used as the reference clock. The first 3500 UIs in the acquisition are used.
- An analysis window is established to be 250 bits centered in the 3500 UI clock recovery window. The mask is placed based on the median of the 250 bit analysis window.
- If there are enough data points in the record, the clock recovery window is advanced by 100 UI, a new mean UI is computed, and analysis is repeated over the middle 250 UI. This process is repeated until the advancing clock recovery window passes the end of the data record.

Part II
PCI Express Version 1.0a

Agilent Technologies

Part II

3 Transmitter (T_x) Tests, PCI-E 1.0a, Full Power

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for T_x Compliance

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the Ch2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern as defined in section 4.2.8 of the PCI Express Base Specification, Rev 2.0 will be transmitted.

Table 1 Probing Options for Transmitter Testing

	Probing Configurations			Captured Waveforms	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes
	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No

Single-Ended SMA Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

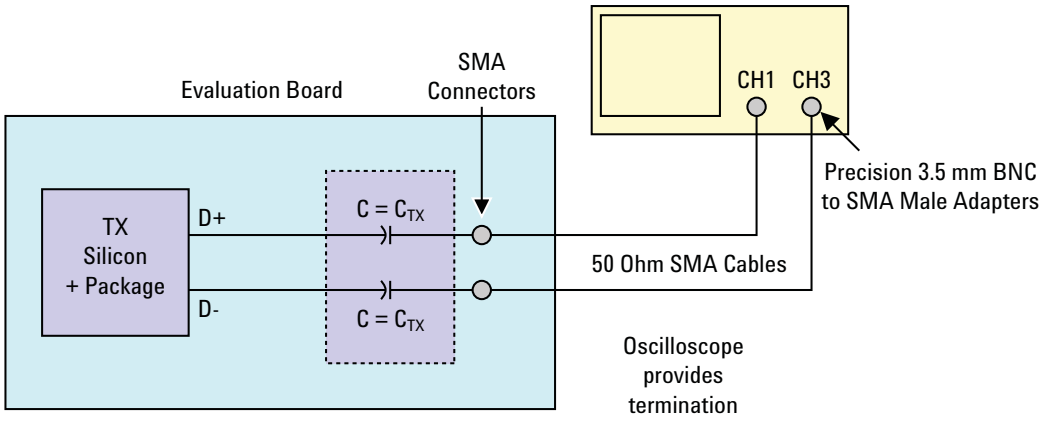


Figure 2 Single-Ended SMA Probing

Single-Ended Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

Place single-ended grounds as close to the signal line’s reference ground as possible.

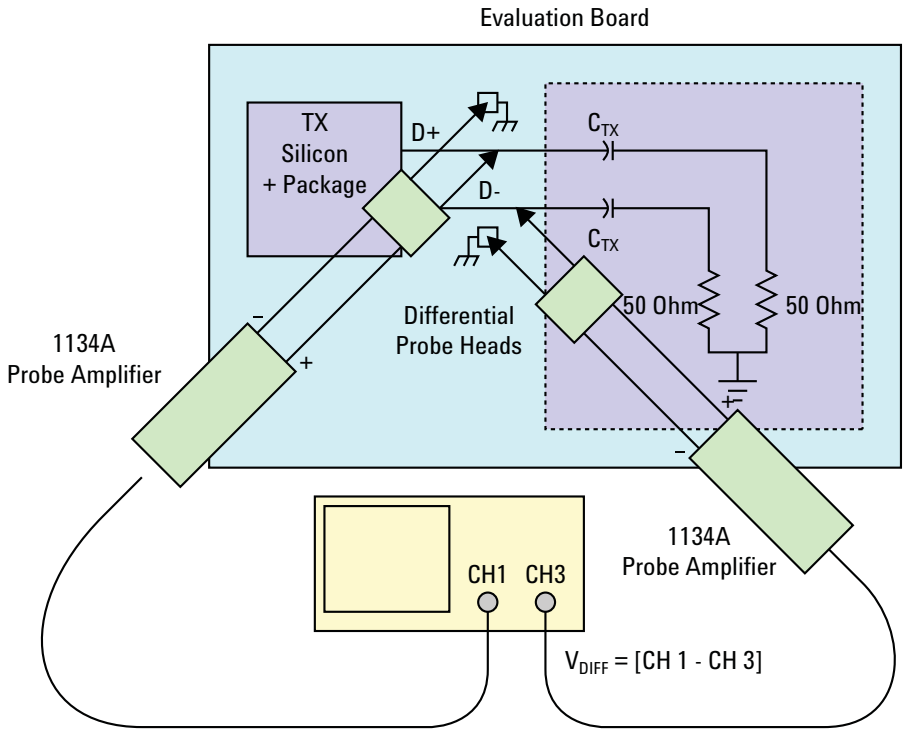


Figure 3 Single-Ended Probing

Differential Probing (Ch2)

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

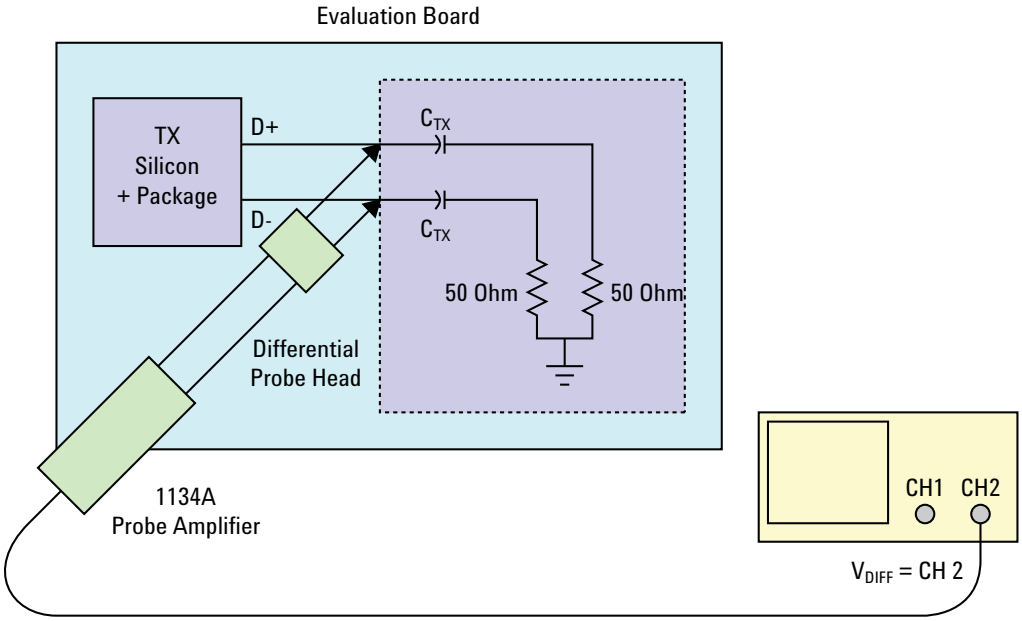


Figure 4 Differential Probing

T_x Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification)

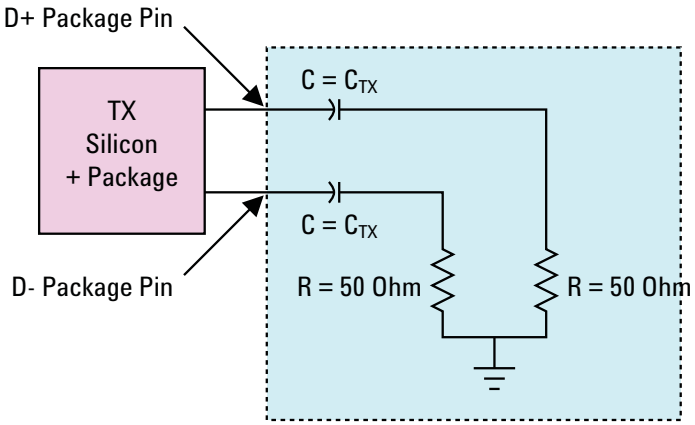


Figure 5 Driver Compliance Test Load.

Running Signal Quality Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to "Signal Quality" in the "Transmitter (T_x) Tests" group.

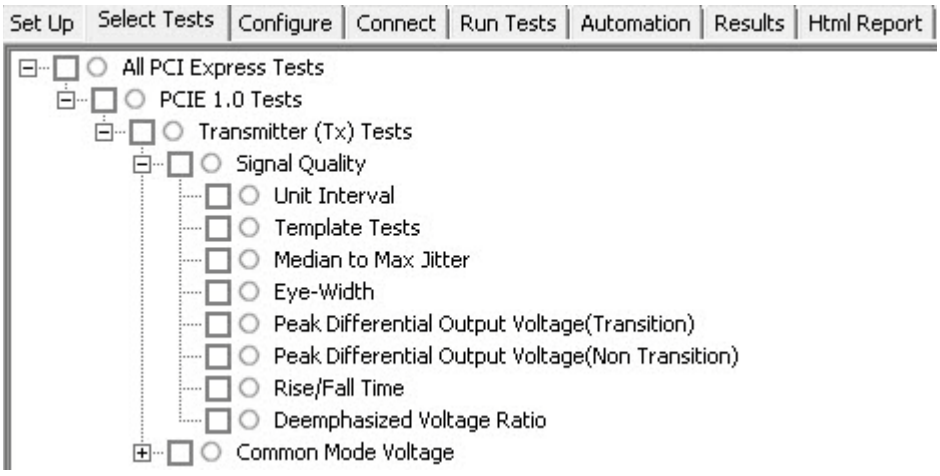


Figure 6 Selecting Transmitter (T_x) Signal Quality Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 2 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Signal Quality Tests" on page 38 and select **Unit Interval**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.

4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `399.88ps < UI < 400.12ps`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

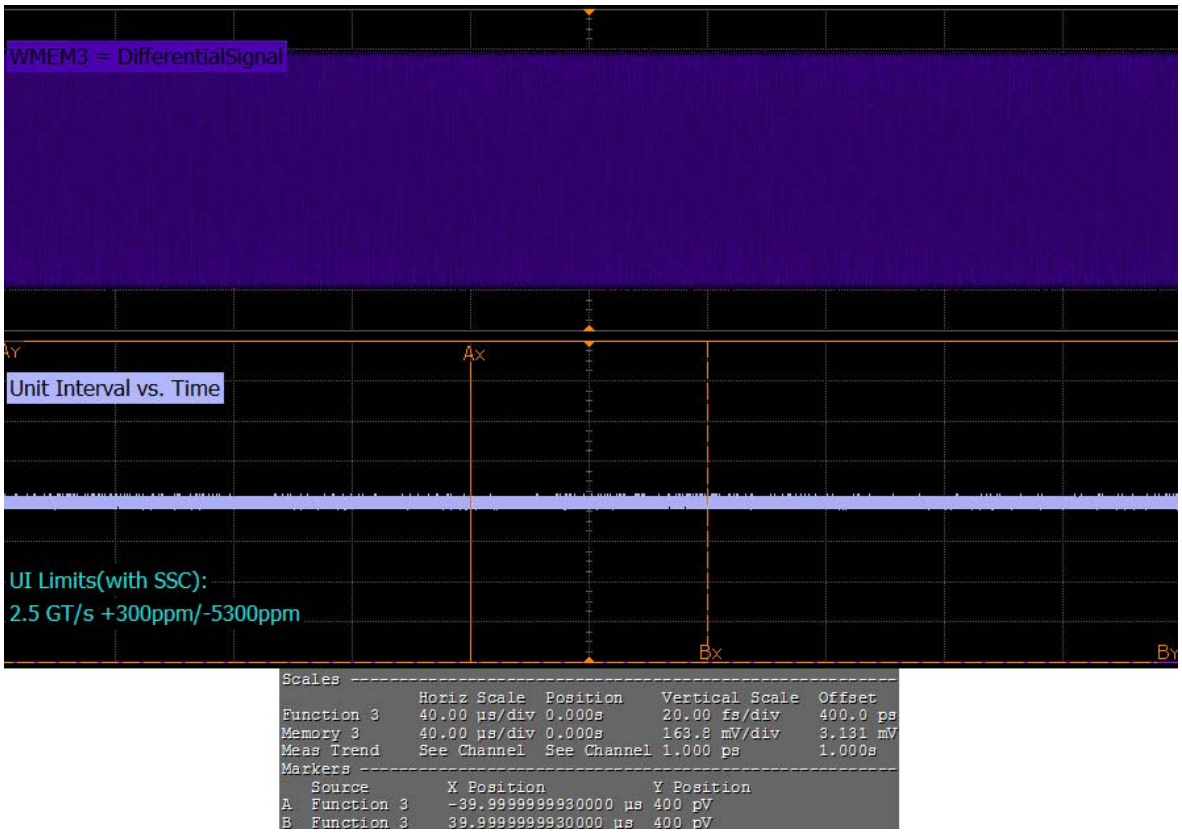


Figure 7 Reference Image for Unit Interval Test

Template Test

All PCIE devices must meet the transmitter eye diagram as specified in the PCI Express Base Specification, Rev 2.0.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 3 Template Test Details

Symbol	Parameter	Min	Max	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p T_x voltage swing	0.8V	1.2V	The differential p-p T_x voltage swing parameter is defined as $2^* \mid V_{TXD+} - V_{TXD-} \mid$ as measured with the compliance test load.

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level.
- As measured with compliance test load. Template test is defined as

$$\text{Template test} = 2^* \left| V_{TXD+} - V_{TXD-} \right|.$$

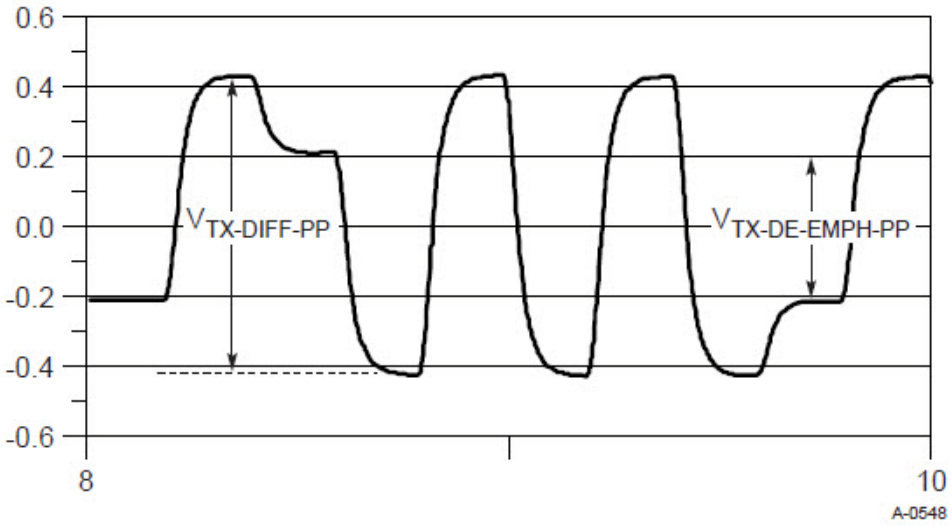


Figure 8 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Signal Quality Tests" on page 38 and select **Template Tests**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the transmitter compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the mean differential p-p T_x voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $0.8V < V_{TX-DIFF-PP} < 1.2V$ and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help

.

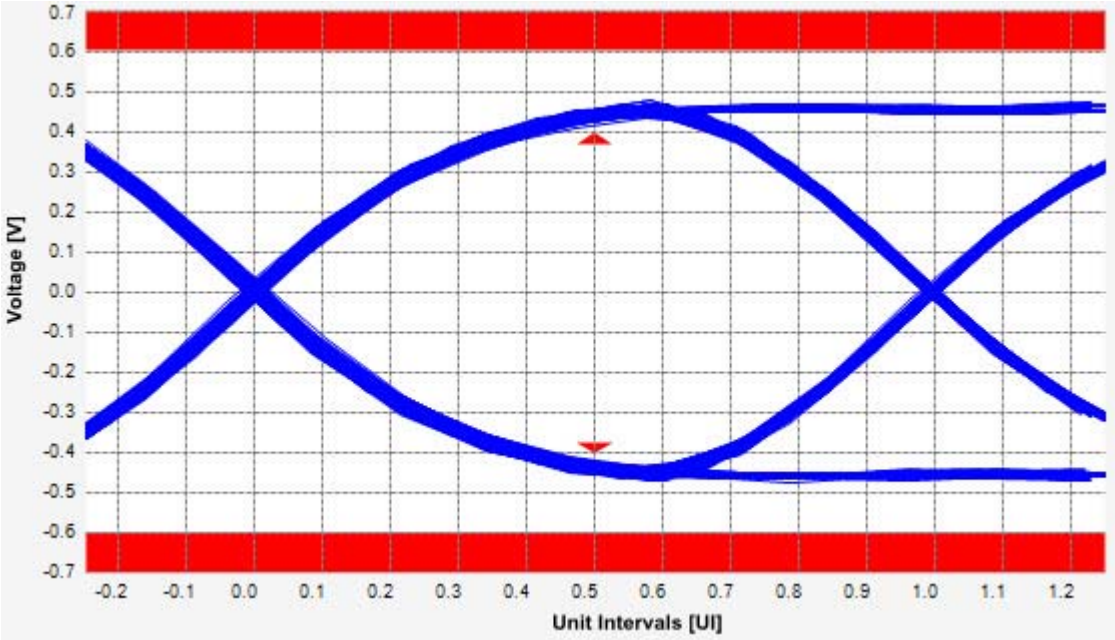


Figure 9 Reference Image for Template (Transition) Test

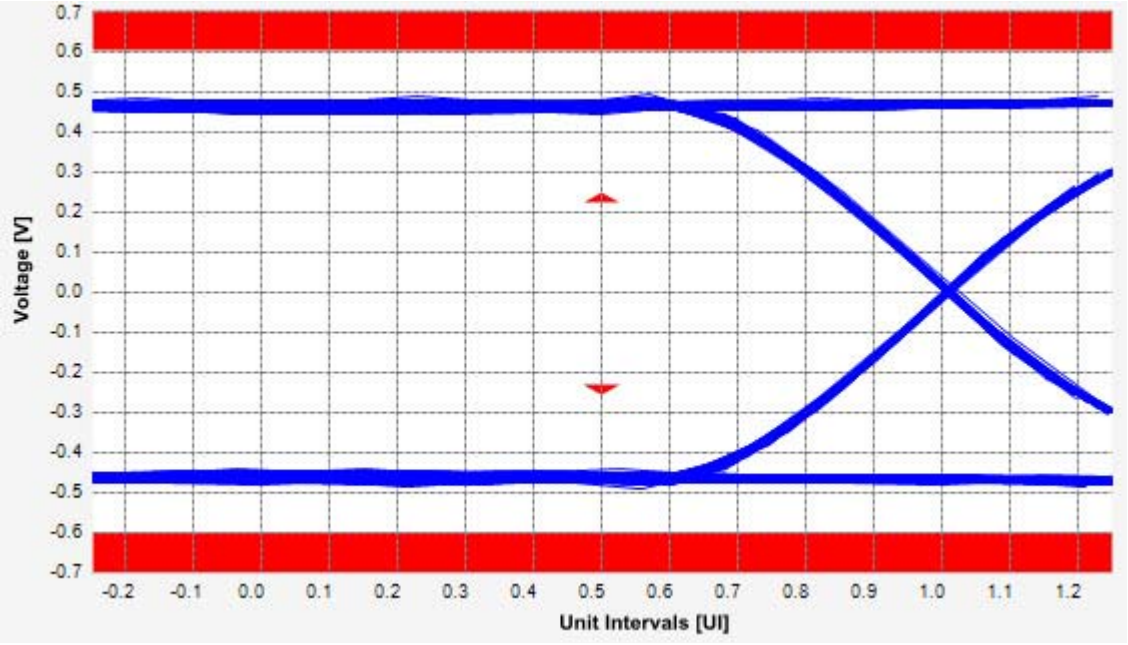


Figure 10 Reference Image for Template (Non-transition) Test

Median to Max Jitter Test

Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to the recovered T_X UI. The purpose of this test is to measure the median to max jitter between the jitter median and max deviation from the median.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 4 Median to Max Jitter Test Details

Symbol	Parameter	Max	Comments
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	0.125 UI	This parameter is measured differentially at zero crossing points on a 2.5GT/s clock recovery function.

Test Definition Notes from the Specification

Measurements at 5.0GT/s require an oscilloscope with a bandwidth of >= 12.5 GHz, or equivalent, while measurements made at 2.5GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5GT/s may be measured within 200mils of Tx device's pins although deconvolution is recommended. For measurement setup details, refer to Figure 4-23 and Figure 4-24. At least 10^6 UI of data must be acquired.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Signal Quality Tests" on page 38 and select **Median to Max Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTestWrapper.dll file.

2 Computes the median to max jitter using the following formula:

Median to max jitter = Maximum peak to peak jitter after filter /2

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `0.125UI >` $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 5 Eye Width Test Details

Symbol	Parameter	Min	Comments
$T_{TX\text{-}EYE}$	Minimum T_X Eye Width	0.75 UI	This parameter includes Rj at 10^{-12} and excludes single source clock or reference clock jitter.

Test Definition Notes from the Specification

- Measurements at 5.0GT/s require an oscilloscope with a bandwidth of >= 12.5 GHz, or equivalent, while measurements made at 2.5GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5GT/s may be measured within 200mils of Tx device's pins although deconvolution is recommended. For measurement setup details, refer to Figure 4-23 and Figure 4-24. At least 10^6 UI of data must be acquired.
- Transmitter jitter is measured by driving the Transmitter under test with a low jitter "ideal" clock and connecting the DUT to a reference load.
- Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5GT/s and 5.0GT/s use different filter functions that are defined in Figure 4-21. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.
- For 5.0GT/s, de-emphasis timing jitter must be removed. An additional HPF function must be applied as shown in Figure 4-21. This parameter is measured by accumulating a record length of 10^6 UI while the DUT outputs a compliance pattern. $T_{MIN\text{-}PULSE}$ is defined to be nominally 1 UI wide and is bordered on both sides by pulses of the opposite polarity. Refer to Figure 4-29.

NOTE The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Signal Quality Tests" on page 38 and select **Eye Width**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express Base Specification, Rev 2.0 as `0.75 UI <` T_{TX-EYE}.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 6 Peak Differential Output Voltage Test Details

Symbol	Parameter	Min	Max	Comments

Table 6 Peak Differential Output Voltage Test Details

$V_{TX-DIFF-PP}$	Differential p-p T_x Voltage Swing	0.80 V	1.2 V	The differential p-p T_x voltage swing parameter is defined as $2*\|V_{TXD+} - V_{TXD-}\|$ as measured with the compliance test load.

Test Definition Notes from the Specification

- $V_{TX-DIFFp-p} = 2*|V_{TX-D+} - V_{TX-D-}|$

.

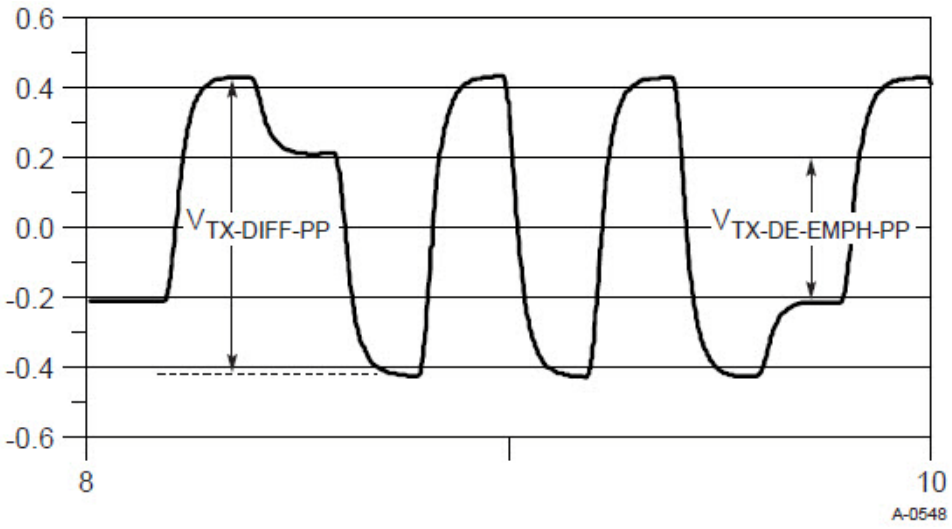


Figure 11 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Signal Quality Tests" on page 38 and select **Peak Differential Output Voltage (Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

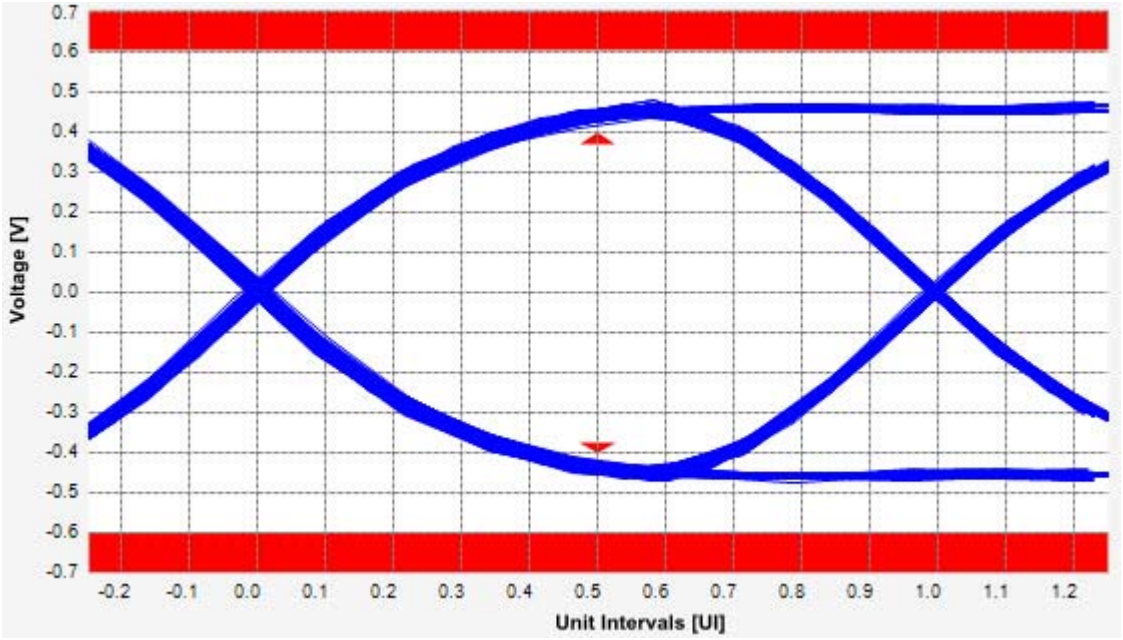


Figure 12 Reference Image for Peak Differential Output Voltage (Transition) Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 7 Peak Differential Output Voltage Test Details

Symbol	Parameter	Min	Max	Comments
$V_{TX-DIFF-PP}$	Differential p-p T_x Voltage Swing	0.80 V	1.2 V	The differential p-p T_x voltage swing parameter is defined as $2*\|V_{TXD+} - V_{TXD-}\|$ as measured with the compliance test load.

Test Definition Notes from the Specification

$$V_{TX-DIFFp-p} = 2*|V_{TX-D+} - V_{TX-D-}|$$

..

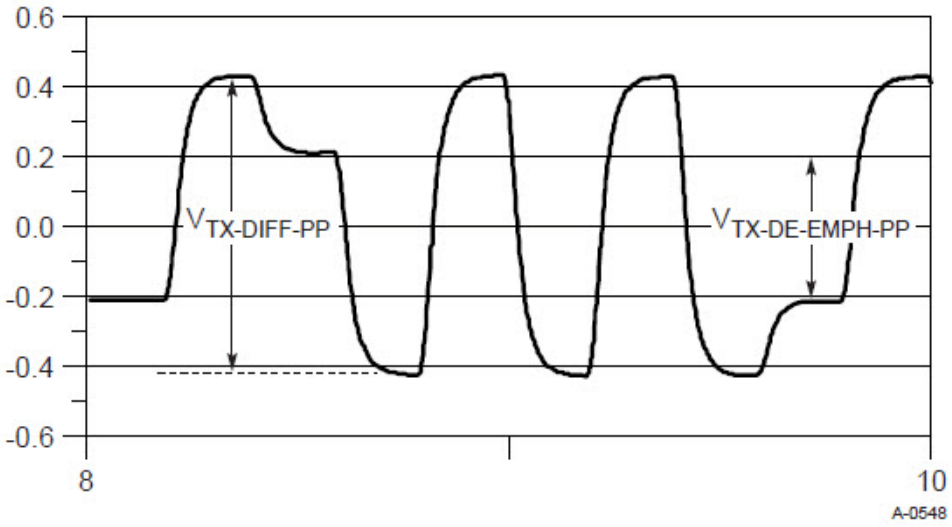


Figure 13 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Signal Quality Tests" on page 38 and select **Peak Differential Output Voltage (Non Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1. Extracts the non transition eye diagram data from the SigTestWrapper.dll file.
2. Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3. Finds the peak differential output voltage (non transition) mean value from the center of UI.
4. Compares the measured peak differential output voltage (non transition) value to the compliance test limits.
5. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

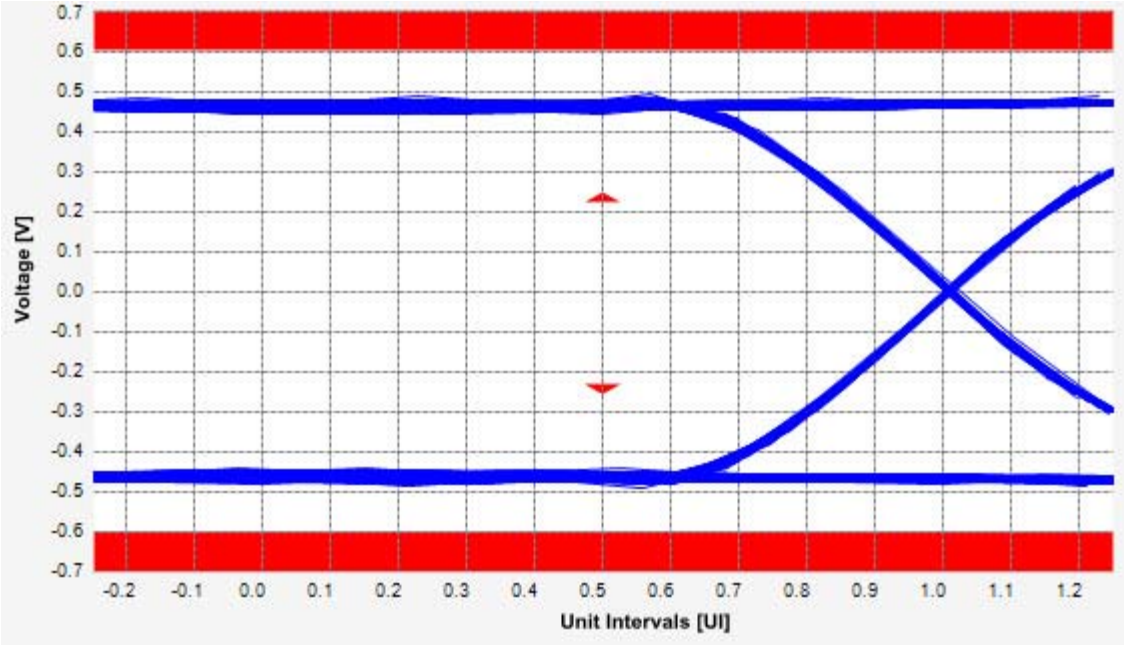


Figure 14 Reference Image for Peak Differential Output Voltage (Non-Transition) Test

Rise/Fall Time Test

Rise/Fall time is taken independently on each single ended waveform source when you use two single ended probes or two SMA cables as the signal source. Differential signal rise/fall time shows up when you select differential probe type measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform.

Rise Time. This measurement is the time difference of the values observed when the V_{REF-HI} and the V_{REF-LO} reference level are crossed on the rising edge of the waveform.

$$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$$

Where:

't_{RISE}' is a rise time measurement.

't_{HI+}' is a set of t_{HI} for rising edges only.

't_{LO+} is a set of t_{LO} for rising edges only.

'i' and 'j' are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}.

'n' is the index of rising edges in the waveform.

Rise time for $v_{D+}(t)$ is as follows:

$$t_{D+RISE}(n) = t_{D+HI+}(i) - t_{D+LO+}(j)$$

and for $v_{D-}(t)$:

$$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$$

Fall Time. This measurement is the time difference of the values observed when the V_{REF-HI} and the V_{REF-LO} reference level are crossed on the falling edge of the waveform.

$$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$$

Where:

't_{FALL}' is a fall time measurement.

't_{HI-}' is set of t_{HI} for falling edge only.

't_{LO-}' is set of t_{LO} for falling edge only.

'i' and j' are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

'n' is the index of falling edges in the waveform.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 8 Rise/Fall Time Test Details

Symbol	Parameter	Min	Comments
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	0.125 UI	This parameter is measured differentially from 20% to 80% of the swing.

NOTE The rise/fall time test is limited to only rising or falling edges of the consecutive transitions for transmitter measurements (TF2 and TR2 as shown in Figure 4-28). TF1 and TR1 are not covered in the current test procedure.

Test Definition Notes from the Specification

Measurements at 5.0GT/s require an oscilloscope with a bandwidth of >= 12.5 GHz, or equivalent, while measurements made at 2.5GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5GT/s may be measured within 200mils of Tx device's pins although deconvolution is recommended. For measurement setup details, refer to Figure 4-23 and Figure 4-24. At least 10^6 UI of data must be acquired.

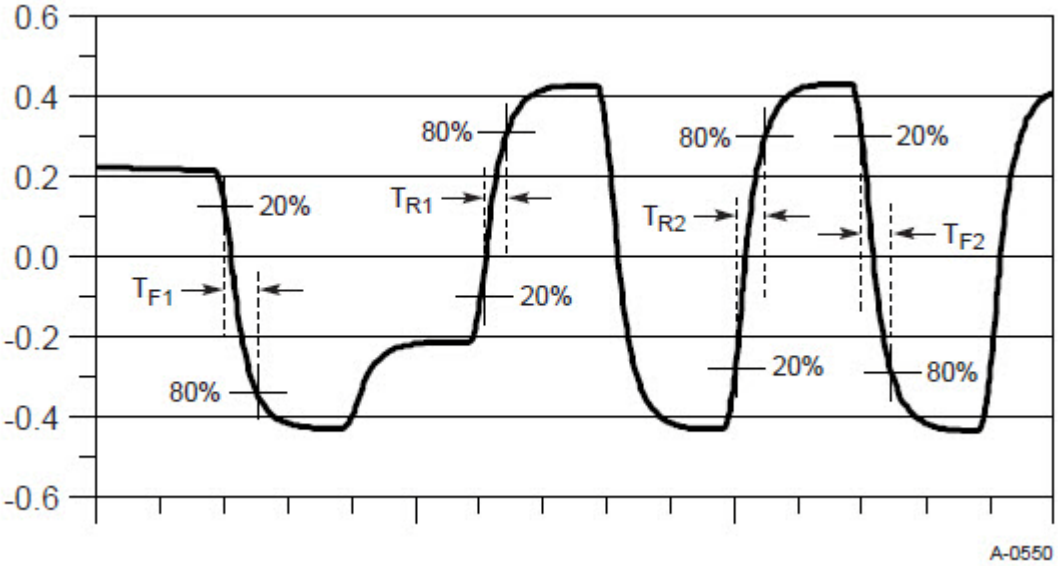


Figure 15 Rise and Fall Time Definition

Understanding the Test Flow

NOTE

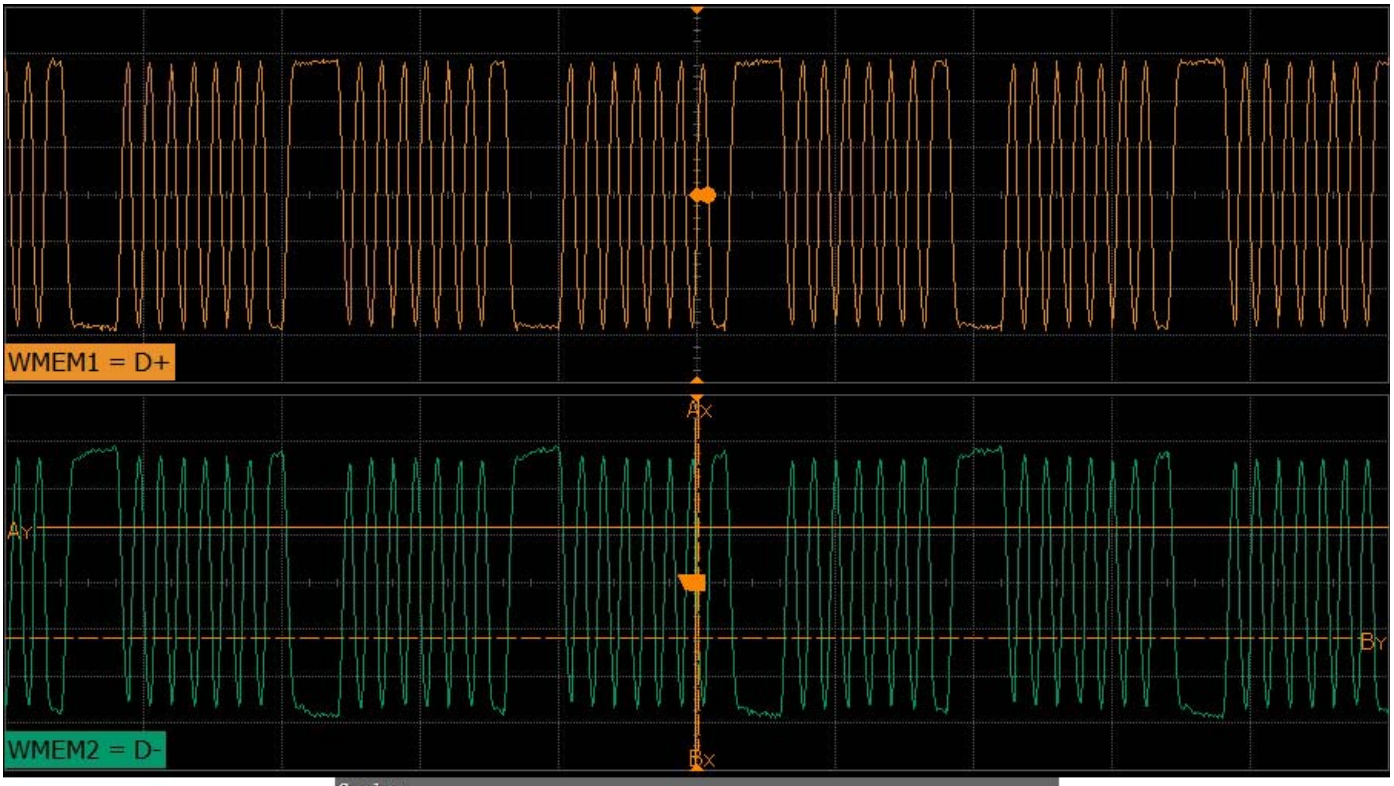
Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Signal Quality Tests" on page 38 and select **Rise/Fall Time**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   a. Sets the value of **Clock Recovery Method** as **First Order PLL**.
   b. Sets the value of **Nominal Data Rate** as **2.500000000Gb/s**.
   c. Sets the value of **Loop Bandwidth** as **1.500MHz**.
3. Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.
4. Measures the non - transition bits eye top and base.
5. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
6. Measures the transition bits eye top and base.
7. Configures **Thresholds** using **Measurement Analysis (EZJIT)** as follows:
   a. Sets **Thresholds** as **20%,50%,80% of Top, Base**.
   b. Defines **Top/Base** values using the previously measured eye top and base as **Histogram**.
8. If the **Transition Time Threshold** is configured as **Variable** using Automated Test Engine, then:
   a. Configures the value for **Setup Horizontal** to 50ps and **Center Reference** to 180ps.
   b. Configures **Real-Time Eye Setup** using **Serial Data**.
   c. Selects **Real-Time Eye Bits** as **Pattern Qualify** and measures the fall time de-emphasis bits.
   d. **Real-Time Eye Bits** as **Pattern Qualify** and measures the rise time de-emphasis bits.
   e. **Real-Time Eye Bits** as **Pattern Qualify** and measures the fall time transition bits.
   f. **Real-Time Eye Bits** as **Pattern Qualify** and measures the rise time transition bits.
   g. Reports the maximum and minimum value for rise and fall time.
   h. Reports the worst value as actual result.
9. Finds the minimum value from the minimum rise time and the minimum fall time. Compares the obtained value with the value as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $0.125\ UI < T_{TX\text{-}RISE}, T_{TX\text{-}FALL}$.
10. Reports the worst case measured rise/fall time value as the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales				
	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	5.000 ns/div	0.000s	83.75 mV/div	3.515 mV
Memory 2	5.000 ns/div	0.000s	82.00 mV/div	465.4 µV

Markers			
	Source	X Position	Y Position
A	Memory 2	-37.0000000000000 ps	96.714 mV
B	Memory 2	77.0000000000000 ps	-97.503 mV

Figure 16 Reference Image for Rise/Fall Time Test

Deemphasized Voltage Ratio Test

Deemphasized voltage ratio is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 9 Deemphasized Voltage Ratio Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0 dB	-4.0 dB

Test Definition Notes from the Specification

Root complex Tx de-emphasis is configured from Upstream controller. Downstream Tx de-emphasis is set via a command, issued at 2.5GT/s. For details, refer to the appropriate location in Section 4.2.

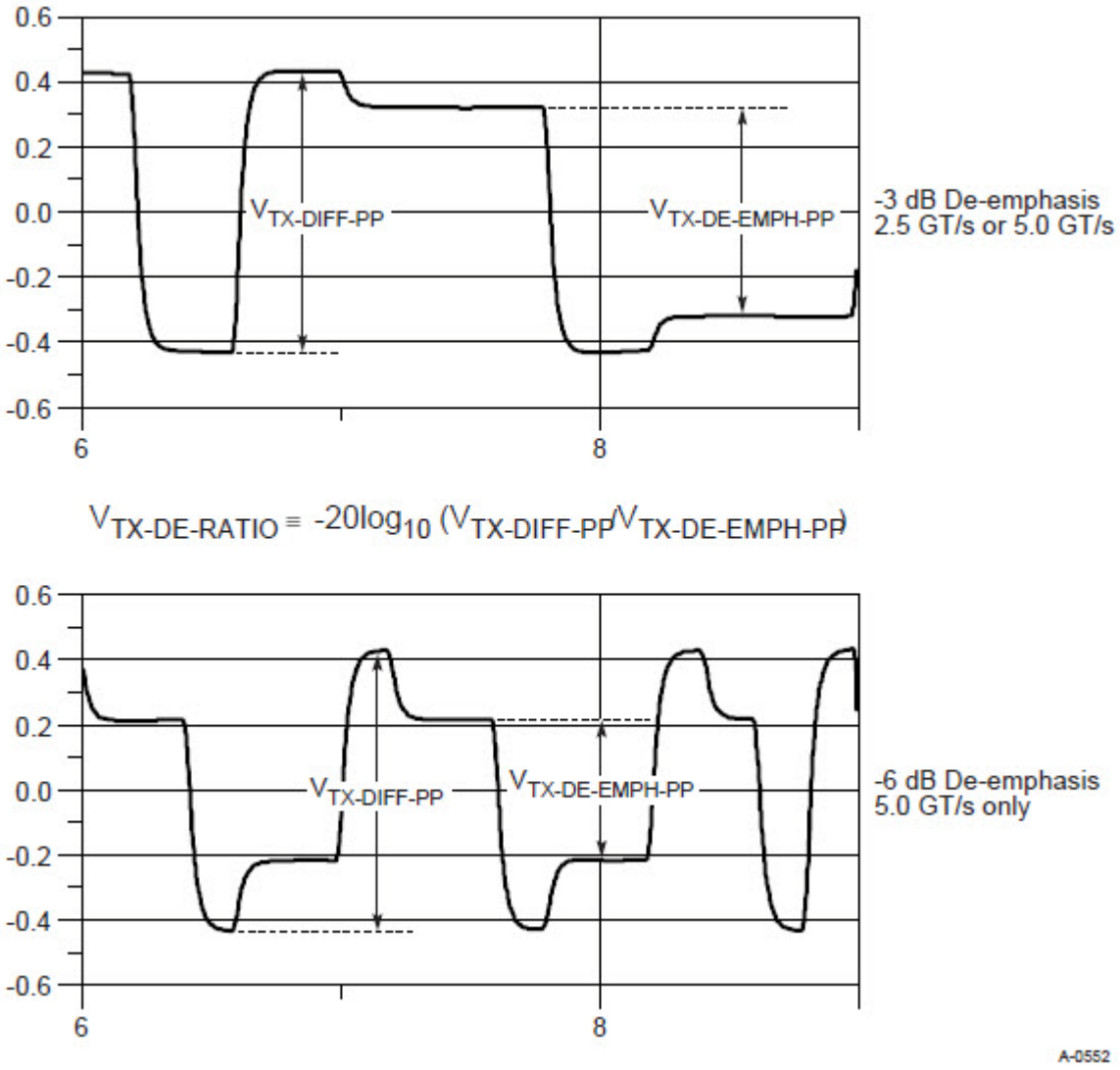


Figure 17 De-emphasized Voltage Ratio

Understanding the Test Flow

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Signal Quality Tests" on page 38 and select **Deemphasized Voltage Ratio**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:

   a Sets the value of **Clock Recovery Method** as **First Order PLL**.

   b Sets the value of **Nominal Data Rate** as **5.000000000Gb/s**.

   c Sets the value of **Loop Bandwidth** as **1.500MHz**.

3 Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.

4 Measures the non-transition bits eye top and base.

5 Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.

6 Measures the transition bits eye top and bases.

7 Finds the differential value between the transition bits eye top and base as $V_{TX\text{-}DIFF\text{-}PP}$ using **Histogram**.

8 Finds the differential value between the non-transition bits eye top and base as $V_{TX\text{-}DE\text{-}EMPH\text{-}PP}$ using **Histogram**.

9 Calculates de-emphasis ratio using the following formula:

$$\text{De-emphasis ratio} = -20*\log 10(V_{TX-DIFF-PP}/V_{TX-DE-EMPH-PP})$$

10 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $-4.0\ dB < V_{TX\text{-}DE\text{-}RATIO} < -3.0\ dB$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Running Common Mode Voltage Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to "Common Mode Voltage" in the "Transmitter (T_x) Tests" group.

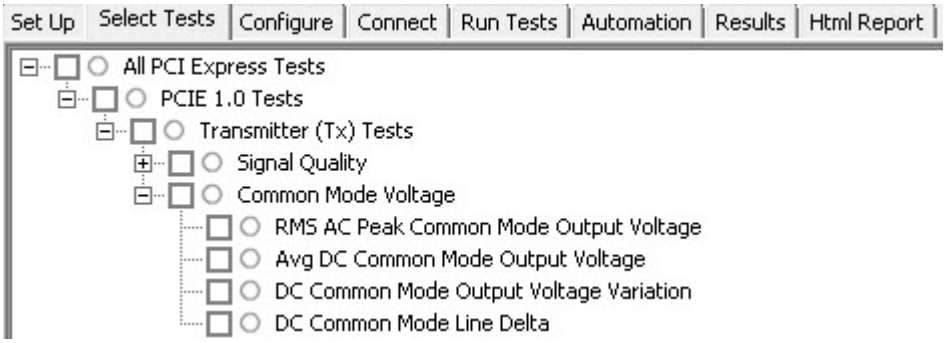


Figure 18 Selecting Transmitter (T_x) Common Mode Voltage Tests

RMS AC Peak Common Mode Output Voltage Test

The RMS AC Peak Common Mode Output Voltage is computed as:

$$V_{TX\text{-}AC\text{-}CM\text{-}p} = RMS[(V_{D+} + V_{D-})/2 - DC_{AVG}(V_{D+} + V_{D-})/2]$$

It is specified at the measurement point into a timing and voltage compliance test load and measured over any 250 consecutive T_X UIs.

NOTE This test is only available when the single-ended or SMA probing method has been used (see "Probing the Link for Tx Compliance" on page 34).

The AC common mode RMS voltage measurement calculates the RMS statistic of the common mode voltage waveform with the DC value removed.

$$v_{AC\text{-}RMS\text{-}CM}(i) = RMS\ (v_{AC\text{-}M}(i))$$

where:

'i' is the index of all waveform values.

'$v_{AC\text{-}RMS\text{-}CM}$' is the RMS of the AC common mode voltage signal.

'$v_{AC\text{-}M}$' is the AC common mode voltage signal.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 10 RMS AC Peak Common Mode Output Voltage Test Details

Symbol	Parameter	Max
$V_{TX\text{-}CM\text{-}AC\text{-}p}$	RMS AC Peak Common Mode Output Voltage	20 mV

Test Definition Notes from the Specification

$V_{TX\text{-}AC\text{-}CM\text{-}PP}$ and $V_{TX\text{-}AC\text{-}CM\text{-}P}$ are defined in Section 4.3.3.7. Measurement is made over at least 10^6 UI.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. Follow the procedure in "Running Common Mode Voltage Tests" on page 60 and select **RMS AC Peak Common Mode Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Sets up DC common mode voltage using **Math (FFT and more...)** as follows:
   a. Configures **Operator** as **Common Mode** measurements.
   b. Loads common mode signal.
   c. Measures the average of common mode using **V average** measurement from scope.
   d. Measures compliance test limit boundaries (0V to 3.6V) using **Markers**.
4. Measures **RMS Type** as **AC** and **Units** as **Volt** using **V rms Measurement**.
5. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $20\ mV > V_{TX\text{-}CM\text{-}AC\text{-}p}$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to

view the details. For information about the test results, refer to **Viewing Results** in the online help.

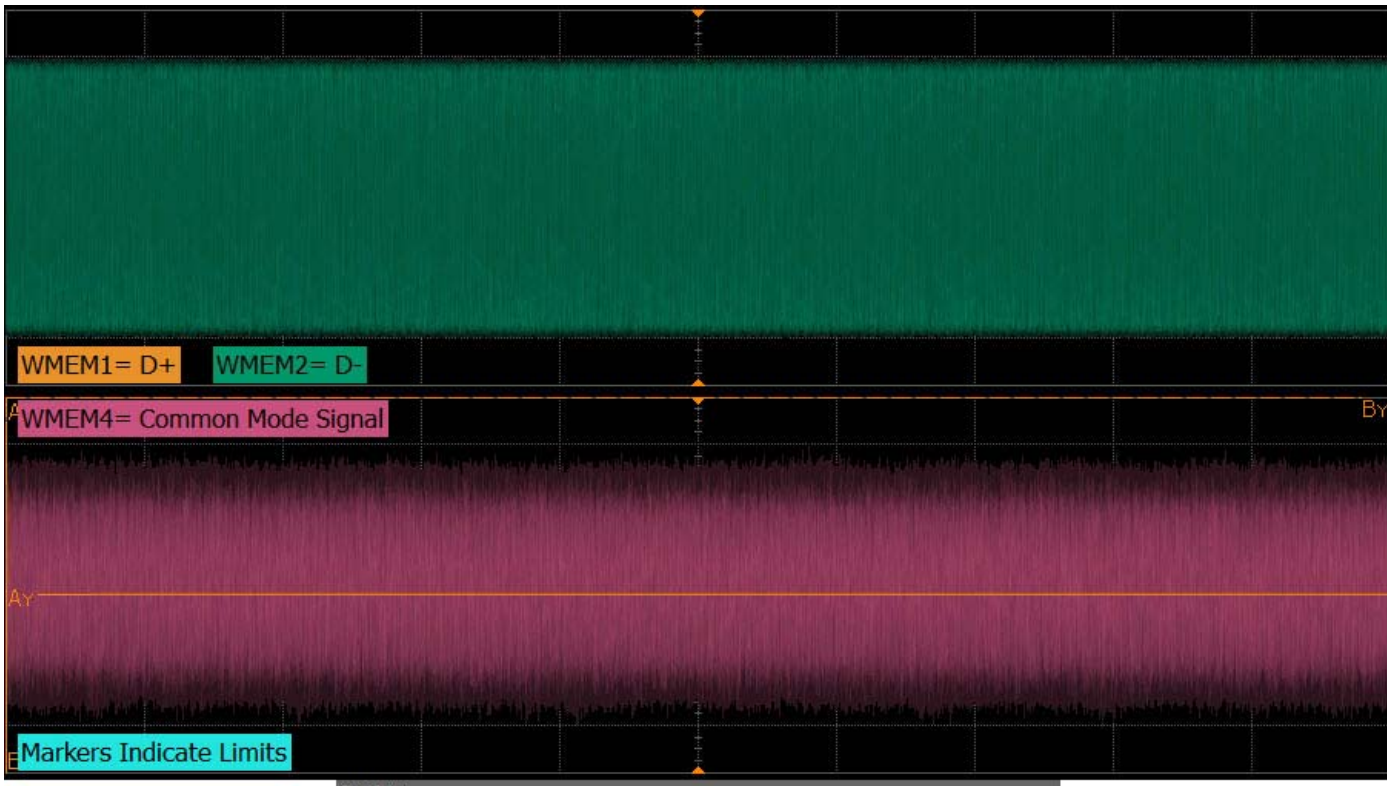


Figure 19 Reference Image for RMS AC Peak Common Mode Output Voltage Test

Avg DC Common Mode Output Voltage Test

The **Avg DC Common Mode Voltage** test measurement computes the DC average of the common mode signal:

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCI Express Base Specification, Rev 2.0 states that the transmitter DC common mode voltage ($V_{TX\text{-}DC\text{-}CM}$) must be held at the same value during all states.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 11 Avg DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

NOTE This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled. For more information, see "Probing the Link for Tx Compliance" on page 34.

Test Definition Notes from the Specification

The allowed DC common mode voltage at the Transmitter pins under any conditions.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Common Mode Voltage Tests" on page 60 and select **Avg DC Common Mode Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Setup DC common mode voltage as follows:

   a Enables and displays common mode measurements.

   b Loads common mode signal to waveform memory.

   c Loads and enhance dynamic range D+ signal and D- signal.

   d Enables the average common mode measurement.

   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).

4 Measures the average value of D+ and D- signal.

5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $V_{TX\text{-}DC\text{-}CM}$ is `0` to `3.6 V (+/- 100mV).`

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to

view the details. For information about the test results, refer to **Viewing Results** in the online help.

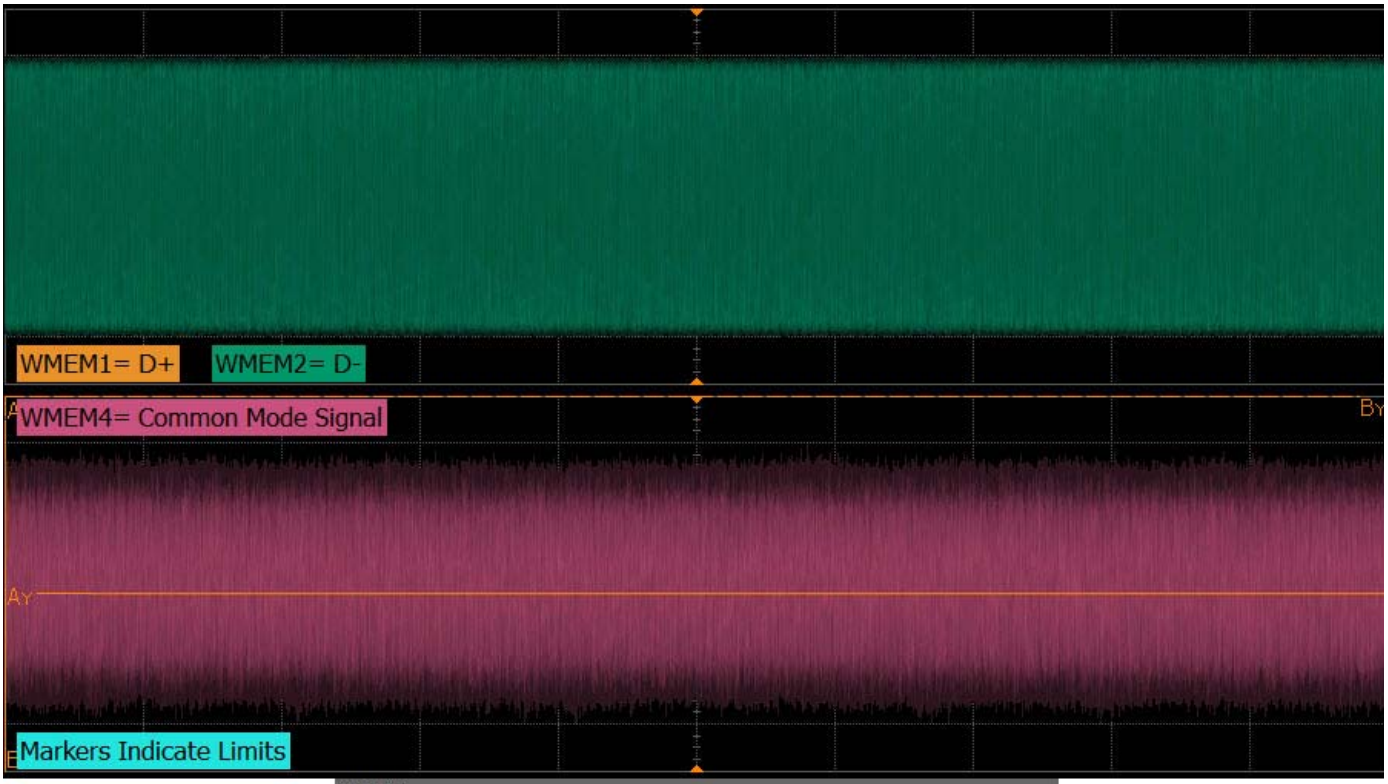


Figure 20 Reference Image for Average DC Common Mode Output Voltage Test

DC Common Mode Output Voltage Variation Test

The T_X DC common mode voltage ($V_{TX\text{-}DC\text{-}CM}$) must be held at the same value during all states. The allowable range for $V_{TX\text{-}DC\text{-}CM}$ is 0 to 3.6 V (+/- 100mV).

The **DC Common Mode Output Voltage Variation** test measurement computes the worst case positive or negative excursion of the common mode signal from the average DC Common Mode Voltage $V_{TX\text{-}DC\text{-}CM}$ as:

$$V_{TX\text{-}DC\text{-}CM\text{-}VARIATION} = |\text{Max}(\text{Max}\ (V_{CM(i)}), \text{Min}\ (V_{CM(i)})) - V_{TX\text{-}DC\text{-}CM}|$$

Where:

'i' is the index of all waveform values.

'V_{CM}' is the common mode signal (V_{TX-D+} + V_{TX-D-})/2.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 12 DC Common Mode Output Voltage Variation Test Details

Symbol	Parameter	Min	Max
$V_{TX-DC-CM}$	Transmitter DC common mode voltage	0 V	3.6V

Test Definition Notes from the Specification

The allowed DC common-mode voltage at the transmitter pins under any conditions.

NOTE This test is only available when the single-ended or SMA probing method has been used (see "Probing the Link for Tx Compliance" on page 34).

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Common Mode Voltage Tests" on page 60 and select **DC Common Mode Output Voltage Variation**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Avg DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the average DC common mode output voltage test:
   - **a** Maximum common mode value
   - **b** Minimum common mode value
2 Finds the worst value between maximum common mode value and minimum common mode value.

3 Computes the DC common mode line delta by absolute the difference between average DC value of D+ and average DC value of D-.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $0<=|V_{TX-DC-CM-VARIATION}|<=100$ mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common Mode Line Delta Test

The **DC Common Mode Line Delta** computes the absolute difference between the average value of the D+ and the D- waveforms signals.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 13 DC Common Mode Line Delta Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0m V	25 mV

Test Definition Notes from the Specification

$$|V_{TX-CM-DC-D+\ [during\ L0]} - V_{TX-CM-DC-D-\ [during\ L0]}|<=25mV$$

Where,

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $|V_{TX-D+}|$ [during L0]

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $V_{TX-D-}|$ [during L0]

NOTE This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled. For more information, see "Probing the Link for Tx Compliance" on page 34).

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Common Mode Voltage Tests" on page 60 and select **DC Common Mode Line Delta**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the average DC common mode output voltage test.

1 Reports the following measurement results obtained from running the average DC common mode output voltage test:
   - **a** DC Common Mode Line Delta
   - **b** Average DC value of D+
   - **c** Average DC value of D-
2 Computes the DC common mode line delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $V_{TX\text{-}CM\text{-}LINE\text{-}DELTA} < 25mV$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

4 Transmitter (Tx) Tests, PCI-E 1.0a, Low Power

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

The *Mobile Graphic Low Power Addendum to The PCIE Base Specification 1.0* describes the reduced power requirement of a transmitter on Mobile Platform. To meet low power requirement, a device must be compliant to the PCIE Base Specfication 1.0a except for electrical specification in section 2.2 of the addendum. The addendum also states that a low power device does not implement de-emphasis.

PCIE 1.0a Low Power Transmitter Tests consist of all tests from PCIE 1.0 Full (Standard) Power Tests except de-emphasis tests. The following table shows all the PCIE 1.0a Low Power Tests:

Table 14 PCIE 1.0a Low Power Transmitter Tests

Test Name	Remarks	See
Unit Interval	Same as Full Power	page 39.
Template Tests	Different	page 41.
Median to Max Jitter	Different	page 45.
Eye-Width	Different	page 46.
Peak Differential Output Voltage	Different	page 48.
Rise/Fall Time	Same as Full Power	page 53.
RMS AC Peak Common Mode Output Voltage	Same as Full Power	page 61.
Avg DC Common Mode Output Voltage	Same as Full Power	page 63.
DC Common Mode Output Voltage Variation	Same as Full Power	page 66.
DC Common Mode Line Delta	Same as Full Power	page 68.

All the tests above remarked with “Same as Full Power” share the same Method of Implementation (MOI) with PCIE 1.0 Full Power (refer to the page numbers shown). The differences in the test method are described in this chapter.

Probing the Link for T_x Compliance

When performing low-power transmitter tests, probing is the same as for full-power tests. See "Probing the Link for Tx Compliance" on page 34.

T_x Compliance Test Load

When performing low-power transmitter tests, the compliance test load is the same as for full-power tests. See "Tx Compliance Test Load" on page 38.

Running Signal Quality Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to "Signal Quality" in the "Transmitter (Tx) Tests" group.

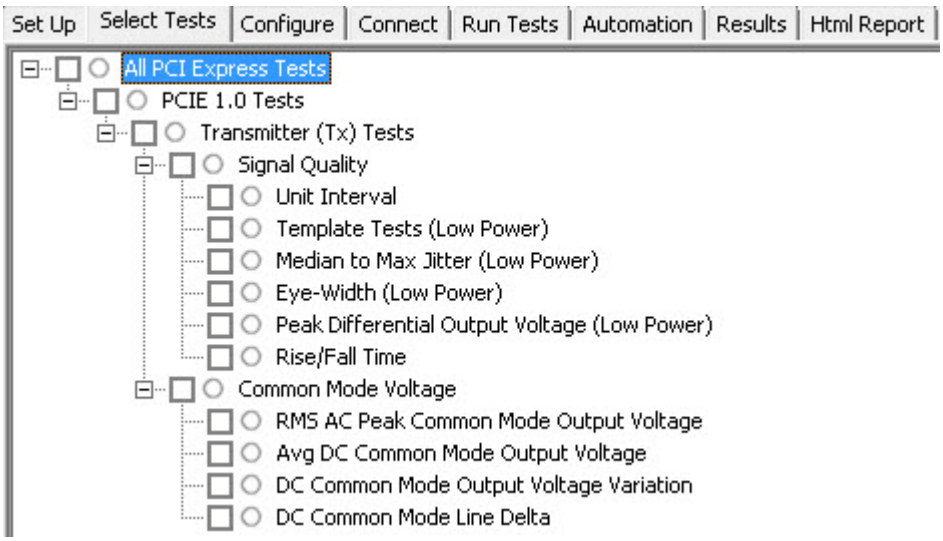


Figure 21 Selecting Transmitter (Tx) Signal Quality Tests

Unit Interval Test

When performing low-power transmitter tests, the T_x Unit Interval test is the same as for full-power tests. See "Unit Interval Test" on page 39.

Template Test (Low Power)

Test Definition/Reference

Mobile Graphics Low-Power Addendum to the PCI Express Base Specification 1.0

- Compliance of the transmitter eye diagram uses the same methodology as outlined in PCI Express Base 1.0a. The Tx eye diagram is specified using the passive compliance/test measurement load (see Figure 2-1 of Mobile Low Power PCIE Specification) in place of any real PCI Express interconnect plus Rx component. Because de-emphasis is not implemented, the transition and de-emphasized bit transitions are merged into a single Transmitter compliance eye diagram.
- The eye diagram must be valid for any 250 consecutive UIs.
- A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

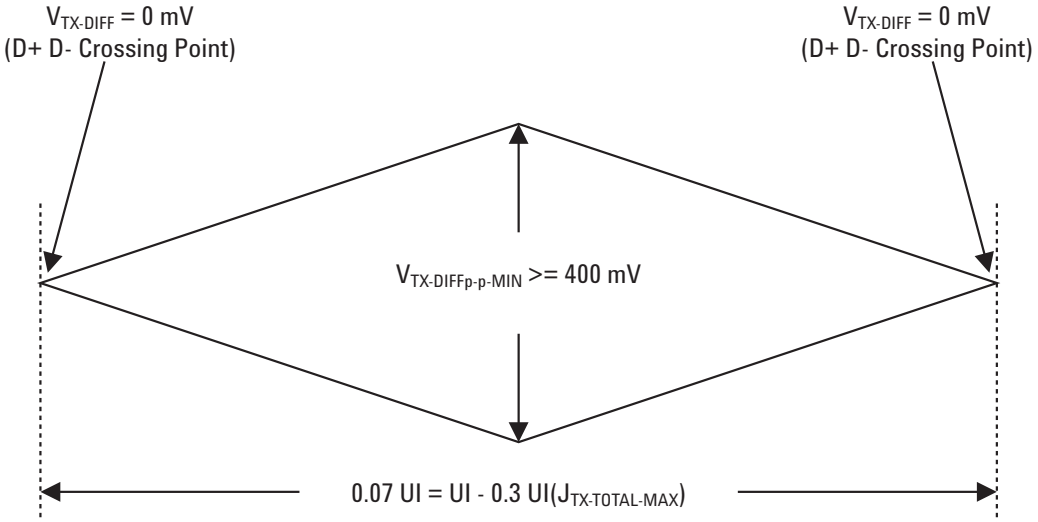


Figure 22 Transmitter Compliance Eye Diagram from Figure 2-2 of the Mobile Graphic Low-Power Addendum.

Difference in Test Procedure Compared to Full Power

- Different eye diagram used. The eye diagram can be found in Figure 2.2 of Mobile Low Power PCIE Specification.
- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Template Test" on page 41.

Median to Max Jitter Test (Low Power)

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Median to Max Jitter Test" on page 45.

Eye-Width Test (Low Power)

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Eye-Width Test" on page 46.

Peak Differential Output Voltage Test (Low Power)

Difference in Test Procedure Compared to Full Power

- Different specification used:

Table 15 $V_{TX\text{-}DIFFp\text{-}p}$ from Table 2-1 of the Mobile Graphic Low-Power Addendum.

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Pk-Pk Output Voltage	0.400 V		1.2 V

- $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{TX\text{-}D+} - V_{TX\text{-}D-}|$

See Also "Peak Differential Output Voltage (Transition) Test" on page 48.

Rise/Fall Time Test

When performing low-power transmitter tests, the Tx Rise/Fall Time test is the same as for full-power tests. See "Rise/Fall Time Test" on page 53.

Running Common Mode Voltage Tests

When performing low-power transmitter tests, the common mode voltage tests are the same as for full-power tests. See "Running Common Mode Voltage Tests" on page 60.

5
Receiver (R_x) Tests, PCI-E 1.0a

This section provides the Methods of Implementation (MOIs) for Receiver tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

NOTE

None of the included receiver tests validate the receiver's ability to correctly receive data (also known as receiver tolerance). Rather, they validate that the signal as seen by the receiver meets or exceeds various parameters (maximum voltage, jitter, eye width, etc.). These tests validate the transmitter and interconnect. Separate receiver tolerance testing is required to ensure the receiver is correctly receiving data.

Probing the Link for Rx Compliance

Receiver tests are done by probing the link as close as is feasibly possible to the pins of the receiver device. Alternatively, a dummy load can be used for the termination of the link. To probe the receiver link, you can:

- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the Ch2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

Table 16 Probing Options for Receiver Testing

	Probing Configurations			Captured Waveforms	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**
DUT Connection	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No

Single-Ended Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

Channel-to-channel deskew is required using this technique because two channels are used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

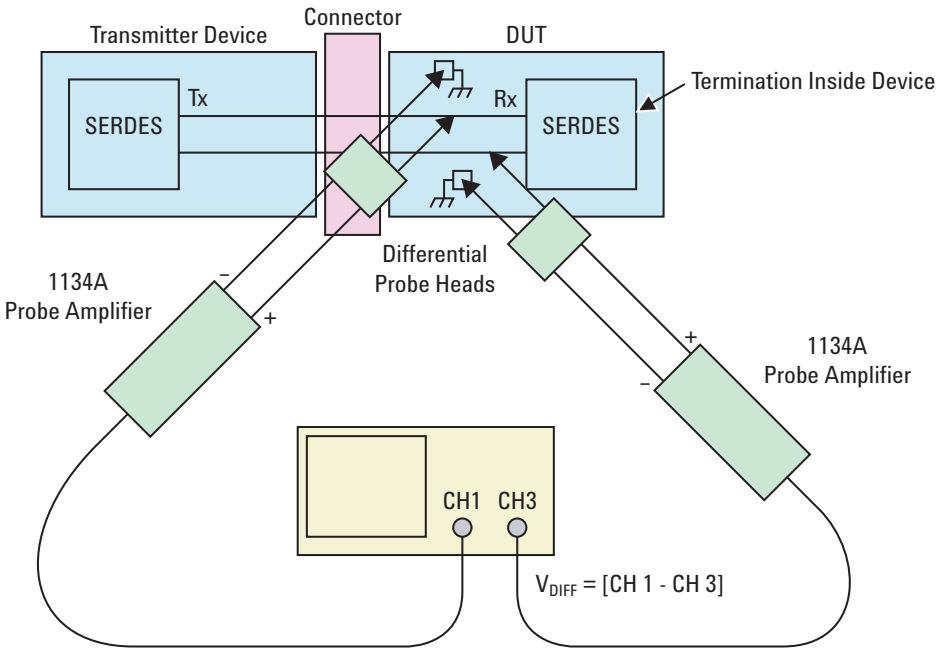


Figure 23 Single-Ended Probing

Differential Probing (Ch2)

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

A single channel of the oscilloscope is used, so de-skew is not necessary.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

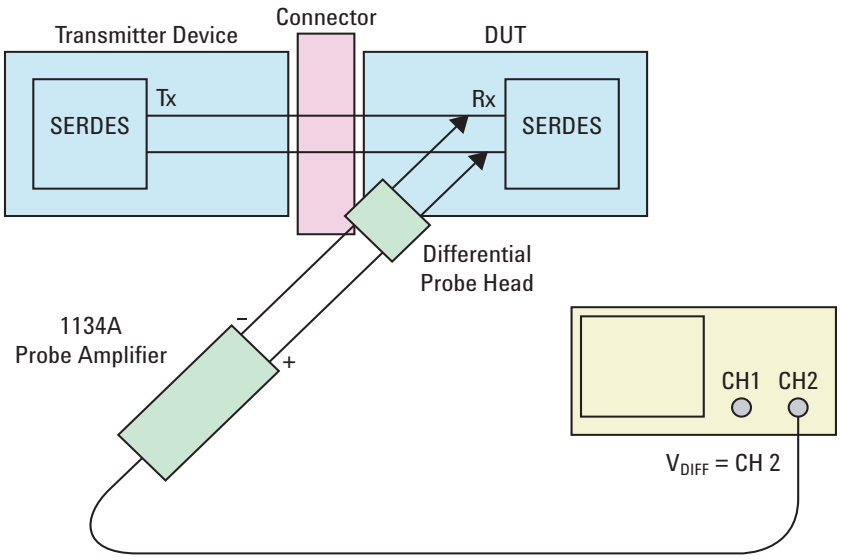


Figure 24 Differential Probing

Running Receiver Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "Receiver (R_x) Tests" group.

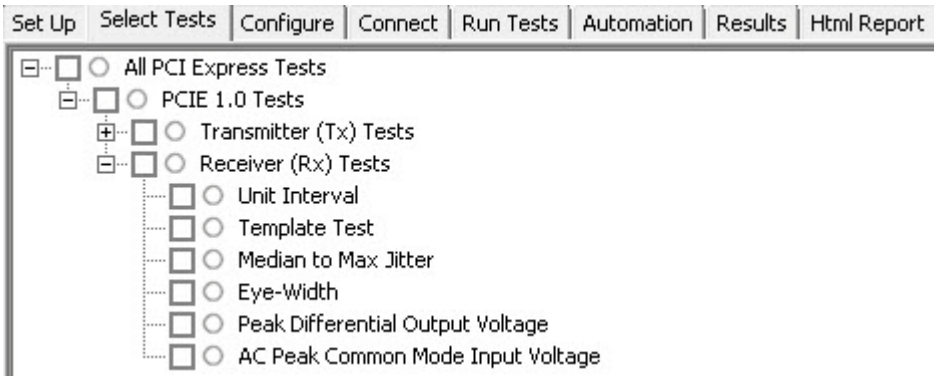


Figure 25 Selecting Receiver (Rx) Tests

Unit Interval Test

A recovered receiver unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$R_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The R_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another R_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case R_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 17 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- UI is specified to be +/-300 ppm.
- UI does not account for SSC dictated variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

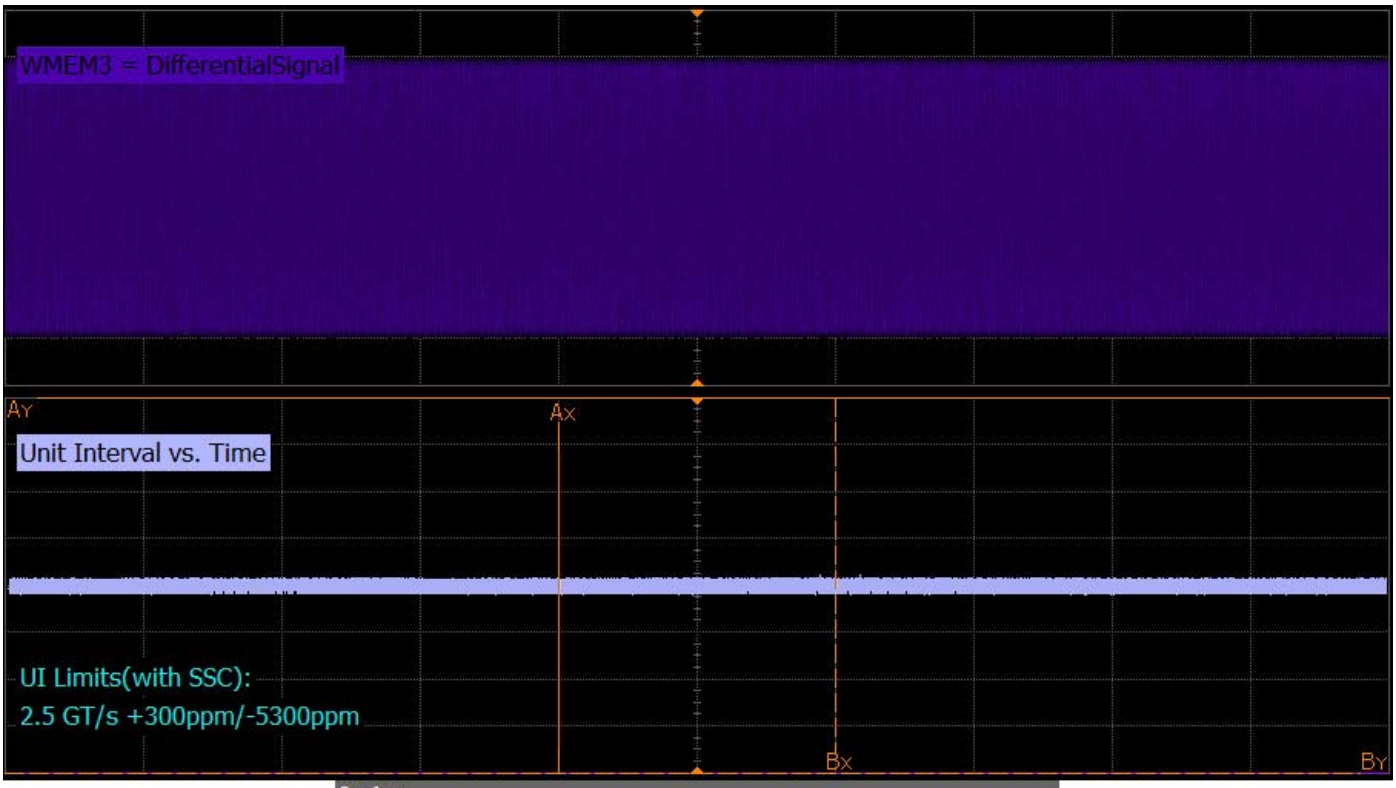
NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Receiver Tests" on page 81 and select **Unit Interval**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Fits and displays all sample data on screen.
3. Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a. Selects **Unit Interval** as data measurement analysis unit.
   b. Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.
4. Indicates the upper and lower limit of the measured data using markers.
5. Measures the minimum, mean and maximum values of the UI.
6. Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `399.88ps < UI < 400.12ps`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

NOTE The MOI for the measurement of UI at the receiver is identical to measuring it at the transmitter, with the exception of the test point. Refer to "Unit Interval Test" on page 39.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	40.00 µs/div	0.000s	20.00 fs/div	400.0 ps
Memory 3	40.00 µs/div	0.000s	162.5 mV/div	2.240 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-40.0000000200000 µs	400 pV
B	Function 3	40.0000000200000 µs	400 pV

Figure 26 Reference Image for Unit Interval Test

Template Test

A receiver must reliably receives all data that meets the differential receiver input specifications as shown in PCI Express Base Specification, rev 2.0. This test does not validate the receiver's tolerance.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 18 Template Test Details

Symbol	Parameter	Min	Max

Table 18 Template Test Details

$V_{RX-DIFF-PP-CC}$	Differential R_x peak-peak voltage for common Refclk Rx architecture	0.175V	1.2V
$V_{RX-DIFF-PP-DC}$	Differential R_x peak-peak voltage for data clocked Rx architecture	0.175V	1.2V

- All links are assumed active while generating the eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level.
- For more information on the receiver parameter details, refer to Section 4.3.7.2.2 of the base specification.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Receiver Tests" on page 81 and select **Template Test**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the receiver compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the mean differential p-p R_x voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the base specification as $0.175V < V_{RX-DIFF-PP-CC} < 1.2V$ and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is

captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

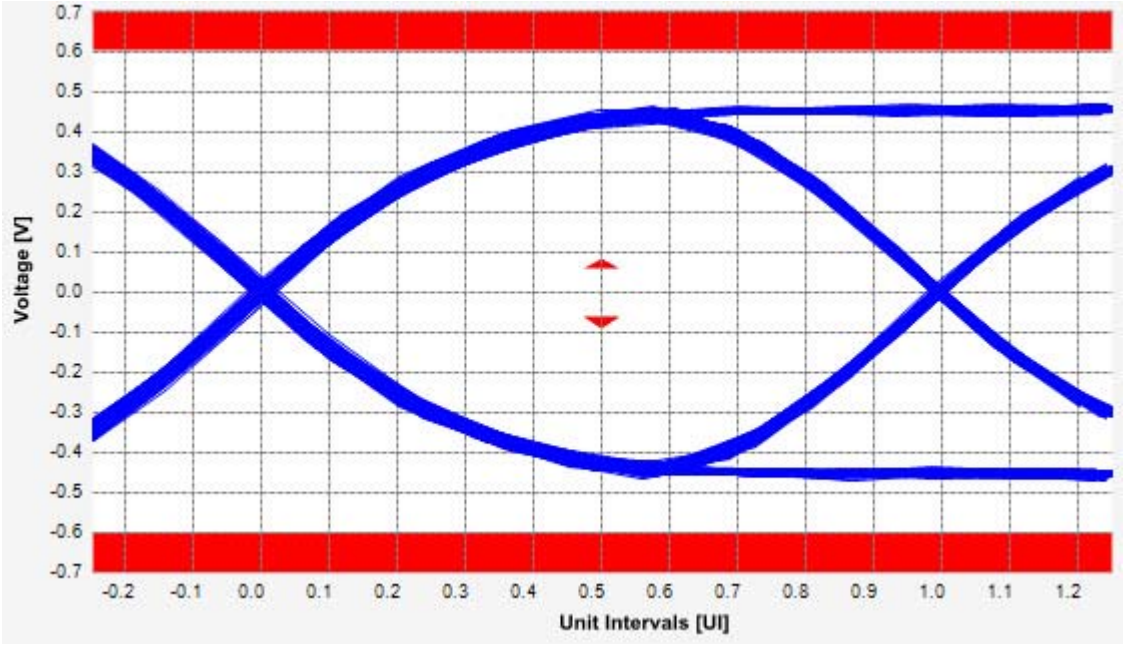


Figure 27 Reference Image for Template (transition) Test

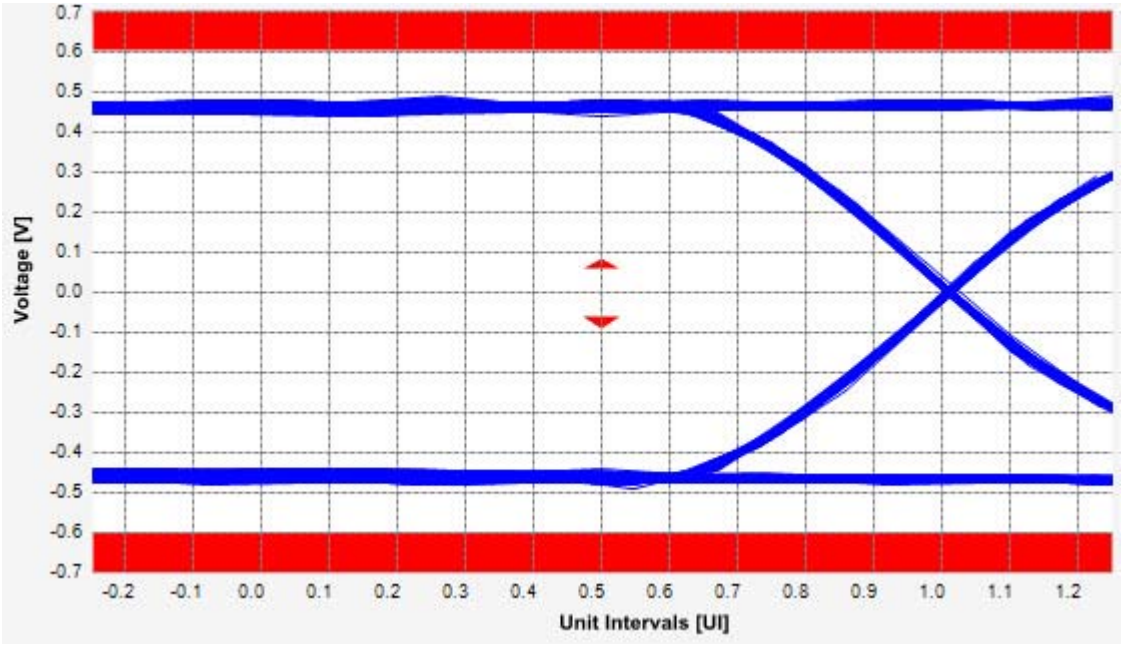


Figure 28 Reference Image for Template (non-transition) Test

Median to Max Jitter Test

Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to the recovered T_X UI. The purpose of this test is to measure the median to max jitter between the jitter median and max deviation from the median.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 19 Median to Max Jitter Test Details

Symbol	Parameter	Max
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time delta between median and deviation from the median.	0.3UI

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Receiver Tests" on page 81 and select **Median to Max Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTestWrapper.dll file.

2 Computes the median to max jitter using the following formula:

Median to max jitter = Maximum peak to peak jitter after filter /2

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the base specification as `0.3UI >` $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 20 Eye Width Test Details

Symbol	Parameter	Min	Comments
T_{RX-EYE}	Receiver eye time opening	0.40 UI	Minimum eye time at R_x pins to yield a 10^{-12} BER.

Test Definition Notes from the Specification

Receiver eye margins are defined into a 2 x 50 Ω reference load. A receiver is characterized by driving it with a signal whose characteristics are defined by the parameters specified in Table 4-10 and Table 4-11.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Receiver Tests" on page 81 and select **Eye Width**.

The PCI Express test application performs the following automated steps for measuring the **Eye Width** test based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express Base Specification, Rev 2.0 as `0.40UI <` T_{RX-EYE}.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform.

$$V_{RX-DIFF-PP-CC} = 2*Max(Max(V_{DIFF(i)}),M(axin)(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 21 Peak Differential Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{RX-DIFF-PP-CC}$	Differential p-p T_x Voltage Swing	0.175 V	1.2 V

NOTE For more information on the peak differential output voltage test definition, refer to Section 4.3.7.2.2 of the base specification.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Receiver Tests" on page 81 and select **Peak Differential Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1. Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2. Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3. Finds the peak differential output voltage (transition) mean value from the center of UI.
4. Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

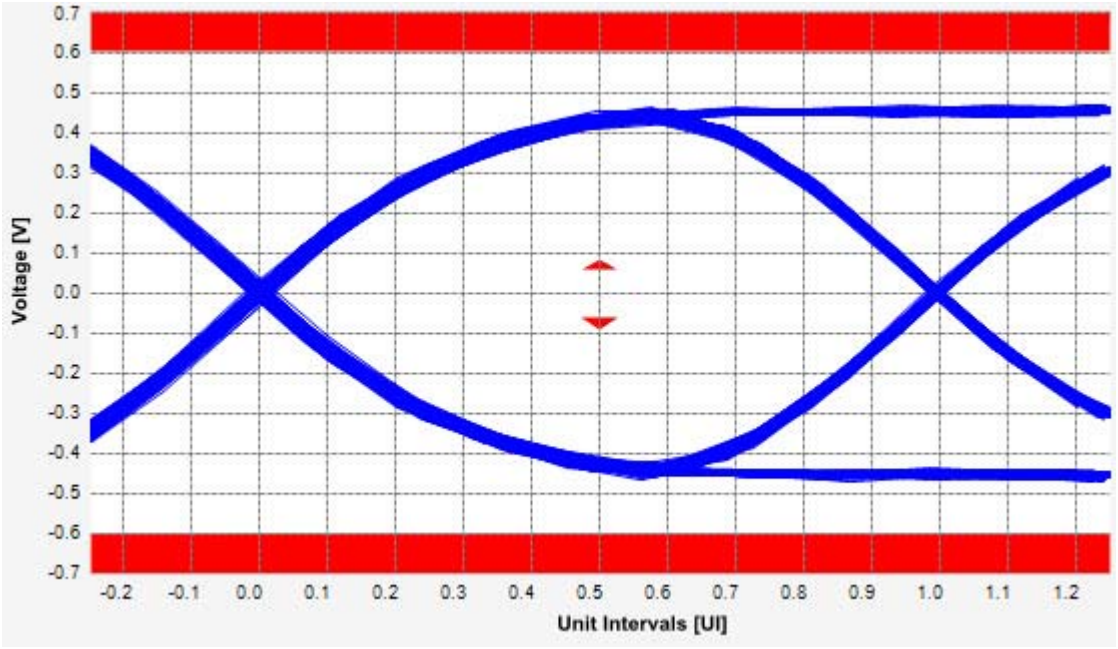


Figure 29 Reference Image for Peak Differential Output Voltage Test

AC Peak Common Mode Input Voltage Test

The average DC common mode voltage measurement computes the DC average of the common mode signal.

$$V_{TX\text{-}CM\text{-}DC} = DC_{AVG} \text{ of } |V_{TX\text{-}D+} + V_{TX\text{-}DC+}|/2$$

The PCIE Base Specification states that the transmitter DC common mode voltage must be held at the same value during all states.

NOTE This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel in put used), this test will be disabled. (see "Probing the Link for Rx Compliance" on page 78).

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 22 AC Peak Common Mode Input Voltage Test Details

Symbol	Parameter	Max	Comments
$V_{RX-CM-AC-P}$	RMS AC Common Mode Voltage	150 mV	Measured at Rx pins into a pair of 50 ohm terminations into ground.

Test Definition Notes from the Specification

Common Mode peak voltage is defined by the expression: max {|(Vd+ - Vd-) - V_{-CMDC}|}.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. Follow the procedure in "Running Receiver Tests" on page 81 and select **AC Peak Common Mode Input Voltage**.

The PCI Express test application performs the following automated steps for measuring the **AC Peak Common Mode Input Voltage** test based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Sets up DC common mode voltage using **Math (FFT and more...)** as follows:
   a. Configures **Operator** as **Common Mode** measurements.
   b. Loads common mode signal.
   c. Measures the average of common mode using V average measurement from scope.
   d. Measures compliance test limit boundaries (0V to 3.6V) using **Markers**.
4. Measures the average value of D+ and D- signal.
5. Computes DC common mode value by absolute the average of the total average value of the D+ signal and average value of D- signal.
6. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `150 mV >` $V_{RX-CM-AC-p}$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

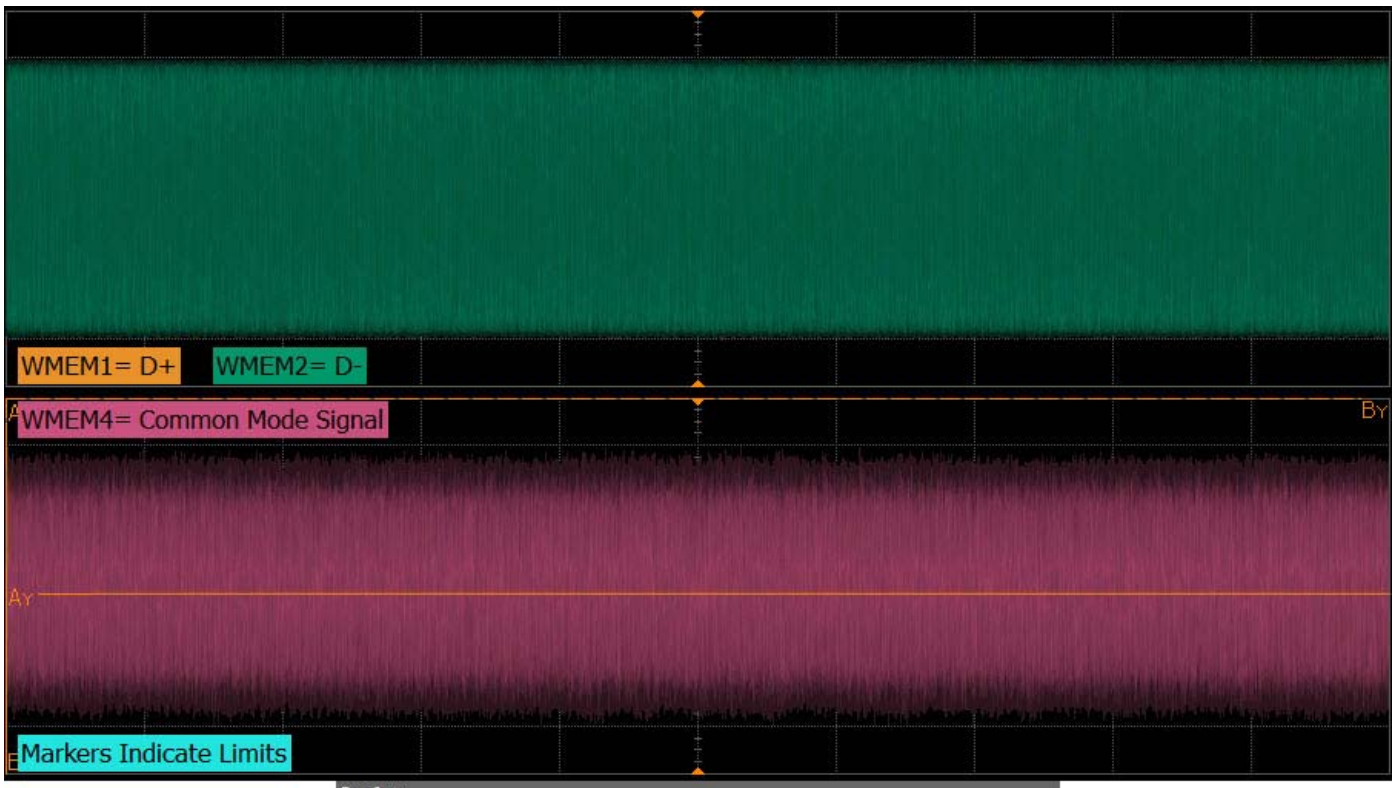


Figure 30 Reference Image for AC Peak Common Mode Input Voltage Test

6
Add-In Card (T_x) Tests, PCI-E 1.0a

This section provides the Methods of Implementation (MOIs) for Add-In Card tests using an Agilent 90000X Series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Add-In Card Compliance

Connecting the Signal Quality Load Board for Add-in Card Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 or by-1 connector slot.

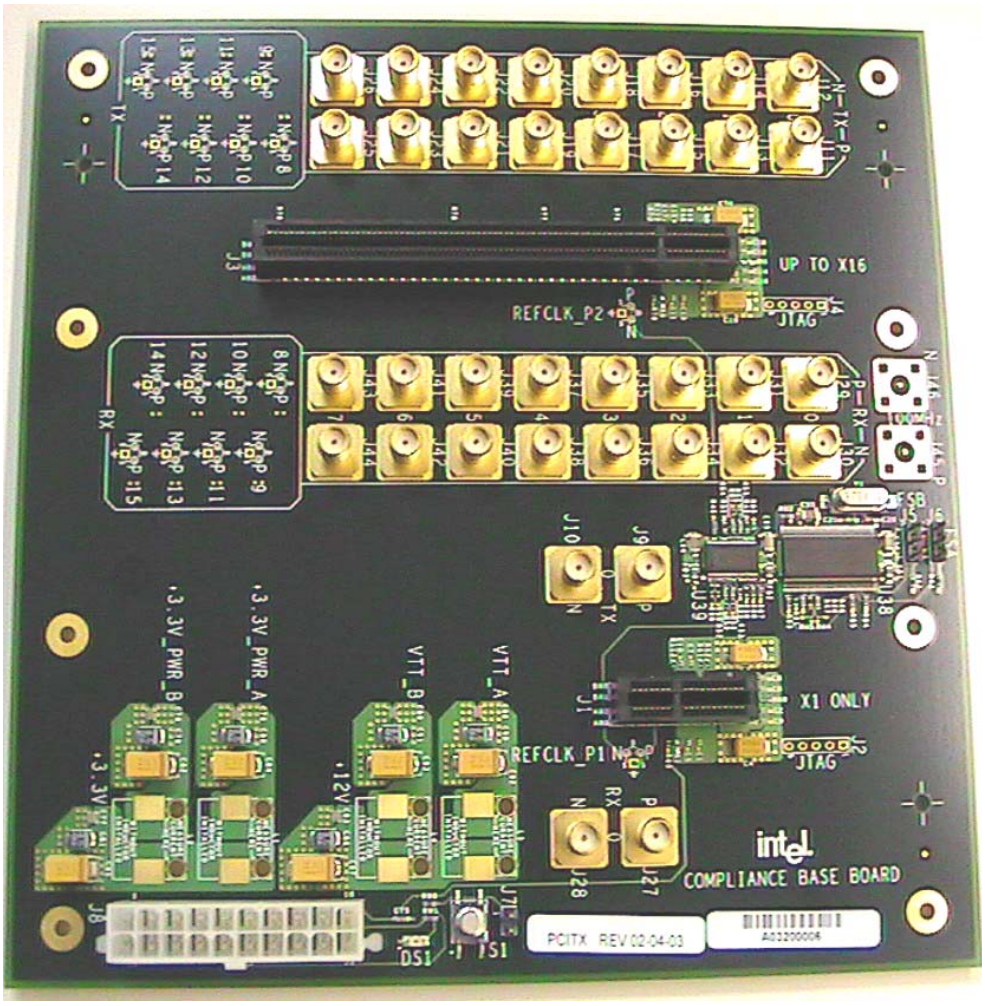


Figure 31 Compliance Base Board (CBB) Add-in Card Fixture

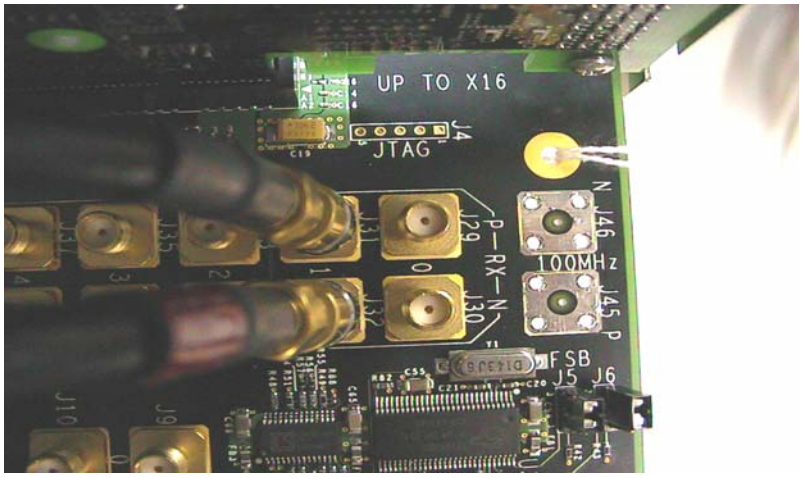


Figure 32 Compliance Base Board (CBB) SMA Probing Option

2 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the TX LANE P under test (where Lane 1 is under test in this example shown in Figure 32 above).

   b Digital Storage Oscilloscope channel 3 to the TX LANE N under test (where Lane 1 is under test in this example shown in Figure 32 above).

NOTE The Compliance Base Board labeled PCITX Rev 02-04-03 silkscreen incorrectly labels the add-in card transmitter probing locations as RX.

When SMA probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 626).

Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 33 on page 98). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

3 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

4 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

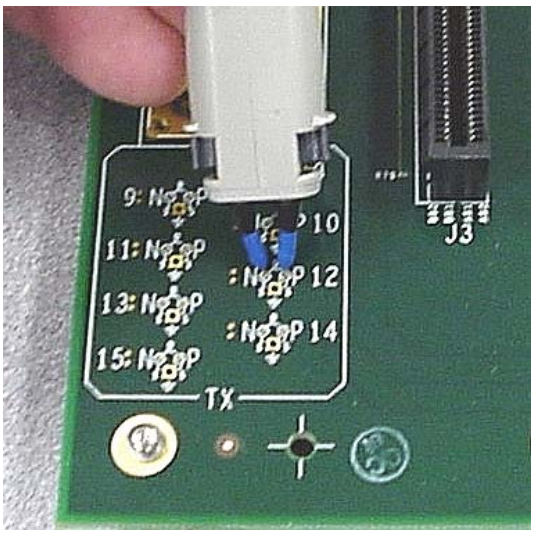


Figure 33 Compliance Base Board (CBB) Active Probing Option

Running Add-In Card Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "Add-In Card (T_x) Tests" group.

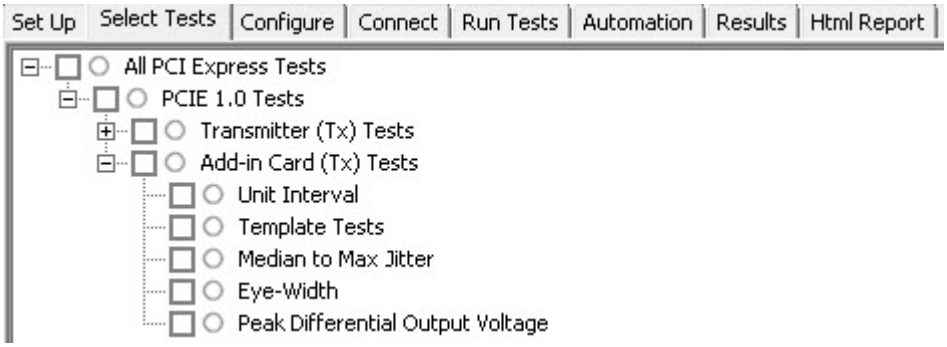


Figure 34 Selecting Add-In Card (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 23 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Add-In Card Tests" on page 99 and select **Unit Interval**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Fits and displays all sample data on screen.
3. Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a. Selects **Unit Interval** as data measurement analysis unit.
   b. Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.
4. Indicates the upper and lower limit of the measured data using markers.
5. Measures the minimum, mean and maximum values of the UI.
6. Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `399.88ps < UI < 400.12ps`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

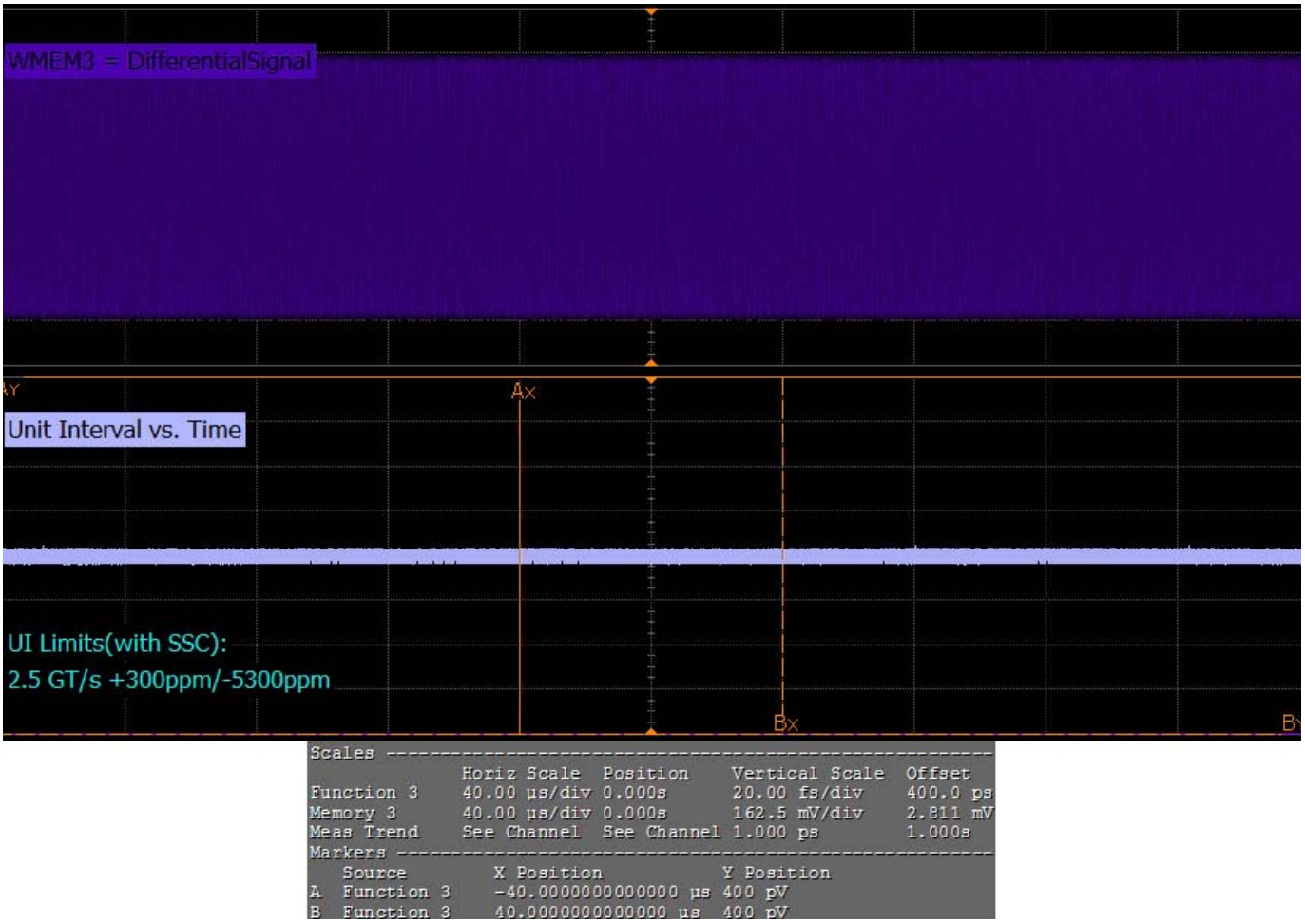


Figure 35 Reference Image for Unit Interval Test

Template Test

Add-in cards must meet the **Add-in Card Transmitter Path Compliance Eye-Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 1.0a, Section 4.7.1, Table 4-6 as

measured at the card edge-fingers. This test does not validate the receiver's tolerance, rather it validates that the signal at the receiver meets the specifications in Figure 4-8.

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.1 is used as reference to check the compliance of the DUT.

Table 24 Template Test Details

Symbol	Value
Vtx_A	>= 514 mV
$Vtx_{A\_}d$	>= 360 mV
Ttx_A	>= 237 ps

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level ($Vtx_{A\_}d$).
- The values in Table 4-6 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. Exact conditions required for verifying compliance while generating this eye diagram are be given in the compliance testing document. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 118.5 ps away from the jitter median.

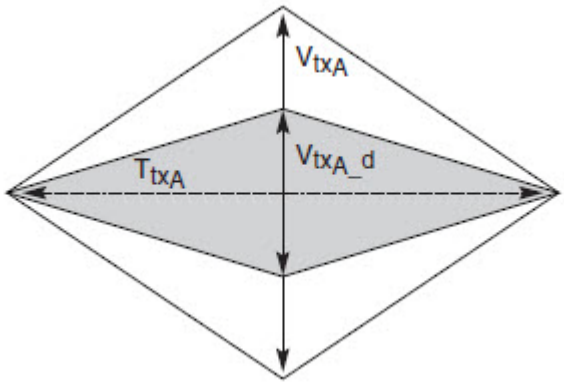


Figure 36 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Add-In Card Tests" on page 99 and select **Template Tests**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs compliance testing using the SigTestWrapper.dll file.
   a. Calls the add-in card compliance test function from the SigTestWrapper.dll file.
   b. Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.
3. Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.
4. Reports the mean differential voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 1.0a and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

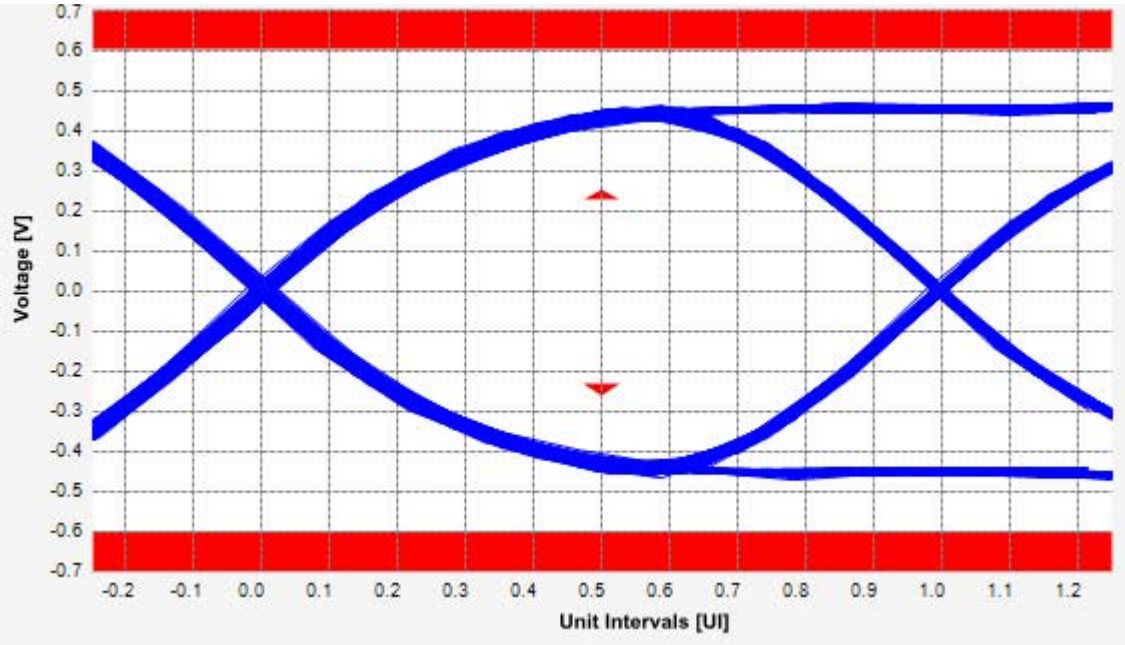


Figure 37 Reference Image for Template (Transition) Test

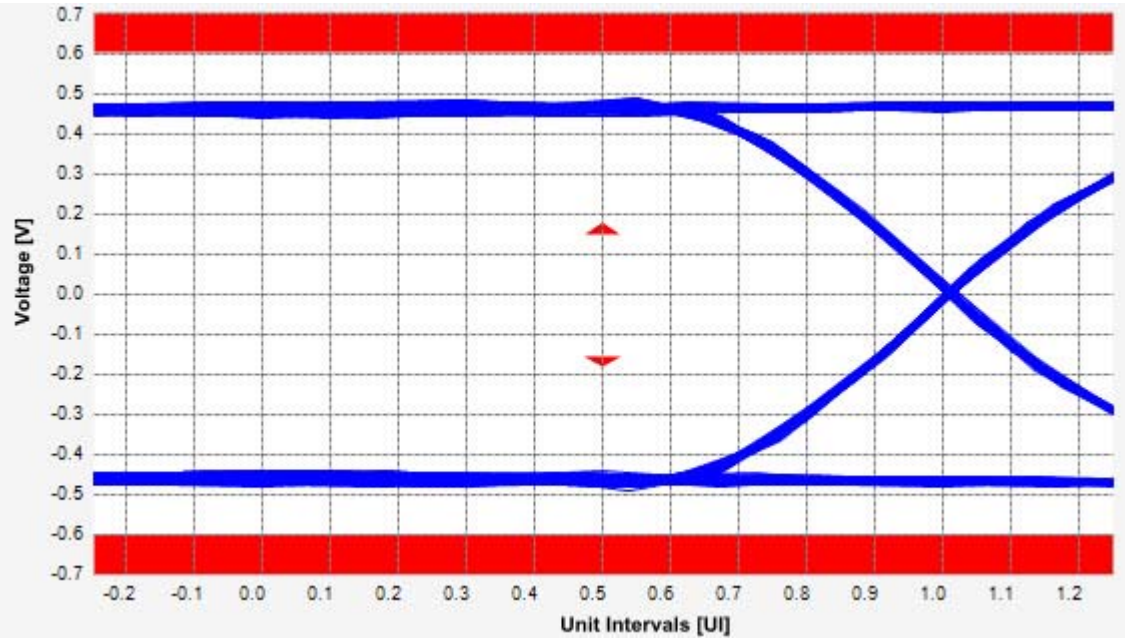


Figure 38 Reference Image for Template (Non-Transition) Test

Median to Max Jitter Test

Median to max jitter test measures the median to max jitter between the jitter median and max deviation from the median. The limit for the median to max jitter is calculated by the following equation:

$$\text{Median to max jitter} = (1\ UI - \text{Eye Width})/2$$

Where,

1 UI = 400ps

Eye Width = 237ps

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.1 is used as reference to check the compliance of the DUT.

Table 25 Median to Max Jitter Test Details

Symbol	Value
Vtx_A	>= 514 mV
$Vtx_{A\_}d$	>= 360 mV
Ttx_A	>= 237 ps

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{txA_d})
- The values in Table 4-6 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. Exact conditions required for verifying compliance while generating this eye diagram are be given in the compliance testing document. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 118.5 ps away from the jitter median.

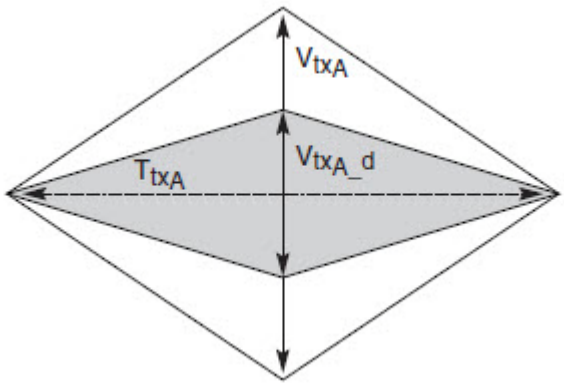


Figure 39 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 99 and select **Median to Max Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTestWrapper.dll file.

2 Computes the median to max jitter using the following formula:

Median to max jitter = Maximum peak to peak jitter after filter / 2

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 1.0a as 81.5ps.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is

captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.1 is used as reference to check the compliance of the DUT.

Table 26 Eye Width Test Details

Symbol	Value	Comments
Vtx_A	>= 514 mV	All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (Vtx_A_d).
Vtx_A_d	>= 360 mV	
Ttx_A	>= 237 ps	

Test Definition Notes from the Specification

The values in Table 4-6 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. Exact conditions required for verifying compliance while generating this eye diagram are be given in the compliance testing document. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 118.5 ps away from the jitter median.

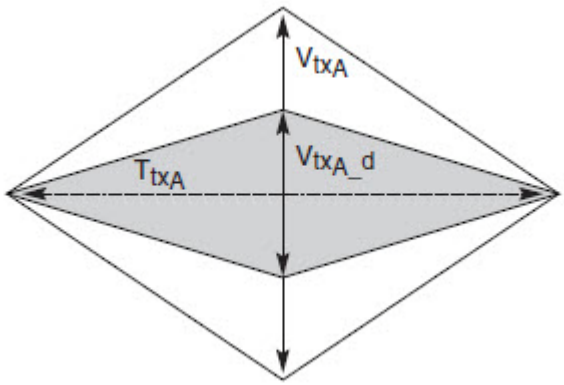


Figure 40 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 99 and select **Eye Width**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 1.0a.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits as T_{txA} >237ps.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to

view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),M(axin)(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.1 is used as reference to check the compliance of the DUT.

Table 27 Peak Differential Output Voltage Test Details

Symbol	Value
Vtx_A	>= 514 mV
Vtx_A_d	>= 360 mV
Ttx_A	>= 237 ps

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (VtxA_d).
- The values in Table 4-6 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card. Exact conditions required for verifying compliance while generating this eye diagram are be given in the compliance testing document. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 118.5 ps away from the jitter median.

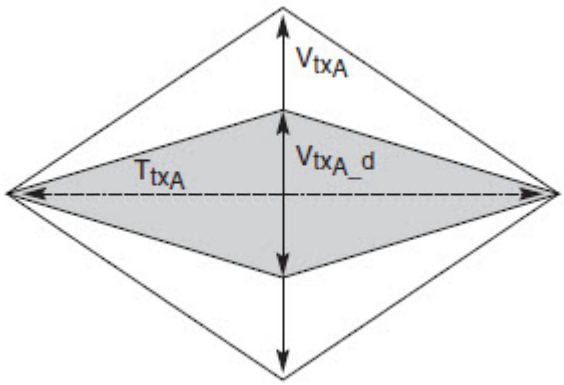


Figure 41 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 99 and select **Peak Differential Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1. Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2. Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3. Finds the peak differential output voltage (transition) mean value from the center of UI.
4. Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

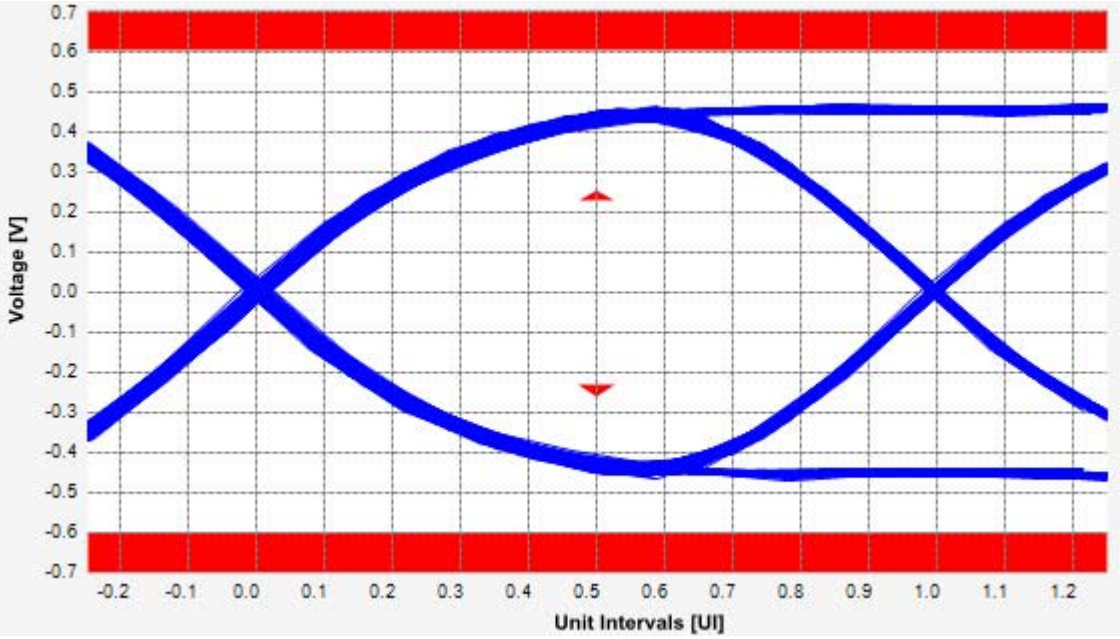


Figure 42 Reference Image for Peak Differential Output Voltage Test

7
System Board (Tx) Tests, PCI-E 1.0a

This section provides the Methods of Implementation (MOIs) for System Board tests using an Agilent 90000X Series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for System Board Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The PCI Express Signal Quality Load Board has edge fingers for x1, x4, x8 and x16 connectors.

   The PCI Express Signal Quality Load Board will cause a PCI Express 1.0a Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

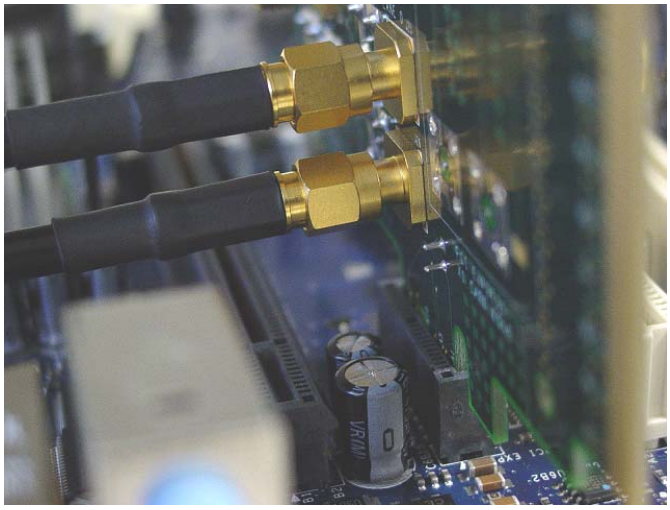


Figure 43 SMA Probing Option

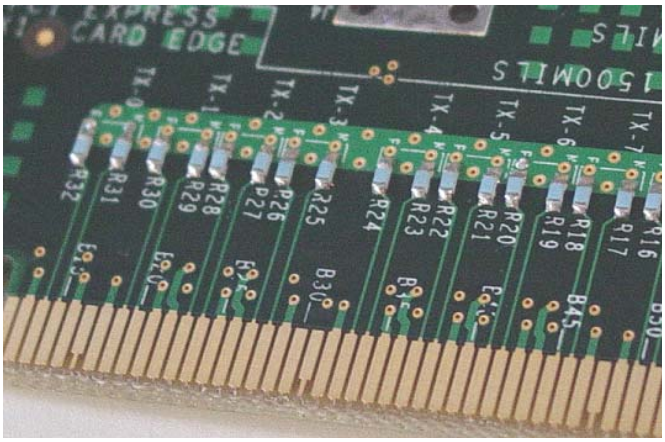


Figure 44 Resistor Terminations for Lanes without SMA Probing

2 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to TX LANE 1 P (where Lane 1 is under test).

   b Digital Storage Oscilloscope channel 3 to TX LANE 1 N (where Lane 1 is under test).

   When SMA probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 626).

   Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 33 on page 98). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

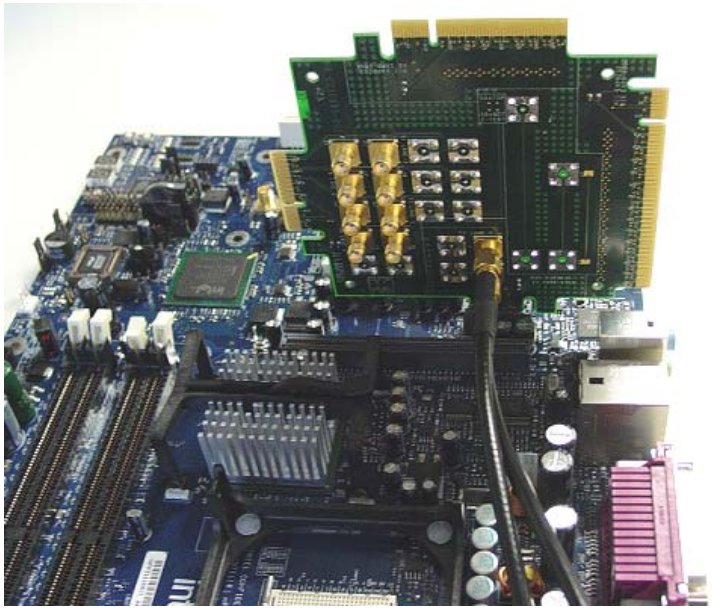


Figure 45 Connecting the PCI Express Signal Quality Test Fixture

Running System Board Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "System Board (Tx) Tests" group.

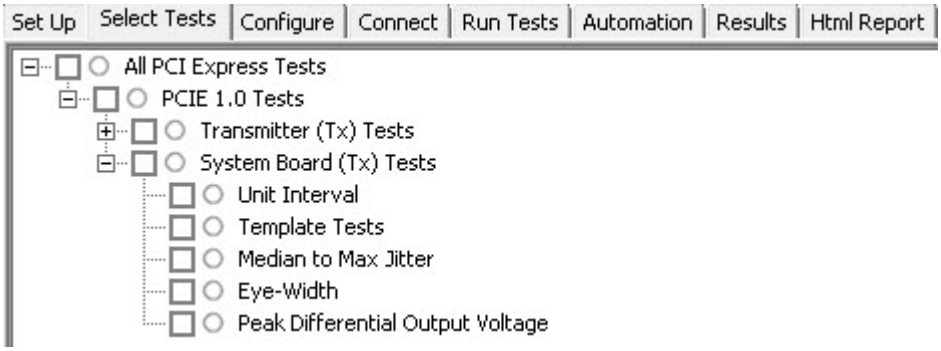


Figure 46 Selecting System Board (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 28 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running System Board Tests" on page 115 and select **Unit Interval**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `399.88ps < UI < 400.12ps`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

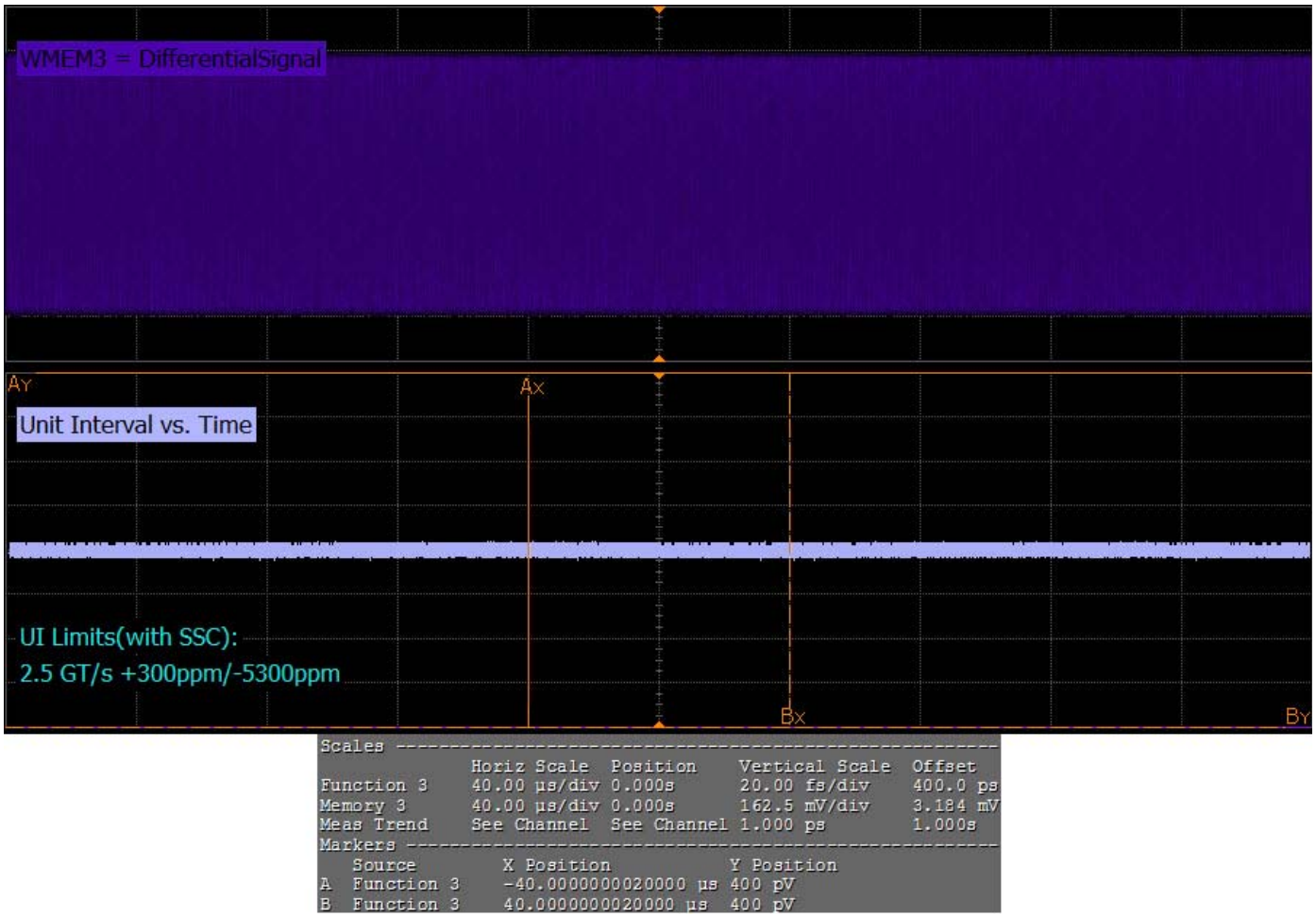


Figure 47 Reference Image for Unit Interval Test

Template Test

System boards must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 1.0a, Section 4.7.3, Table 4-8 as measured after the connector with an ideal load.

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.3 is used as reference to check the compliance of the DUT.

Table 29 Template Test Details

Symbol	Value
Vtx_S	>=274 mV
Vtx_{S_d}	>= 253 mV
Ttx_S	>=183 ps

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (T_{txS_d}).
- The values in Table 4-8 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary of an add-in card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 91.5 ps away from the jitter median.

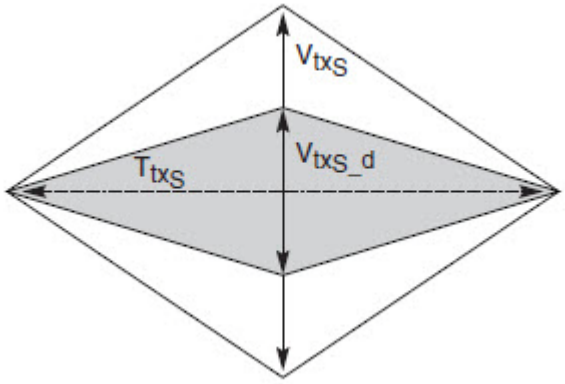


Figure 48 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running System Board Tests" on page 115 and select **Template Tests**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the system board compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the mean differential voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 1.0a and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

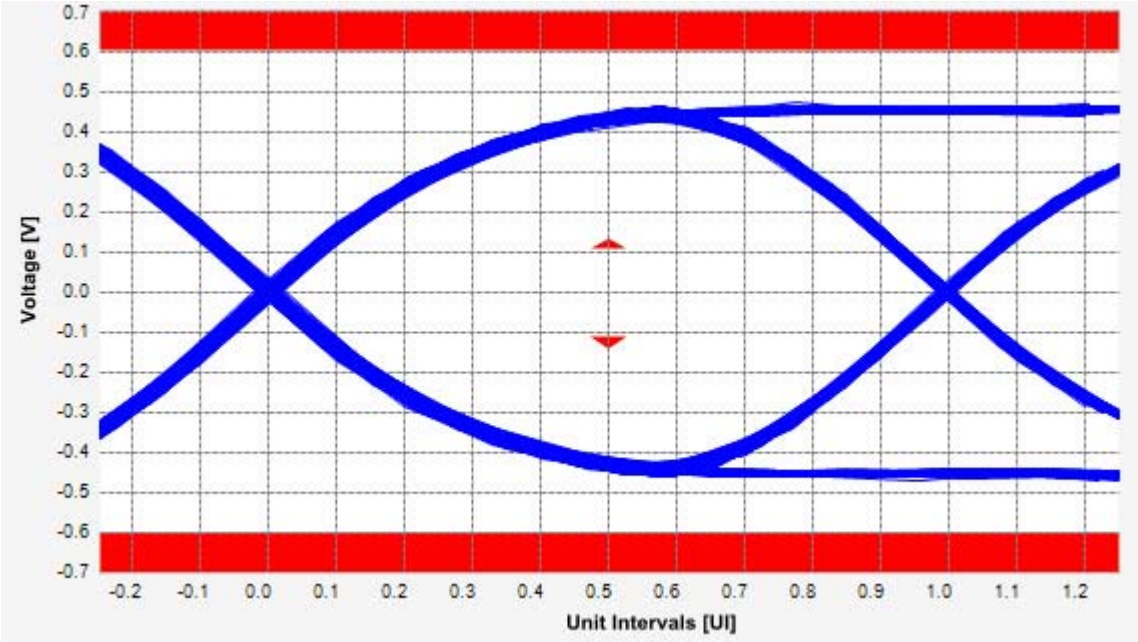


Figure 49 Reference Image for Template (Transition) Test

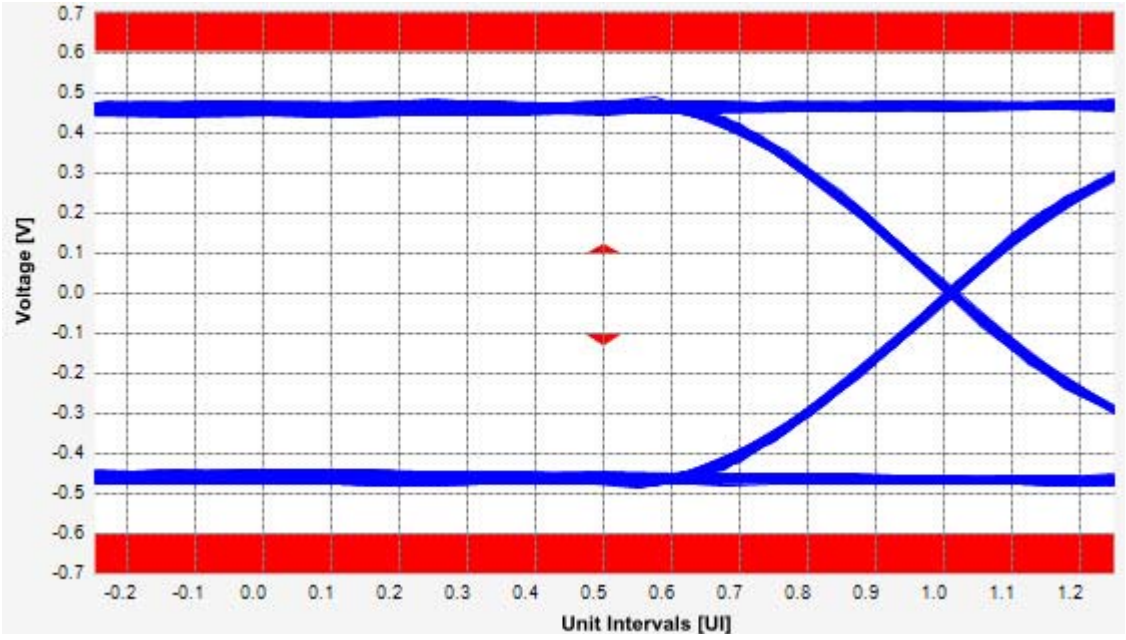


Figure 50 Reference Image for Template (Non-Transition) Test

Median to Max Jitter Test

Median to max jitter test measures the median to max jitter between the jitter median and max deviation from the median. The limit for the median to max jitter is calculated by the following equation:

$$\text{Median to max jitter} = (1\ UI - \text{Eye Width})/2$$

Where,

1 UI = 400ps

Eye Width = 183ps

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.3 is used as reference to check the compliance of the DUT.

Table 30 Median to Max Jitter Test Details

Symbol	Value
Vtx_S	>=274 mV
Vtx_S_d	>= 253 mV
Ttx_S	>=183 ps

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (T_{txS_d}).
- The values in Table 4-8 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary of an add-in card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 91.5 ps away from the jitter median.

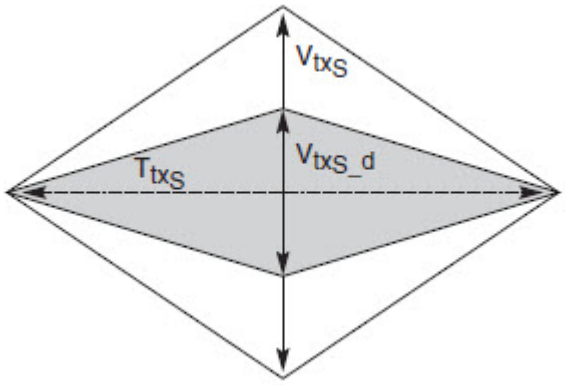


Figure 51 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 115 and select **Median to Max Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTestWrapper.dll file.

2 Computes the median to max jitter using the following formula:

Median to max jitter = Maximum peak to peak jitter after filter / 2

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 1.0a as 108.5ps.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is

captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER-12]$$

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.3 is used as reference to check the compliance of the DUT.

Table 31 Eye Width Test Details

Symbol	Value
Vtx_S	>=274 mV
Vtx_S_d	>= 253 mV
Ttx_S	>=183 ps

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (T_{txS_d}).
- The values in Table 4-8 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary of an add-in card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 91.5 ps away from the jitter median.

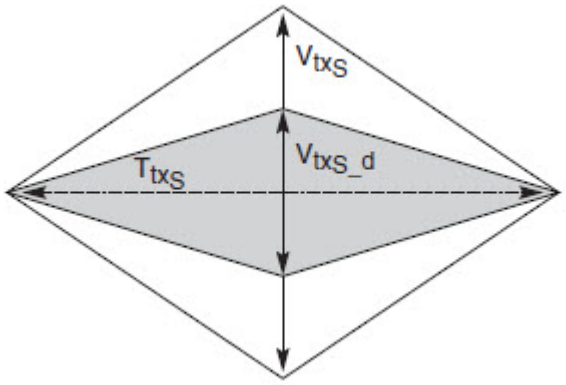


Figure 52 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 115 and select **Eye Width**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 1.0a.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits as T_{txA} >183ps.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to

view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),M(axin)(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.3 is used as reference to check the compliance of the DUT.

Table 32 Peak Differential Output Voltage Test Details

Symbol	Value
Vtx_S	>=274 mV
Vtx_S_d	>= 253 mV
Ttx_S	>=183 ps

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (T_{txS_d}).
- The values in Table 4-8 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary of an add-in card when mated with a connector. The eye diagram is defined and centered with respect to the jitter median. The jitter median should be calculated across any 250 consecutive UIs. The maximum jitter outlier should be no greater than 91.5 ps away from the jitter median.

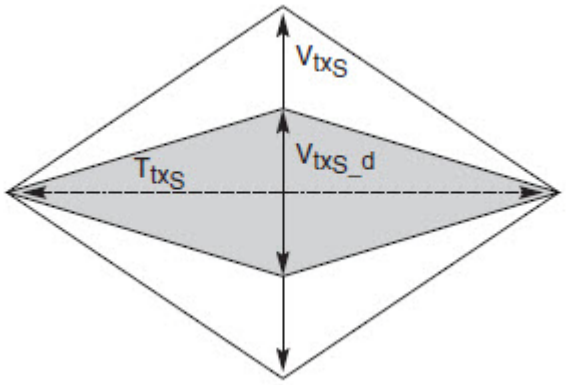


Figure 53 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 115 and select **Peak Differential Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 2.5GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

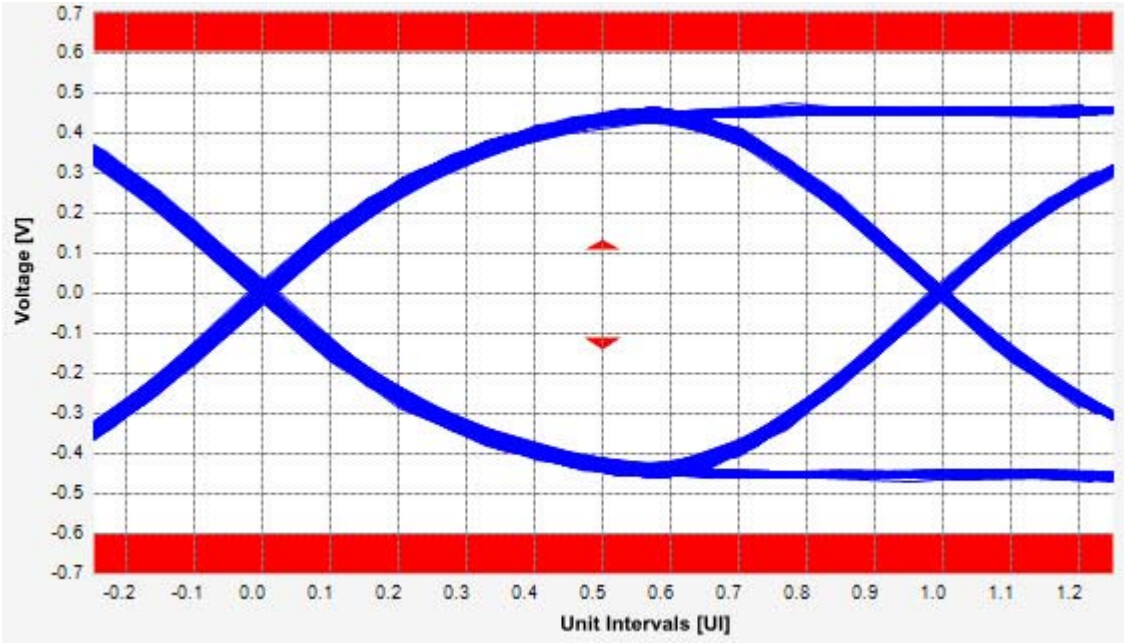


Figure 54 Reference Image for Peak Differential Output Voltage Test

Part III
PCI Express Version 1.1

Agilent Technologies

Part III

8 Transmitter (Tx) Tests, PCI-E 1.1, Full Power

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Tx Compliance

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Base Specification) will be transmitted.

Table 33 Probing Options for Transmitter Testing

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended SMA Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

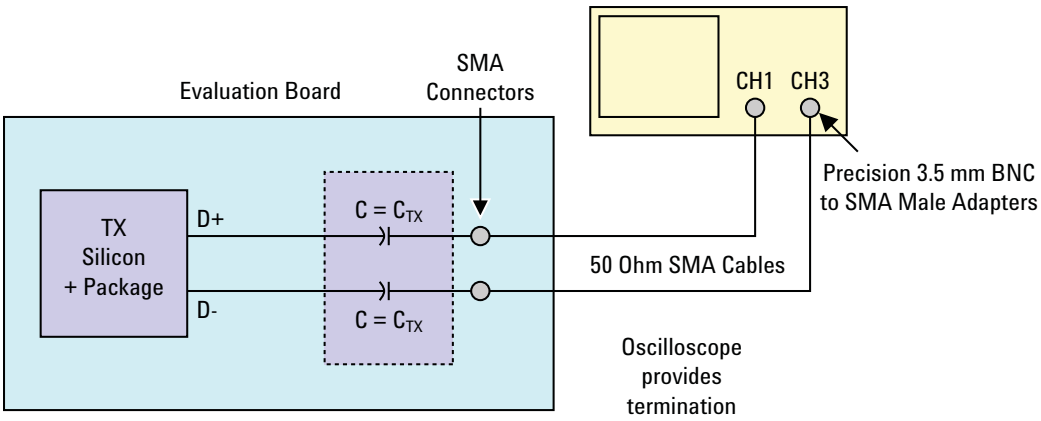


Figure 55 Single-Ended SMA Probing

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

Place single-ended grounds as close to the signal line’s reference ground as possible.

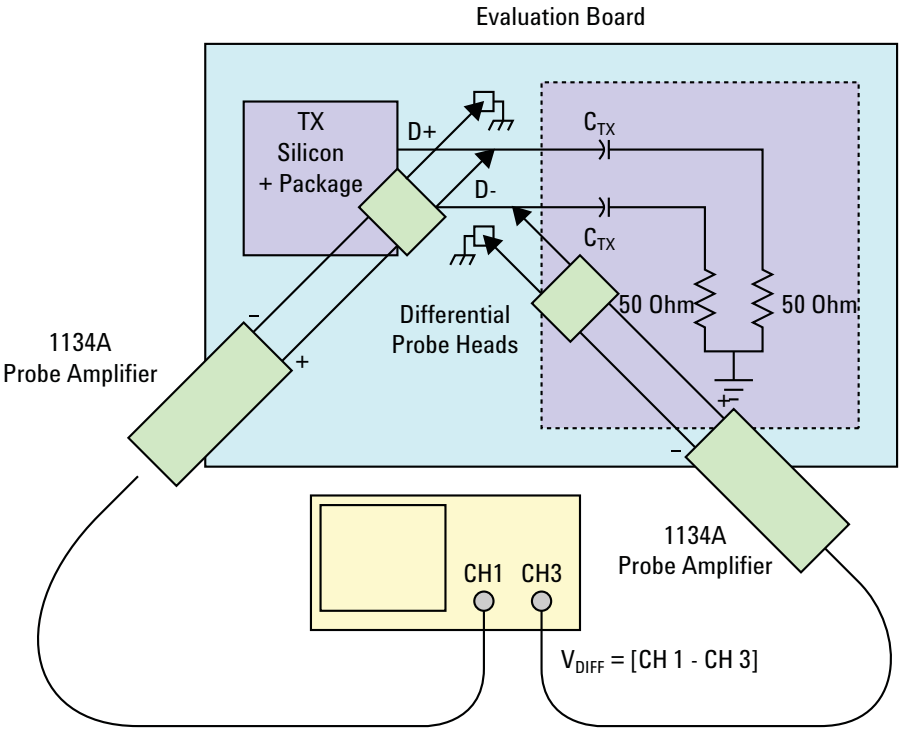


Figure 56 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

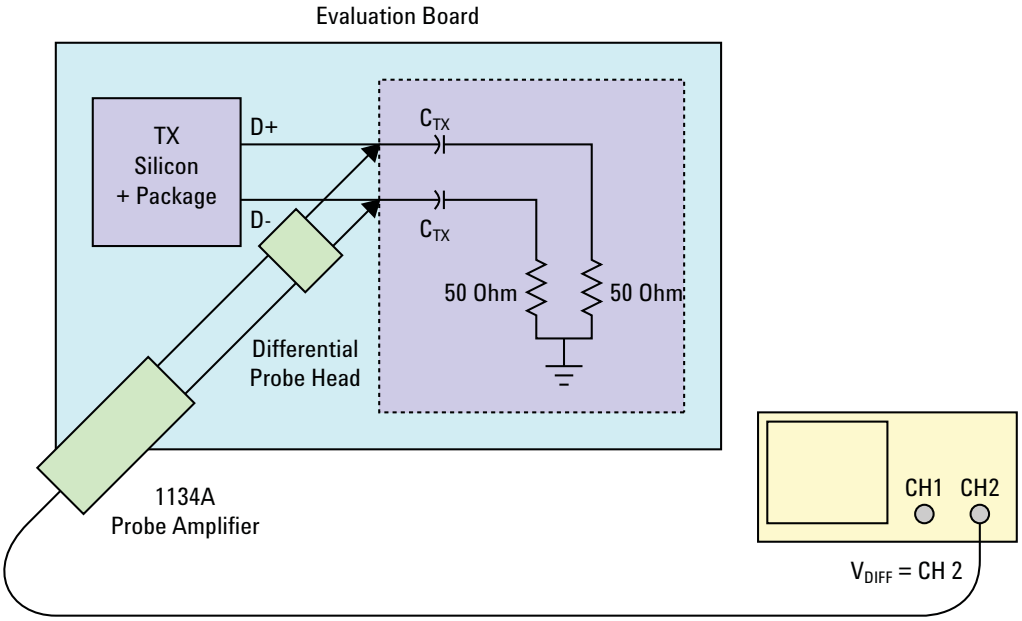


Figure 57 Differential Probing

Tx Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification)

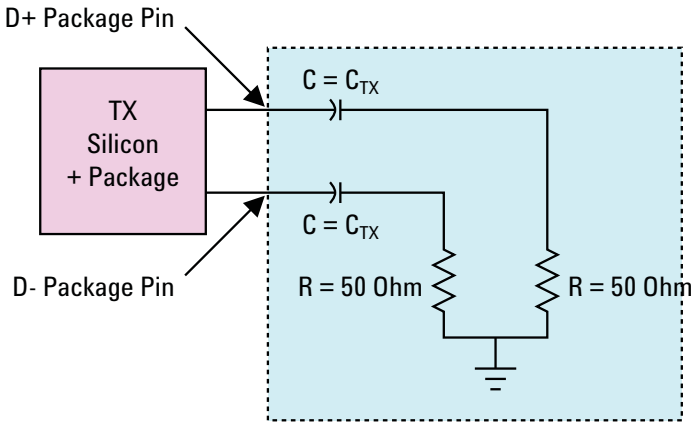


Figure 58 Driver Compliance Test Load.

Running Signal Quality Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to "Signal Quality" in the "Transmitter (Tx) Tests" group.

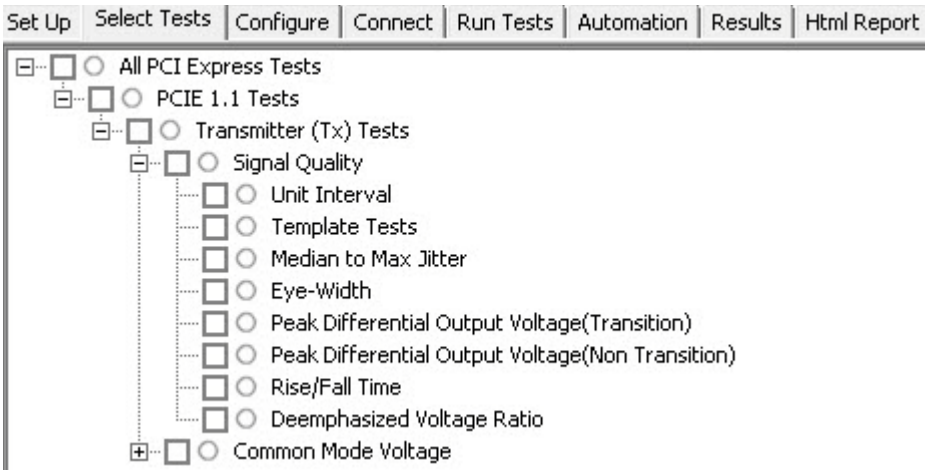


Figure 59 Selecting Transmitter (T_x) Signal Quality Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 34 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Signal Quality Tests" on page 136 and select **Unit Interval**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `399.88ps < UI < 400.12ps`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

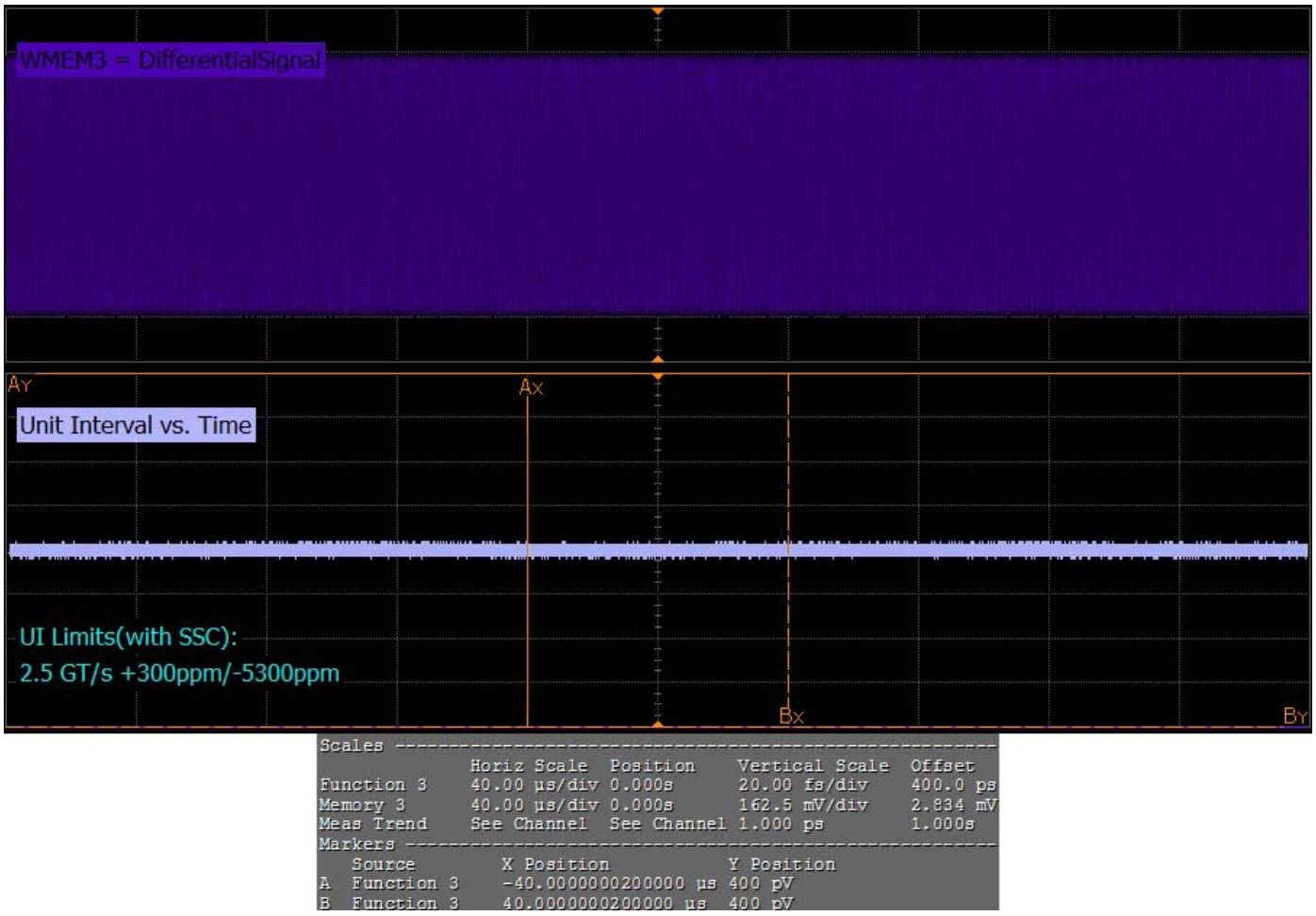


Figure 60 Reference Image for Unit Interval Test

Template Test

All PCIE devices must meet the transmitter eye diagram as specified in the PCI Express Base Specification, Rev 2.0.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 35 Template Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p T_x voltage swing	0.8V	1.2V

Test Definition Notes from the Specification

- The differential p-p Tx voltage swing parameter is defined as $2^*|V_{TXD+}-V_{TXD-}|$ as measured with the compliance test load.
- All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level.

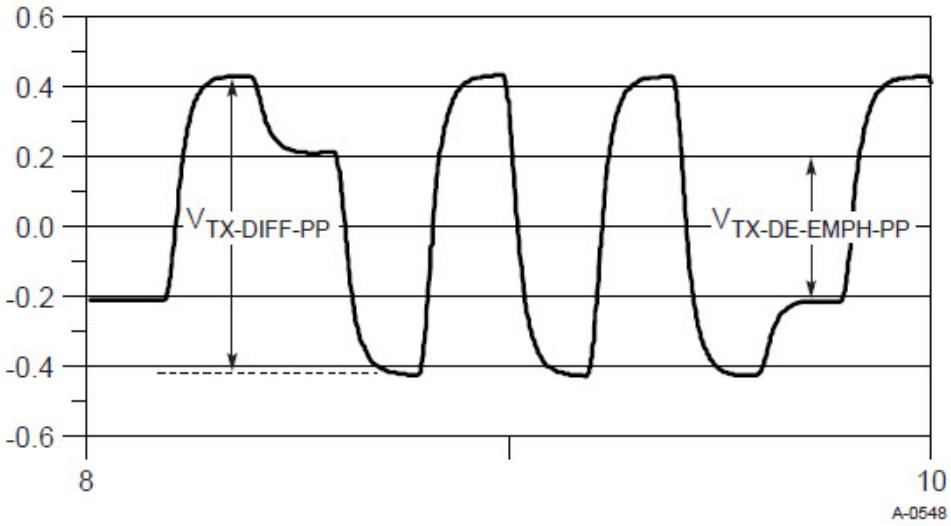


Figure 61 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Signal Quality Tests" on page 136 and select **Template Tests**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the transmitter compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the mean differential p-p T_x voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $0.8V < V_{TX-DIFF-PP} < 1.2V$ and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

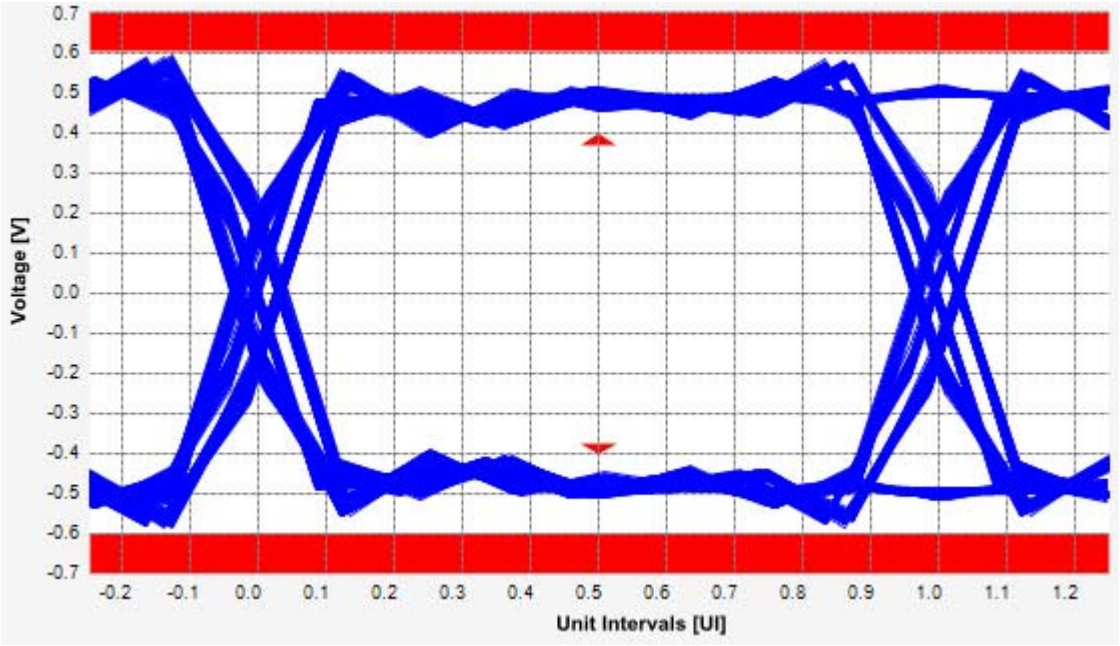


Figure 62 Reference Image for Template (Transition) Test

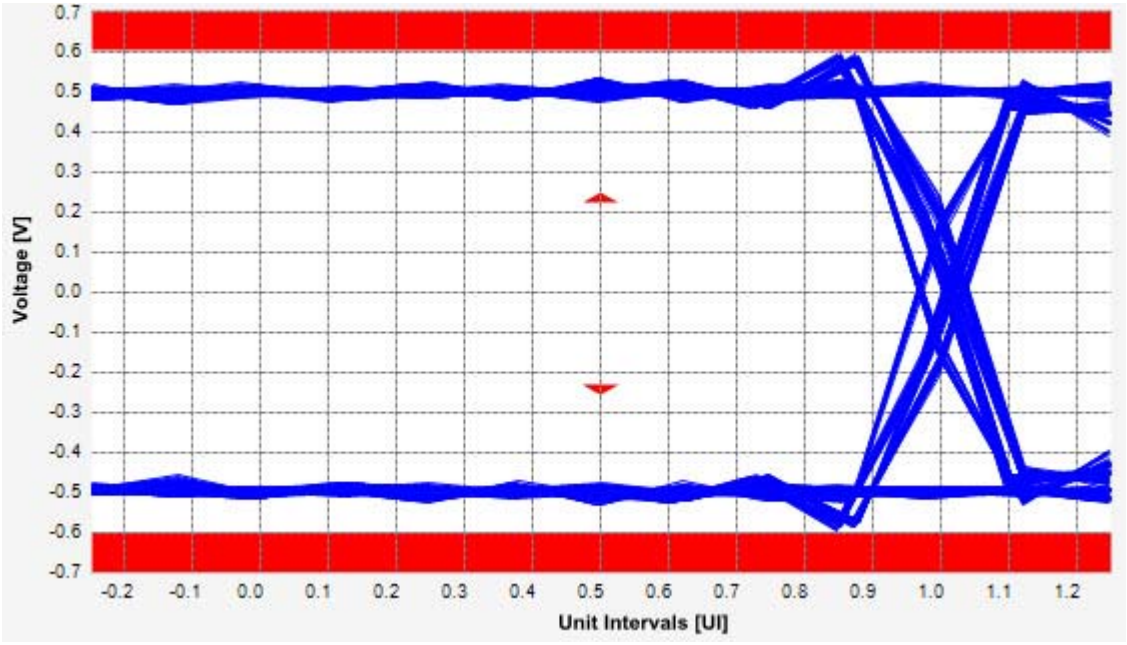


Figure 63 Reference Image for Template (Non-transition) Test

Median to Max Jitter Test

Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to the recovered T_X UI. The purpose of this test is to measure the median to max jitter between the jitter median and max deviation from the median.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 36 Median to Max Jitter Test Details

Symbol	Parameter	Max
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	0.125 UI

Test Definition Notes from the Specification

- This parameter is measured differentially at zero crossing points on a 2.5GT/s clock recovery function.
- Measurements at 5.0GT/s require an oscilloscope with a bandwidth of >= 12.5 GHz, or equivalent, while measurements made at 2.5GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5GT/s may be measured within 200mils of Tx device's pins although deconvolution is recommended. For measurement setup details, refer to Figure 4-23 and Figure 4-24. At least 10^6 UI of data must be acquired.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Signal Quality Tests" on page 136 and select **Median to Max Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTestWrapper.dll file.

2 Computes the median to max jitter using the following formula:

Median to max jitter = Maximum peak to peak jitter after filter /2

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `0.125UI >` $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 37 Eye Width Test Details

Symbol	Parameter	Min	Comments
$T_{TX\text{-}EYE}$	Minimum T_X Eye Width	0.75 UI	This parameter includes Rj at 10^{-12} and excludes single source clock or reference clock jitter.

NOTE The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

Test Definition Notes from the Specification

- Measurements at 5.0GT/s require an oscilloscope with a bandwidth of >= 12.5 GHz, or equivalent, while measurements made at 2.5GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5GT/s may be measured within 200mils of Tx device's pins although deconvolution is recommended. For measurement setup details, refer to Figure 4-23 and Figure 4-24. At least 10^6 UI of data must be acquired.
- Transmitter jitter is measured by driving the Transmitter under test with a low jitter "ideal" clock and connecting the DUT to a reference load.
- Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5GT/s and 5.0GT/s use different filter functions that are defined in Figure 4-21. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.
- For 5.0GT/s, de-emphasis timing jitter must be removed. An additional HPF function must be applied as shown in Figure 4-21. This parameter is measured by accumulating a record length of 10^6 UI while the DUT outputs a compliance pattern. $T_{MIN\text{-}PULSE}$ is defined to be nominally 1 UI wide and is bordered on both sides by pulses of the opposite polarity. Refer to Figure 4-29.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Signal Quality Tests" on page 136 and select **Eye Width**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express Base Specification, Rev 2.0 as $0.75\ UI < T_{TX-EYE}$.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 38 Peak Differential Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX-DIFF-PP}$	Differential p-p T_x Voltage Swing	0.80 V	1.2 V

Test Definition Notes from the Specification

As measured with compliance test load. Defined as $2^{*}|V_{TX\text{-}D+} - V_{TX\text{-}D-}|$

.

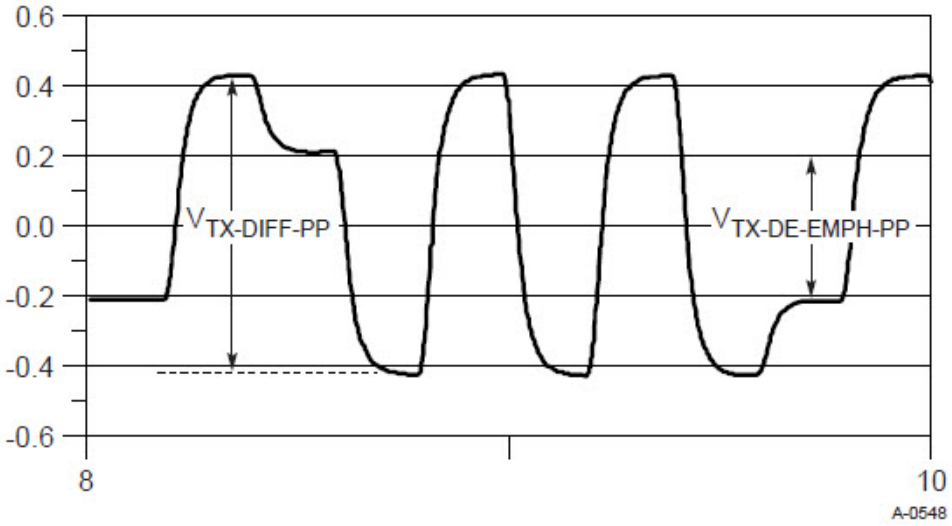


Figure 64 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Signal Quality Tests" on page 136 and select **Peak Differential Output Voltage (Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

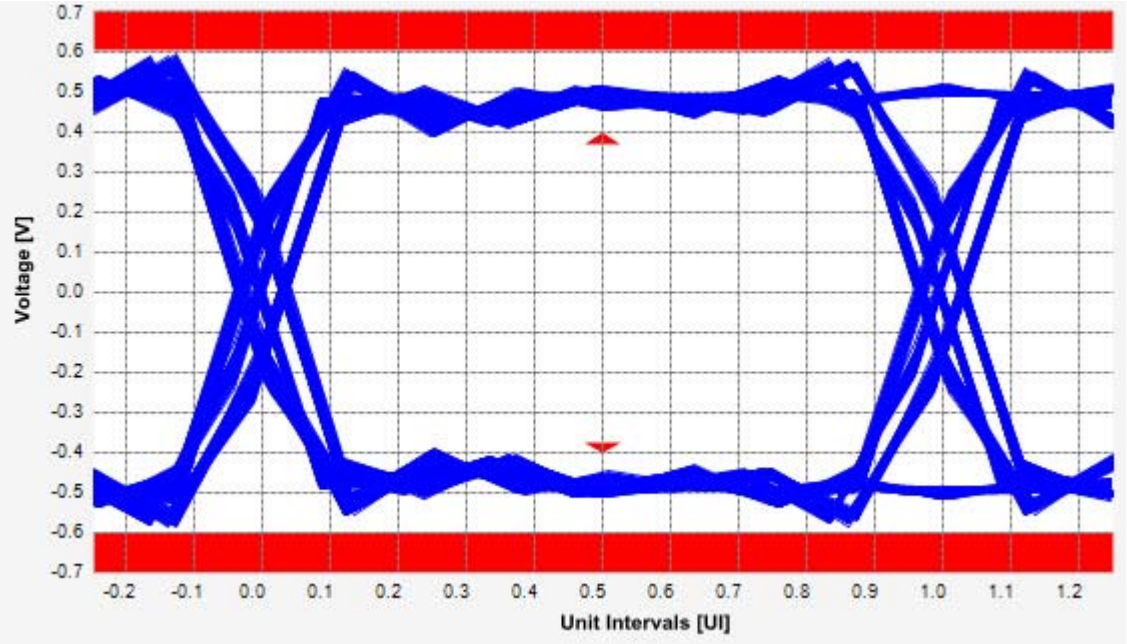


Figure 65 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 39 Peak Differential Output Voltage Test Details

Symbol	Parameter	Min	Max	Comments
$V_{TX-DIFF-PP}$	Differential p-p T_x Voltage Swing	0.80 V	1.2 V	The differential p-p T_x voltage swing parameter is defined as $2^*\lvert V_{TXD+} - V_{TXD-}\rvert$ as measured with the compliance test load.

Test Definition Notes from the Specification

$$V_{TX-DIFFp-p} = 2^*\lvert V_{TX-D+} - V_{TX-D-}\rvert$$

..

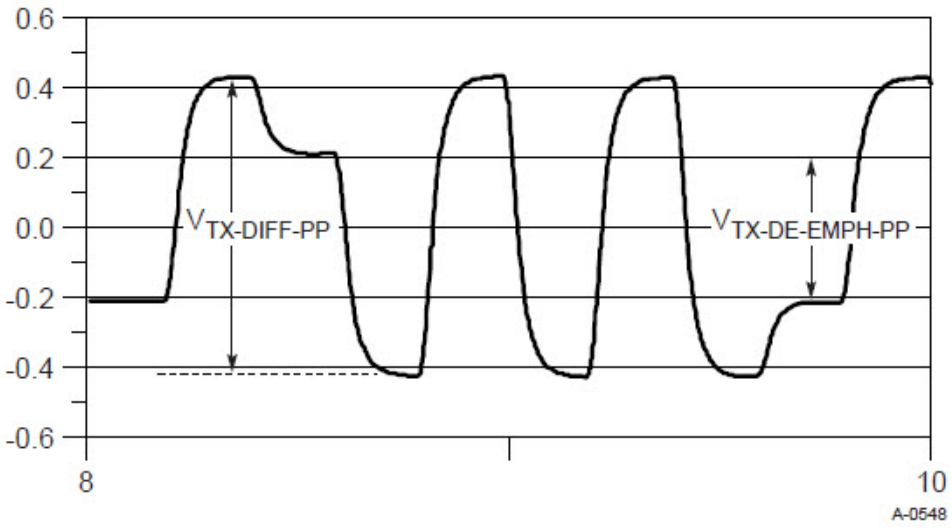


Figure 66 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Signal Quality Tests" on page 136 and select **Peak Differential Output Voltage (Non Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (non transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

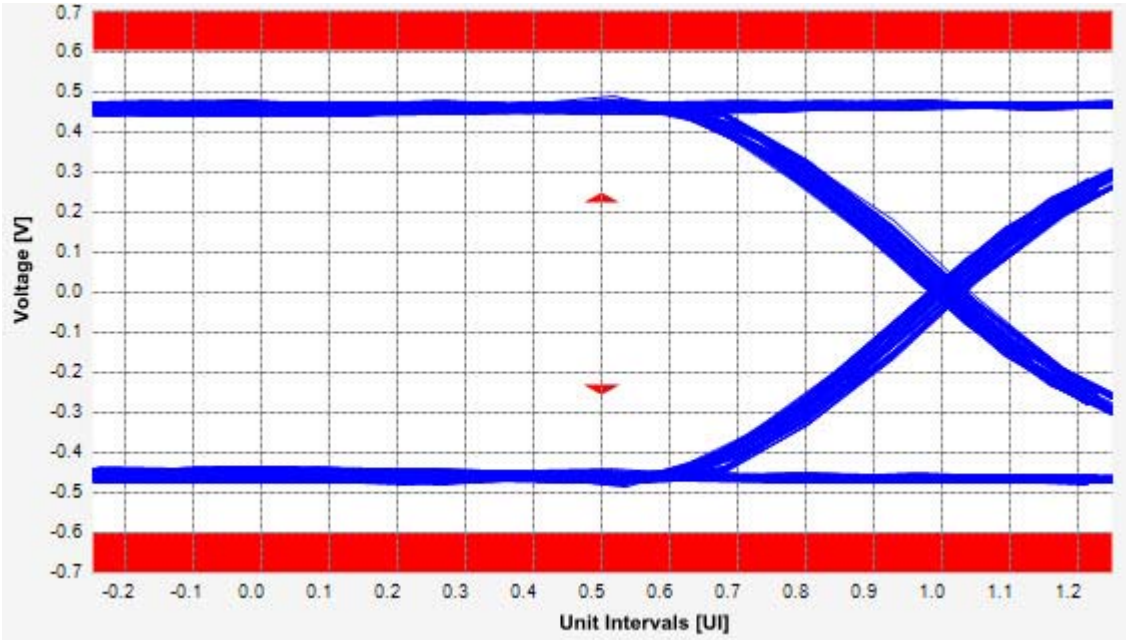


Figure 67 Reference Image for Peak Differential Output Voltage (Non-transition) Test

Rise/Fall Time Test

Rise/Fall time is taken independently on each single ended waveform source when you use two single ended probes or two SMA cables as the signal source. Differential signal rise/fall time shows up when you select differential probe type measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform.

Rise Time. This measurement is the time difference of the values observed when the V_{REF-HI} and the V_{REF-LO} reference level are crossed on the rising edge of the waveform.

$$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$$

Where:

't_{RISE}' is a rise time measurement.

't_{HI+}' is a set of t_{HI} for rising edges only.

't_{LO+} is a set of t_{LO} for rising edges only.

'i' and 'j' are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}.

'n' is the index of rising edges in the waveform.

Rise time for $v_{D+}(t)$ is as follows:

$$t_{D+RISE}(n) = t_{D+HI+}(i) - t_{D+LO+}(j)$$

and for $v_{D-}(t)$:

$$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$$

Fall Time. This measurement is the time difference of the values observed when the V_{REF-HI} and the V_{REF-LO} reference level are crossed on the falling edge of the waveform.

$$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$$

Where:

't_{FALL}' is a fall time measurement.

't_{HI-}' is set of t_{HI} for falling edge only.

't_{LO-}' is set of t_{LO} for falling edge only.

'i' and j' are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

'n' is the index of falling edges in the waveform.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 40 Rise/Fall Time Test Details

Symbol	Parameter	Min	Comments
$T_{TX\text{-}RISE\text{-}FALL}$	Transmitter rise and fall time	0.125 UI	This parameter is measured differentially from 20% to 80% of the swing.

NOTE The rise/fall time test is limited to only rising or falling edges of the consecutive transitions for transmitter measurements (TF2 and TR2 as shown in Figure 4-28). TF1 and TR1 are not covered in the current test procedure.

Test Definition Notes from the Specification

Measurements at 5.0GT/s require an oscilloscope with a bandwidth of >= 12.5 GHz, or equivalent, while measurements made at 2.5GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5GT/s may be measured within 200mils of Tx device's pins although deconvolution is recommended. For measurement setup details, refer to Figure 4-23 and Figure 4-24. At least 10^6 UI of data must be acquired.

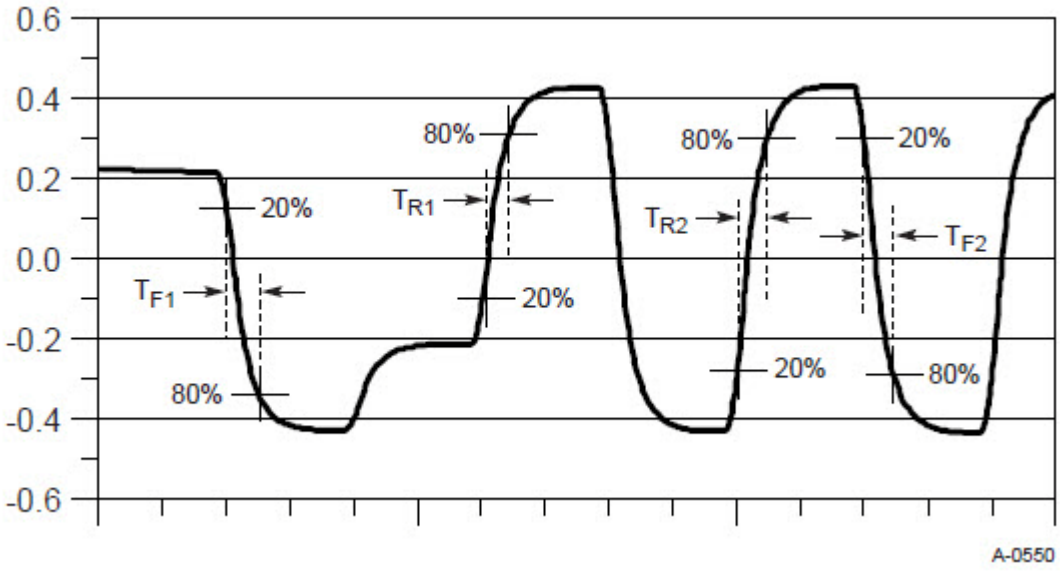


Figure 68 Rise and Fall Time Definition

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Signal Quality Tests" on page 136 and select **Rise/Fall Time**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   a. Sets the value of **Clock Recovery Method** as **First Order PLL**.
   b. Sets the value of **Nominal Data Rate** as **2.500000000Gb/s**.
   c. Sets the value of **Loop Bandwidth** as **1.500MHz**.
3. Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.
4. Measures the non - transition bits eye top and base.
5. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
6. Measures the transition bits eye top and base.
7. Configures **Thresholds** using **Measurement Analysis (EZJIT)** as follows:
   a. Sets **Thresholds** as **20%,50%,80% of Top, Base**.
   b. Defines **Top/Base** values using the previously measured eye top and base as **Histogram**.
8. If the **Transition Time Threshold** is configured as **Variable** using Automated Test Engine, then:
   a. Configures the value for time range to 50ps and time position to 180ps.
   b. Measures the fall time de-emphasis bits.
   c. Measures the rise time de-emphasis bits.
   d. Measures the fall time transition bits.
   e. Measures the rise time transition bits.
   f. Reports the maximum and minimum value for rise and fall time.
   g. Reports the worst value as actual result.

9 Finds the minimum value from the minimum rise time and the minimum fall time. Compares the obtained value with the value as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $0.125\ UI < T_{TX\text{-}RISE}, T_{TX\text{-}FALL}$.

10 Reports the worst case measured rise/fall time value as the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Figure 69 Reference Image for Rise/Fall Time Test

Deemphasized Voltage Ratio Test

Deemphasized voltage ratio is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 41 Deemphasized Voltage Ratio Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0 dB	-4.0 dB

Test Definition Notes from the Specification

Root complex Tx de-emphasis is configured from Upstream controller. Downstream Tx de-emphasis is set via a command, issued at 2.5GT/s. For details, refer to the appropriate location in Section 4.2.

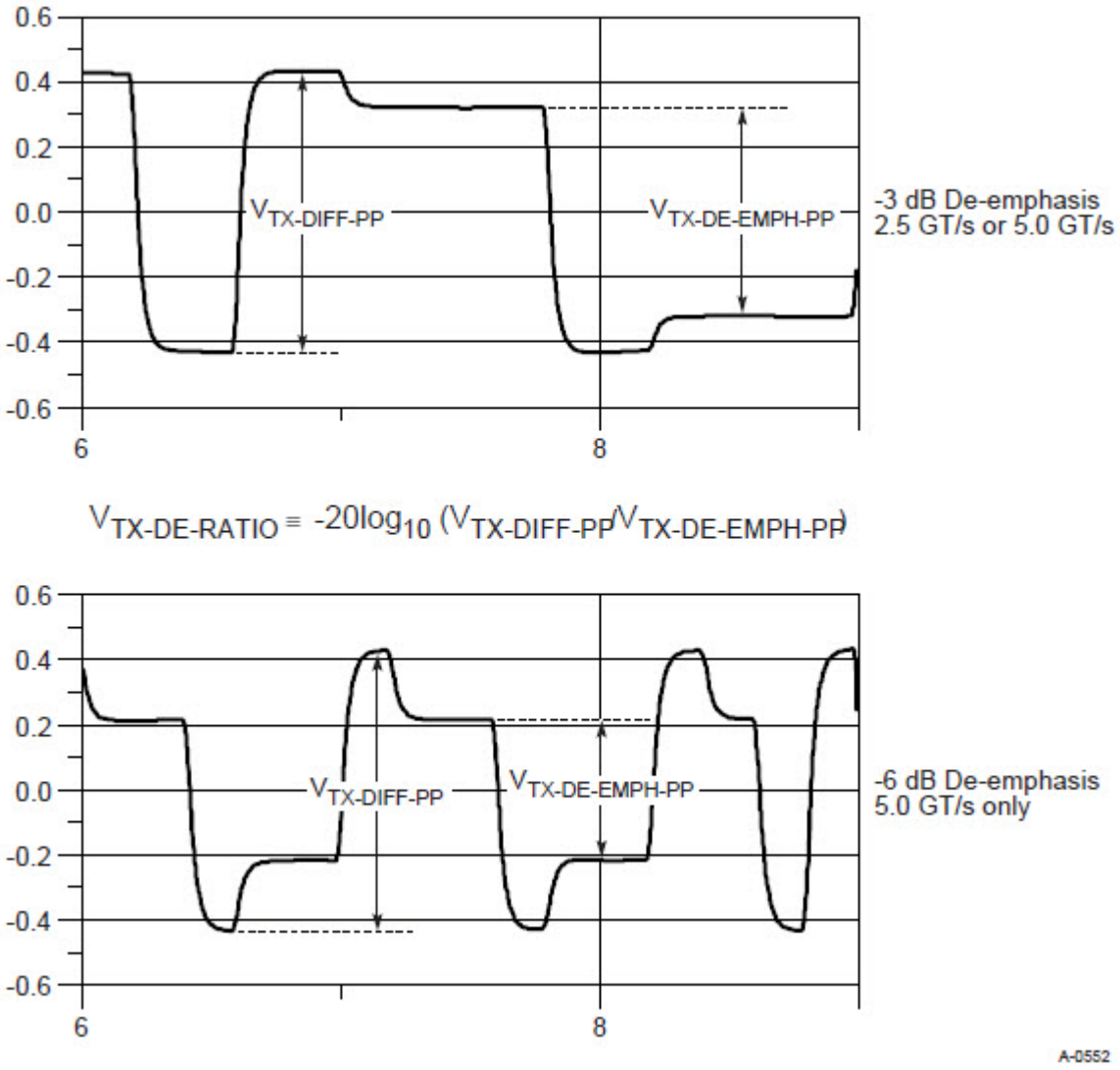


Figure 70 De-emphasized Voltage Ratio

Understanding the Test Flow

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Signal Quality Tests" on page 136 and select **Deemphasized Voltage Ratio**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:

   a Sets the value of **Clock Recovery Method** as **First Order PLL**.

   b Sets the value of **Nominal Data Rate** as **5.000000000Gb/s**.

   c Sets the value of **Loop Bandwidth** as **1.500MHz**.

3 Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.

4 Measures the non-transition bits eye top and base.

5 Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.

6 Measures the transition bits eye top and bases.

7 Finds the differential value between the transition bits eye top and base as $V_{TX\text{-}DIFF\text{-}PP}$ using **Histogram**.

8 Finds the differential value between the non-transition bits eye top and base as $V_{TX\text{-}DE\text{-}EMPH\text{-}PP}$ using **Histogram**.

9 Calculates de-emphasis ratio using the following formula:

$$\text{De-emphasis ratio} = -20*\log 10(V_{TX-DIFF-PP}/V_{TX-DE-EMPH-PP})$$

10 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $-4.0\ \text{dB} < V_{TX\text{-}DE\text{-}RATIO} < -3.0\ \text{dB}$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Running Common Mode Voltage Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to “Common Mode Voltage” in the “Transmitter (T_X) Tests” group.

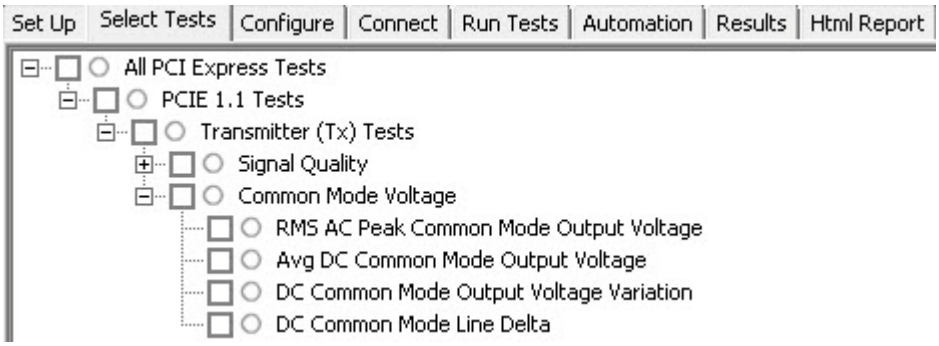


Figure 71 Selecting Transmitter (T_x) Common Mode Voltage Tests

RMS AC Peak Common Mode Output Voltage Test

The **RMS AC Peak Common Mode Output Voltage** is computed as:

$$V_{TX\text{-}AC\text{-}CM\text{-}p} = RMS[(V_{D+} + V_{D-})/2 - DC_{AVG}(V_{D+} + V_{D-})/2]$$

It is specified at the measurement point into a timing and voltage compliance test load and measured over any 250 consecutive T_X UIs.

NOTE This test is only available when the single-ended or SMA probing method has been used (see "Probing the Link for Tx Compliance" on page 132).

The AC common mode RMS voltage measurement calculates the RMS statistic of the common mode voltage waveform with the DC Value removed.

$$v_{AC\text{-}RMS\text{-}CM}(i) = RMS\ (v_{AC\text{-}M}(i))$$

where:

'i' is the index of all waveform values.

'$v_{AC\text{-}RMS\text{-}CM}$' is the RMS of the AC common mode voltage signal.

'$v_{AC\text{-}M}$' is the AC common mode voltage signal.

Test Reference

PCI Express Base Specification, Rev 1.1, Section 4.3.3., Table 4-5 is used as reference to check the compliance of the DUT.

Table 42 RMS AC Peak Common Mode Output Voltage Test Details

Symbol	Parameter	Max
$V_{TX\text{-}CM\text{-}ACp}$	RMS AC Peak Common Mode Output Voltage	20 mV

Test Definition Notes from the Specification

$V_{TX\text{-}AC\text{-}CM\text{-}PP}$ and $V_{TX\text{-}AC\text{-}CM\text{-}P}$ are defined in Section 4.3.3.7. Measurement is made over at least 10^6 UI.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. Follow the procedure in "Running Common Mode Voltage Tests" on page 157 and select **RMS AC Peak Common Mode Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Sets up DC common mode voltage using **Math (FFT and more...)** as follows:
   a. Configures **Operator** as **Common Mode** measurements.
   b. Loads common mode signal.
   c. Measures the average of common mode using **V average** measurement from scope.
   d. Measures compliance test limit boundaries (0V to 3.6V) using **Markers**.
4. Measures **RMS Type** as **AC** and **Units** as **Volt** using **V rms Measurement**.
5. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $20\ mV > V_{TX\text{-}AC\text{-}CM\text{-}p}$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in

the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

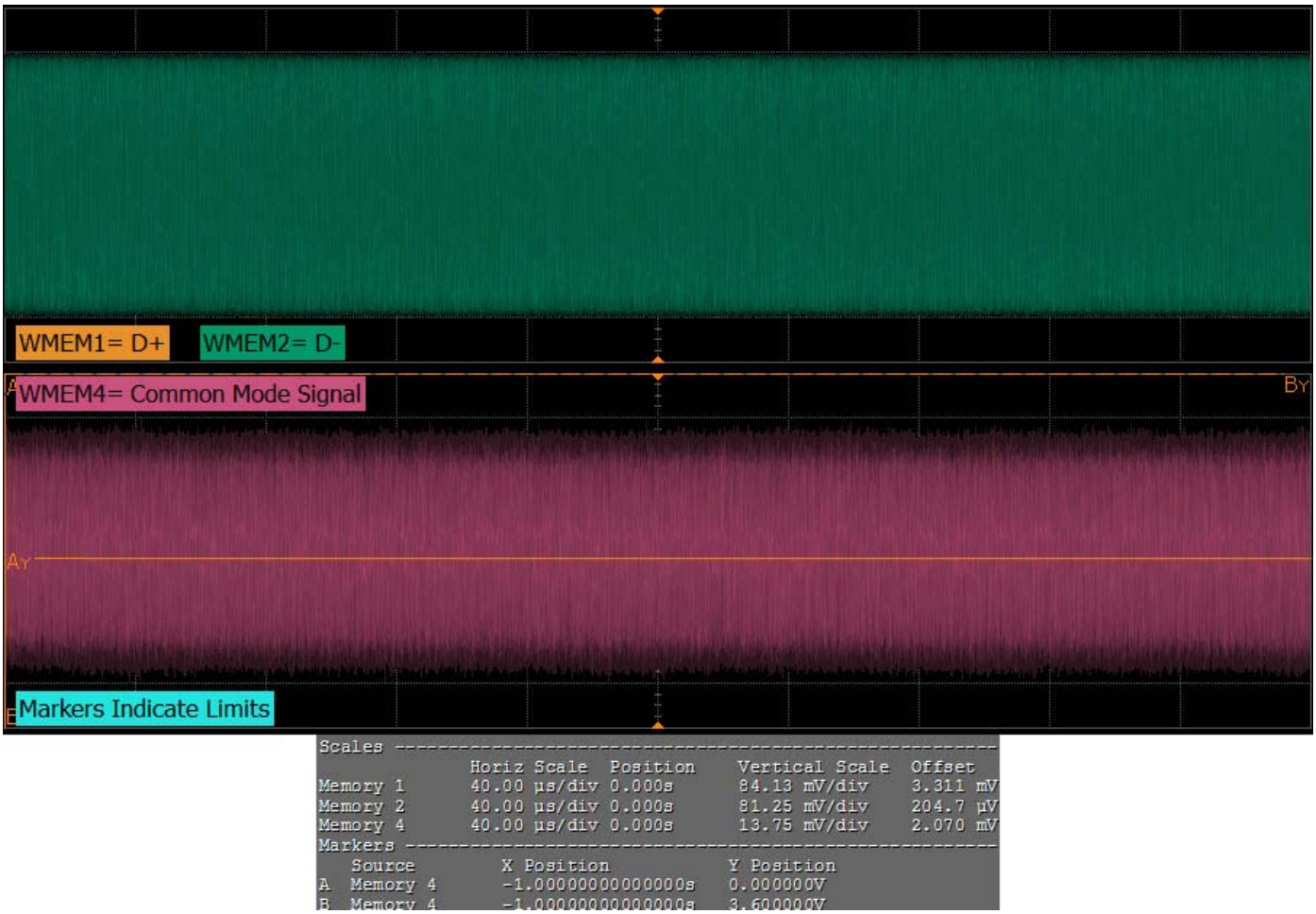


Figure 72 Reference Image for RMS AC Peak Common Mode Output Voltage Test

Avg DC Common Mode Output Voltage Test

The **Avg DC Common Mode Voltage** measurement computes the DC average of the common mode signal:

$$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)} \text{ of } |V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$$

The PCI Express Base Specification, Rev 2.0 states that the transmitter DC common mode voltage ($V_{TX\text{-}DC\text{-}CM}$) must be held at the same value during all states.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 43 Avg DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	The TX DC Common Mode Voltage	0 V	3.6 V

NOTE This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled. For more information, see "Probing the Link for Tx Compliance" on page 132.

Test Definition Notes from the Specification

The allowed DC common mode voltage at the Transmitter pins under any conditions.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Common Mode Voltage Tests" on page 157 and select **Avg DC Common Mode Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Sets up DC common mode voltage as follows:

   a Enables and displays common mode measurements.

   b Loads common mode signal to waveform memory.

   c Loads and enhance dynamic range D+ signal and D- signal.

   d Enables the average common mode measurement.

   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).

4 Measures the average value of D+ and D- signal.

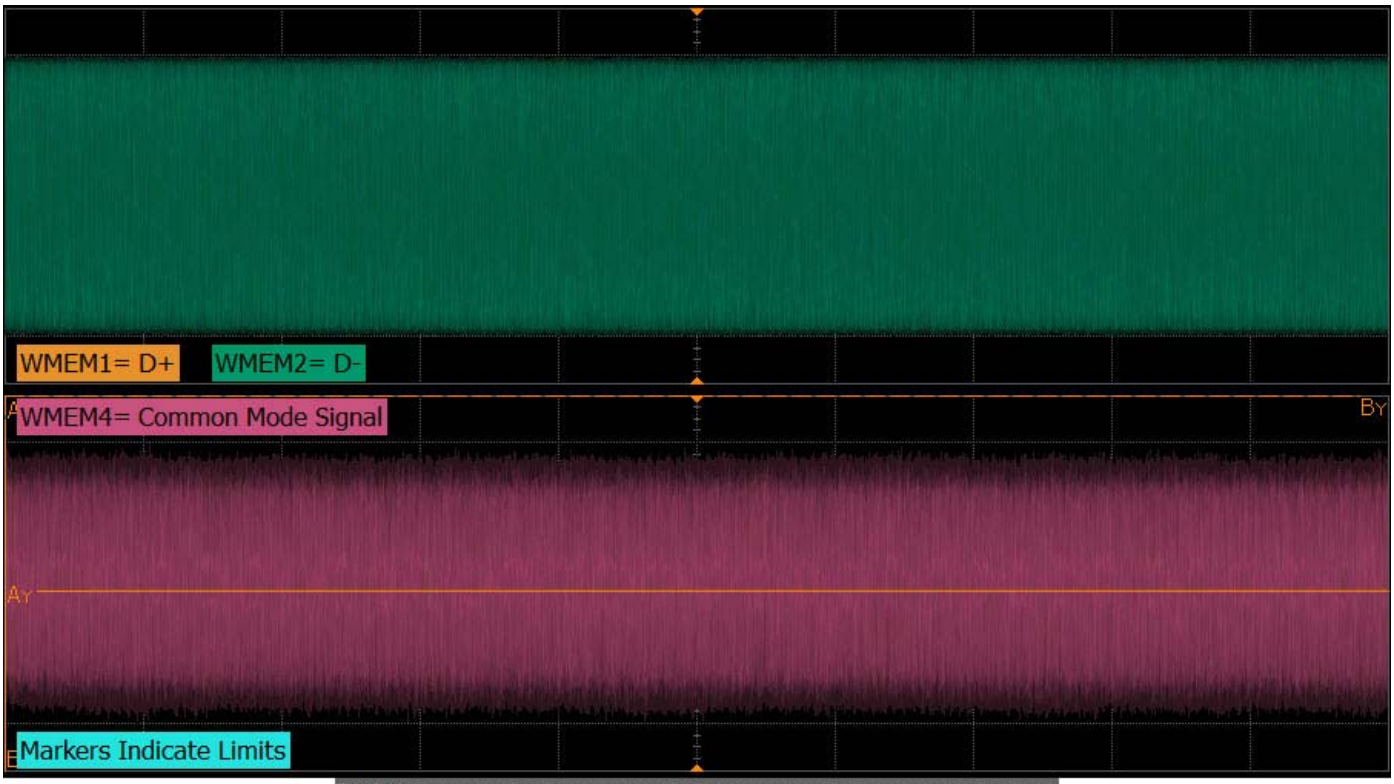
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to

view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	40.00 µs/div	0.000s	84.13 mV/div	3.311 mV
Memory 2	40.00 µs/div	0.000s	81.25 mV/div	204.7 µV
Memory 4	40.00 µs/div	0.000s	13.75 mV/div	2.071 mV

Markers

	Source	X Position	Y Position
A	Memory 4	-1.00000000000000s	0.000000V
B	Memory 4	-1.00000000000000s	3.600000V

Figure 73 Avg DC Common Mode Output Voltage Test

DC Common Mode Output Voltage Variation Test

The **DC Common Mode Voltage** ($V_{TX\text{-}DC\text{-}CM}$) must be held at the same value during all states. The allowable range for $V_{TX\text{-}DC\text{-}CM}$ is 0 to 3.6 V (+/- 100mV).

The T_X DC Common Mode Output Voltage Variation measurement computes the worst case positive or negative excursion of the common mode signal from the average DC Common Mode Voltage $V_{TX\text{-}DC\text{-}CM}$.

$$V_{TX\text{-}DC\text{-}CM\text{-}VARIATION} = |\text{Max}\ (\text{Max}\ (V_{CM(i)}), \text{Min}\ (V_{CM(i)})) - V_{TX\text{-}DC\text{-}CM}\ |$$

Where:

'i' is the index of all waveform values.

'V_{CM}' is the common mode signal ($V_{TX\text{-}D+}$ + $V_{TX\text{-}D\text{-}}$)/2.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 44 DC Common Mode Output Voltage Variation Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC common mode voltage	0 V	3.6V

Test Definition Notes from the Specification

The allowed DC common-mode voltage at the Transmitter pins under any conditions.

NOTE This test is only available when the single-ended or SMA probing method has been used (see "Probing the Link for Tx Compliance" on page 132).

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Common Mode Voltage Tests" on page 157 and select **DC Common Mode Output Voltage Variation**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Avg DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the average DC common mode output voltage test:
   - **a** Maximum common mode value
   - **b** Minimum common mode value

2 Finds the worst value between maximum common mode value and minimum common mode value.

3 Computes the DC common mode line delta by absolute the difference between average DC value of D+ and average DC value of D-.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $0<=|V_{TX\text{-}DC\text{-}CM\text{-}VARIATION}|<=100\ mV$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common Mode Line Delta Test

The **DC Common Mode Line Delta** computes the absolute difference between the average value of the D+ and the D- waveforms signals.

$$|V_{TX\text{-}CM\text{-}DC\text{-}D+\ [during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D-\ [during\ L0]}|<=25mV$$

Where,

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $V_{TX\text{-}D-}|$ [during L0]

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 45 DC Common Mode Line Delta Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0m V	25 mV

NOTE This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled. For more information, see "Probing the Link for Tx Compliance" on page 132).

Test Definition Notes from the Specification

$$|V_{TX\text{-}CM\text{-}DC\text{-}D+\ [during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D-\ [during\ L0]}| <= 25mV$$

Where,

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $V_{TX\text{-}D-}|$ [during L0]

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Common Mode Voltage Tests" on page 157 and select **DC Common Mode Line Delta**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the average DC common mode output voltage test.

1 Reports the following measurement results obtained from running the average DC common mode output voltage test:
   - **a** DC Common Mode Line Delta
   - **b** Average DC value of D+
   - **c** Average DC value of D-
2 Computes the DC common mode line delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $V_{TX\text{-}CM\text{-}LINE\text{-}DELTA} < 25mV$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

9 Transmitter (Tx) Tests, PCI-E 1.1, Low Power

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

The *Mobile Graphic Low Power Addendum to The PCIE Base Specification 1.0* is applicable to PCIE 1.1 as well.

PCIE 1.1 Low Power Transmitter Tests consist of all tests from PCIE 1.1 Full (Standard) Power Tests except de-emphasis tests. The following table shows all the PCIE 1.1 Low Power Tests:

Table 46 PCIE 1.1 Low Power Transmitter Tests

Test Name	Remarks	See
Unit Interval	Same as Full Power	page 137.
Template Tests	Different	page 139.
Median to Max Jitter	Different	page 143.
Eye-Width	Different	page 144.
Peak Differential Output Voltage	Different	page 146.
Rise/Fall Time	Same as Full Power	page 151.
RMS AC Peak Common Mode Output Voltage	Same as Full Power	page 158.
Avg DC Common Mode Output Voltage	Same as Full Power	page 160.
DC Common Mode Output Voltage Variation	Same as Full Power	page 163.
DC Common Mode Line Delta	Same as Full Power	page 165.

All the tests above remarked with “Same as Full Power” share the same Method of Implementation (MOI) with PCIE 1.1 Full Power (refer to the page numbers shown). The differences in the test method are described in this chapter.

Probing the Link for Tx Compliance

When performing low-power transmitter tests, probing is the same as for full-power tests. See “Probing the Link for Tx Compliance" on page 132.

Tx Compliance Test Load

When performing low-power transmitter tests, the compliance test load is the same as for full-power tests. See “Tx Compliance Test Load" on page 136.

Running Signal Quality Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to “Signal Quality” in the “Transmitter (Tx) Tests” group.

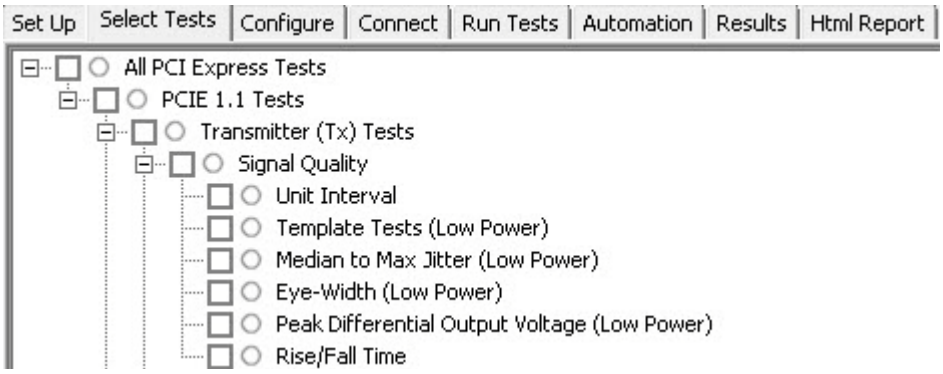


Figure 74 Selecting Transmitter (Tx) Signal Quality Tests

Unit Interval

When performing low-power transmitter tests, the Unit Interval test is the same as for full-power tests. See “Unit Interval Test" on page 137.

Template Tests (Low Power)

Test Definition/Reference

Mobile Graphics Low-Power Addendum to the PCI Express Base Specification 1.0

- Compliance of the transmitter eye diagram uses the same methodology as outlined in PCI Express Base 1.0a. The Tx eye diagram is specified using the passive compliance/test measurement load (see Figure 2-1 of Mobile Low Power PCIE Specification) in place of any real PCI Express interconnect plus Rx component. Because de-emphasis is not implemented, the transition and de-emphasized bit transitions are merged into a single Transmitter compliance eye diagram.
- The eye diagram must be valid for any 250 consecutive UIs.
- A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

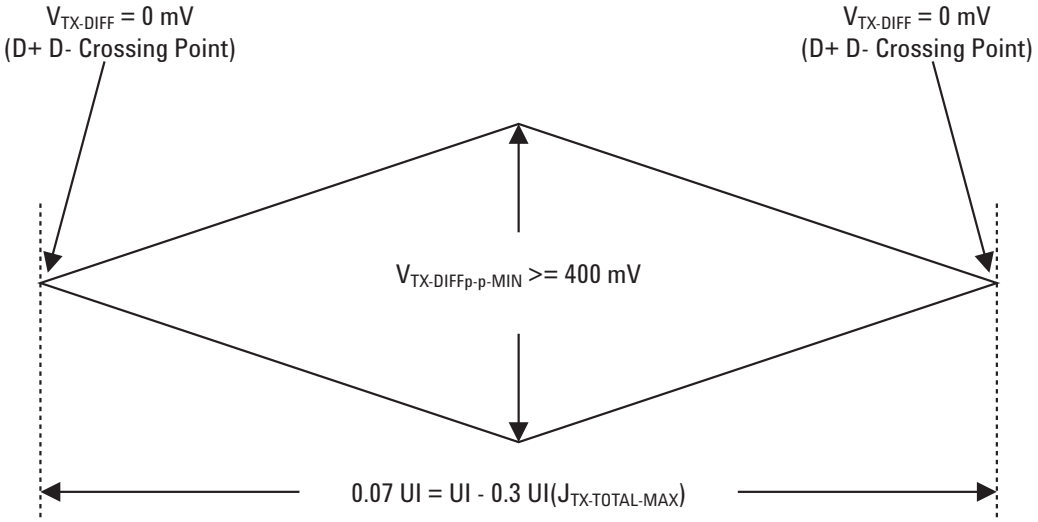


Figure 75 Transmitter Compliance Eye Diagram from Figure 2-2 of the Mobile Graphic Low-Power Addendum.

Difference in Test Procedure Compared to Full Power

- Different Eye diagram used. The Eye diagram can be found in Figure 2.2 of Mobile Low Power PCIE Specification.
- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Template Test" on page 139.

Median to Max Jitter (Low Power)

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Median to Max Jitter Test" on page 143.

Eye-Width (Low Power)

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also "Eye-Width Test" on page 144

Peak Differential Output Voltage (Low Power)

Difference in Test Procedure Compared to Full Power

- Different specification used:

Table 47 $V_{TX\text{-}DIFFp\text{-}p}$ from Table 2-1 of the Mobile Graphic Low-Power Addendum.

Symbol	Parameter	Min	Nom	Max
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Pk-Pk Output Voltage	0.400 V		1.2 V

- $V_{TX\text{-}DIFFp\text{-}p} = 2^{*}|V_{TX\text{-}D+} - V_{TX\text{-}D-}|$
- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 2-1 (Mobile Graphic Low Power Addemdum) and measured over any 250 consecutive TX UIs. Also refer to the Transmitter compliance eye diagram shown in Figure 2-2 (Mobile Graphic Low Power Addemdum).

See Also "Peak Differential Output Voltage (Transition) Test" on page 146.

Rise/Fall Time

When performing low-power transmitter tests, the Tx Rise/Fall Time test is the same as for full-power tests. See "Rise/Fall Time Test" on page 151.

Running Common Mode Voltage Tests

When performing low-power transmitter tests, the common mode voltage tests are the same as for full-power tests. See “Running Common Mode Voltage Tests" on page 157.

10
Receiver (Rx) Tests, PCI-E 1.1

This section provides the Methods of Implementation (MOIs) for Receiver tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

NOTE

None of the included receiver tests validate the receiver's ability to correctly receive data (also known as receiver tolerance). Rather, they validate that the signal as seen by the receiver meets or exceeds various parameters (maximum voltage, jitter, eye width, etc.). These tests validate the transmitter and interconnect. Separate receiver tolerance testing is required to ensure the receiver is correctly receiving data.

Probing the Link for Rx Compliance

Receiver tests are done by probing the link as close as is feasibly possible to the pins of the receiver device. Alternatively, a dummy load can be used for the termination of the link. To probe the receiver link, you can:

- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

Table 48 Probing Options for Receiver Testing

	Probing Configurations			Captured Waveforms	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**
DUT Connection	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

Channel-to-channel deskew is required using this technique because two channels are used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

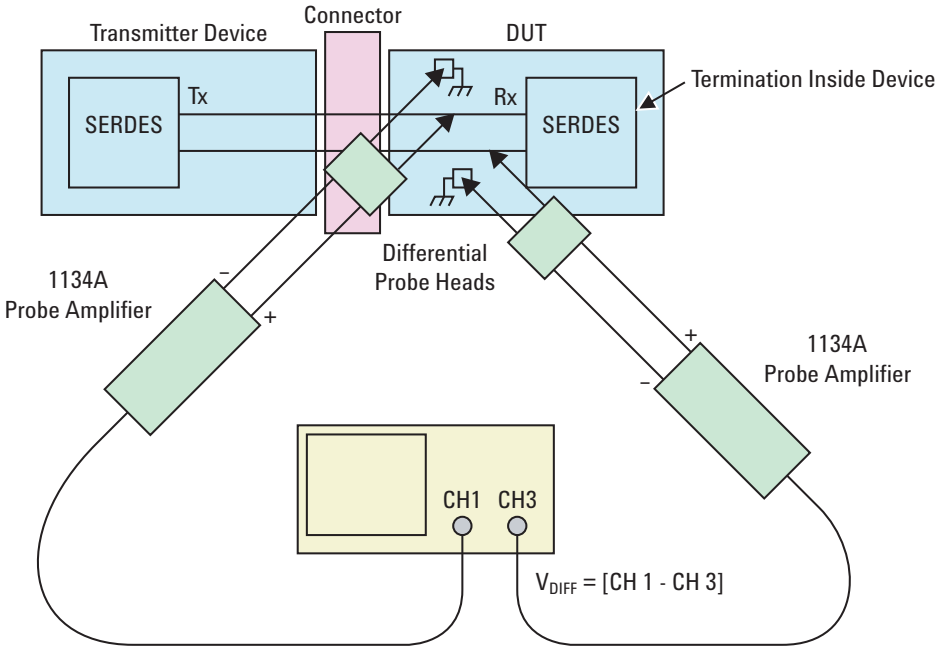


Figure 76 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

A single channel of the oscilloscope is used, so de-skew is not necessary.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

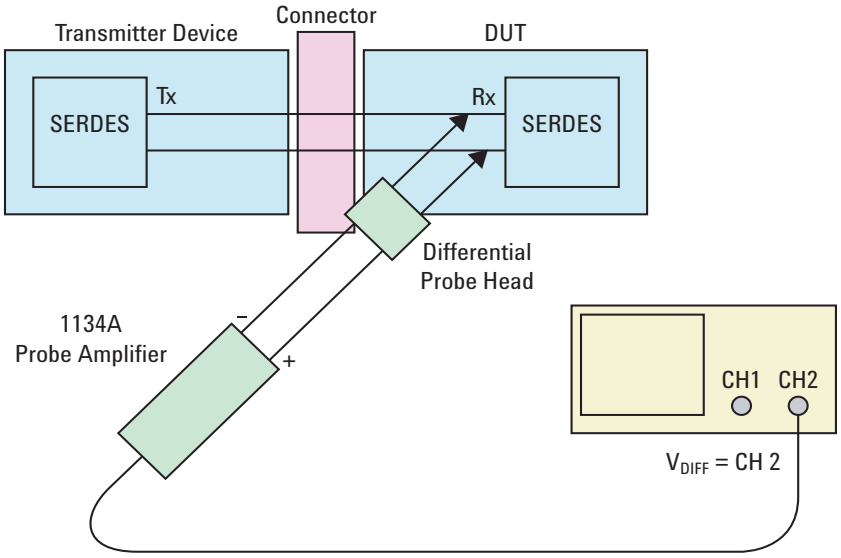


Figure 77 Differential Probing

Running Receiver Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "Receiver (Rx) Tests" group.

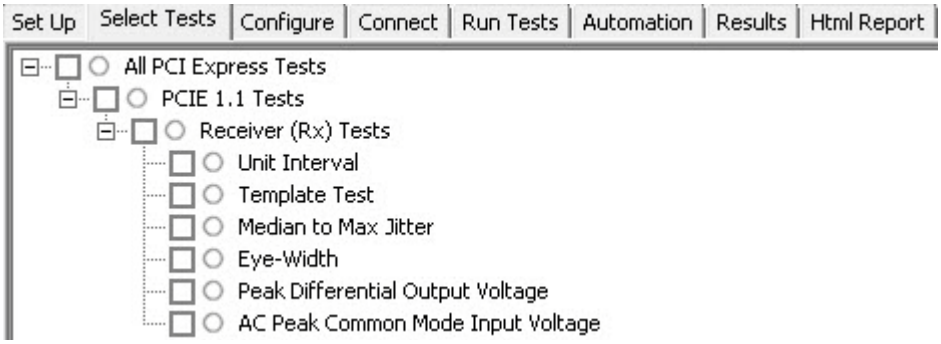


Figure 78 Selecting Receiver (Rx) Tests

Unit Interval Test

A recovered receiver unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$R_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The R_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another R_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case R_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 49 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- UI is specified to be +/-300 ppm.
- UI does not account for SSC dictated variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

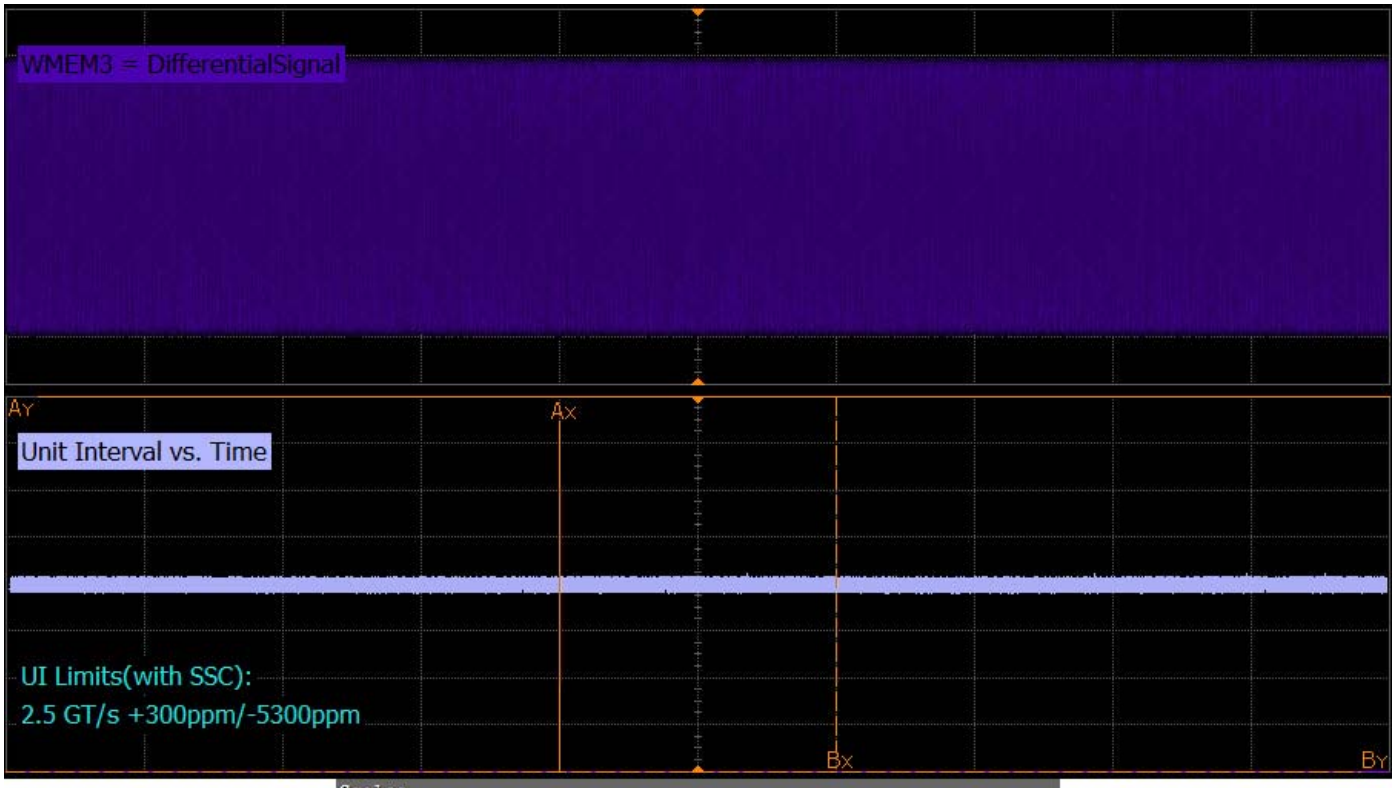
NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Receiver Tests" on page 177 and select **Unit Interval**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Fits and displays all sample data on screen.
3. Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a. Selects **Unit Interval** as data measurement analysis unit.
   b. Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.
4. Indicates the upper and lower limit of the measured data using markers.
5. Measures the minimum, mean and maximum values of the UI.
6. Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `399.88ps < UI < 400.12ps`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

NOTE The MOI for the measurement of UI at the receiver is identical to measuring it at the transmitter, with the exception of the test point. Refer to "Unit Interval Test" on page 137.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	40.00 µs/div	0.000s	20.00 fs/div	400.0 ps
Memory 3	40.00 µs/div	0.000s	162.5 mV/div	3.439 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-40.0000000200000 µs	400 pV
B	Function 3	40.0000000200000 µs	400 pV

Figure 79 Reference Image for Unit Interval Test

Template Test

A receiver must reliably receives all data that meets the differential receiver input specifications as shown in PCI Express Base Specification, rev 2.0. This test does not validate the receiver's tolerance.

All links are assumed active while generating the eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 50 Template Test Details

Symbol	Parameter	Min	Max
$V_{RX-DIFF-PP-CC}$	Differential R_x peak-peak voltage for common Refclk Rx architecture	0.175V	1.2V

Test Definition Notes from the Specification

- All links are assumed active while generating the eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level.
- For more information on the receiver parameter details, refer to Section 4.3.7.2.2 of the base specification.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Receiver Tests" on page 177 and select **Template Test**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the receiver compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the mean differential p-p R_x voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the base specification as $0.175V < V_{RX\text{-}DIFF\text{-}PP\text{-}CC} < 1.2V$ and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is

captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

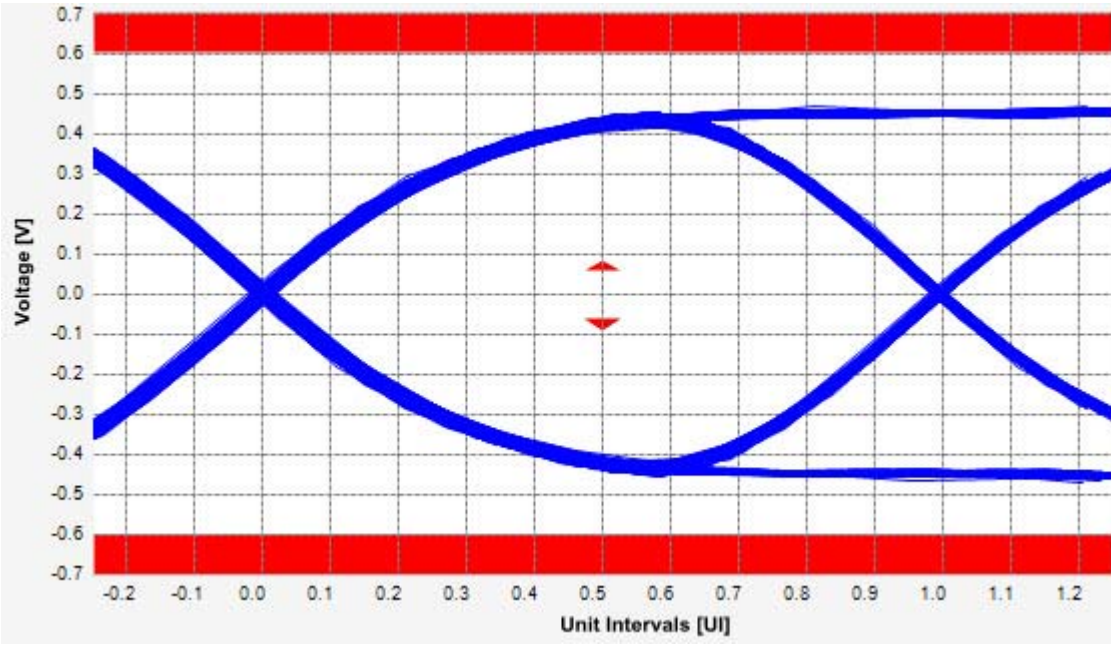


Figure 80 Reference Image for Template (Transition) Test

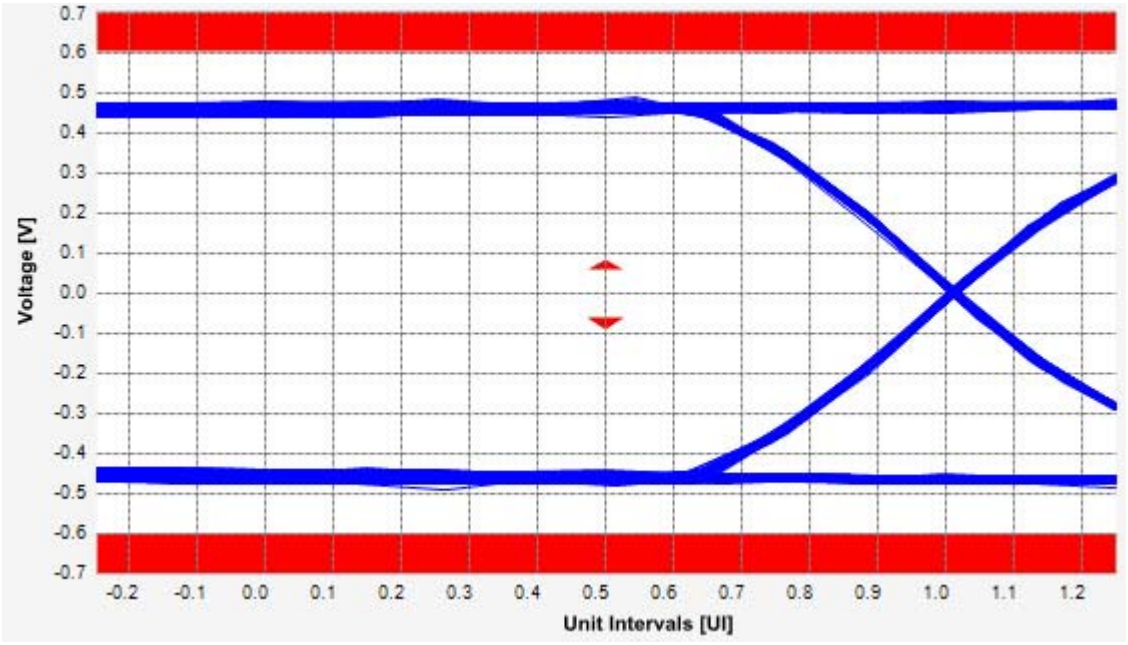


Figure 81 Reference Image for Template (Non-transition) Test

Median to Max Jitter Test

Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to the recovered T_X UI. The purpose of this test is to measure the median to max jitter between the jitter median and max deviation from the median.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 51 Median to Max Jitter Test Details

Symbol	Parameter	Max
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time delta between median and deviation from the median.	0.3UI

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Receiver Tests" on page 177 and select **Median to Max Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTestWrapper.dll file.

2 Computes the median to max jitter using the following formula:

Median to max jitter = Maximum peak to peak jitter after filter /2

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the base specification as `0.3UI >` $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 52 Eye Width Test Details

Symbol	Parameter	Min	Comments
T_{RX-EYE}	Receiver eye time opening	0.40 UI	Minimum eye time at R_x pins to yield a 10^{-12} BER.

Test Definition Notes from the Specification

Receiver eye margins are defined into a 2 x 50 Ω reference load. A receiver is characterized by driving it with a signal whose characteristics are defined by the parameters specified in Table 4-10 and Table 4-11.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Receiver Tests" on page 177 and select **Eye Width**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express Base Specification, Rev 2.0 as `0.40UI <` T_{RX-EYE}.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform.

$$V_{RX-DIFF-PP-CC} = 2*Max(Max(V_{DIFF(i)}),M(axin)(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 53 Peak Differential Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{RX-DIFF-PP-CC}$	Differential p-p T_x Voltage Swing	0.175 V	1.2 V

NOTE For more information on the peak differential output voltage test definition, refer to Section 4.3.7.2.2 of the base specification.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Receiver Tests" on page 177 and select **Peak Differential Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1. Extracts the transition eye diagram data from the SigTestWrapper.dll file.
2. Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3. Finds the peak differential output voltage (transition) mean value from the center of UI.
4. Compares the measured peak differential output voltage (transition) value to the compliance test limits.
5. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

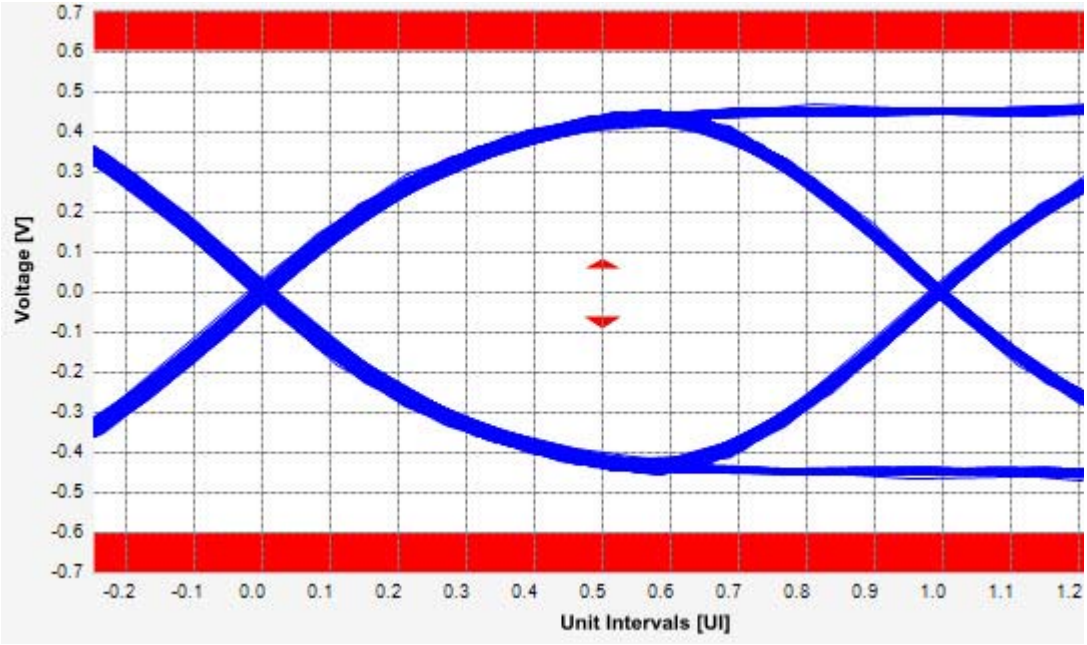


Figure 82 Reference Image for Peak Differential Output Voltage Test

AC Peak Common Mode Input Voltage Test

The average DC common mode voltage measurement computes the DC average of the common mode signal.

$$V_{TX\text{-}CM\text{-}DC} = DC_{AVG} \text{ of } |V_{TX\text{-}D+} + V_{TX\text{-}DC+}|/2$$

The PCIE Base Specification states that the transmitter DC common mode voltage must be held at the same value during all states.

NOTE This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel in put used), this test will be disabled. (see "Probing the Link for Rx Compliance" on page 174).

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 54 AC Peak Common Mode Input Voltage Test Details

Symbol	Parameter	Max	Comments
$V_{RX-CM-AC-P}$	RMS AC Common Mode Voltage	150 mV	Measured at Rx pins into a pair of 50 ohm terminations into ground.

Test Definition Notes from the Specification

Common Mode peak voltage is defined by the expression: max {|(Vd+ - Vd-) - V_{-CMDC}|}.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. Follow the procedure in "Running Receiver Tests" on page 177 and select **AC Peak Common Mode Input Voltage**.

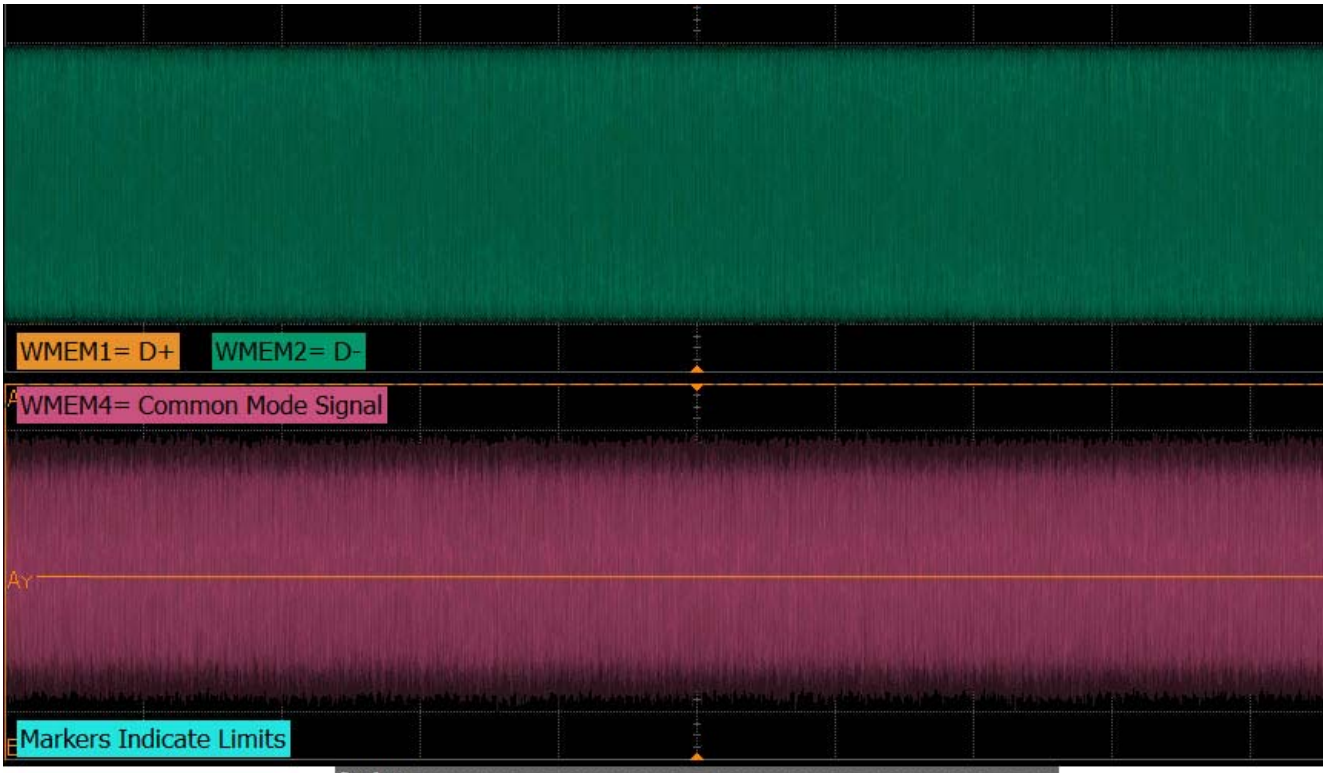
The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Sets up DC common mode voltage using **Math (FFT and more...)** as follows:
   a. Configures **Operator** as **Common Mode** measurements.
   b. Loads common mode signal.
   c. Measures the average of common mode using V average measurement from scope.
   d. Measures compliance test limit boundaries (0V to 3.6V) using **Markers**.
4. Measures the average value of D+ and D- signal.
5. Computes DC common mode value by absolute the average of the total average value of the D+ signal and average value of D- signal.
6. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `150 mV >` $V_{RX-CM-AC-p}$..

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is

captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	40.00 µs/div	0.000s	84.00 mV/div	3.875 mV
Memory 2	40.00 µs/div	0.000s	81.25 mV/div	469.7 µV
Memory 4	40.00 µs/div	0.000s	13.00 mV/div	1.295 mV

Markers

	Source	X Position	Y Position
A	Memory 4	-1.000000000000000s	0.000000V
B	Memory 4	-1.000000000000000s	3.600000V

11
Add-In Card (Tx) Tests, PCI-E 1.1

This section provides the Methods of Implementation (MOIs) for Add-In Card Transmitter tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Add-In Card Compliance

Connecting the Signal Quality Load Board for Add-in Card Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 or by-1 connector slot.

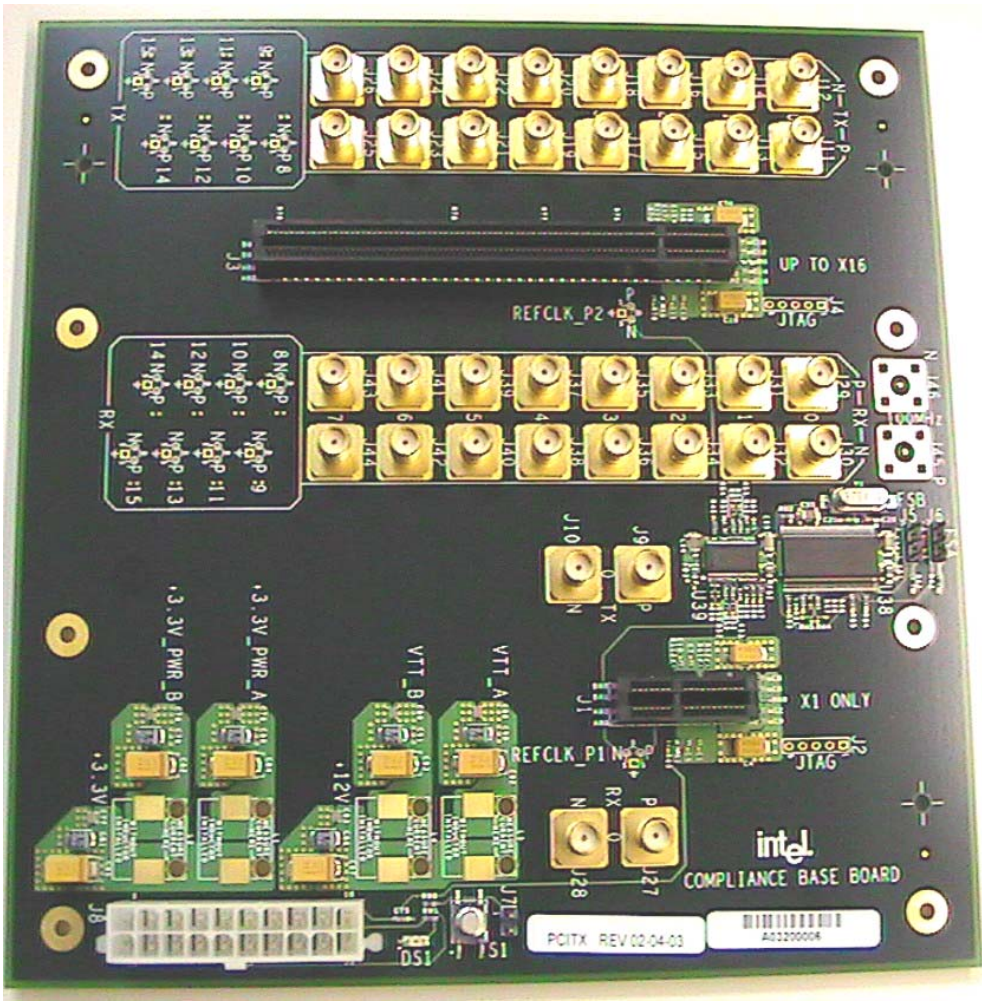


Figure 83 Compliance Base Board (CBB) Add-in Card Fixture

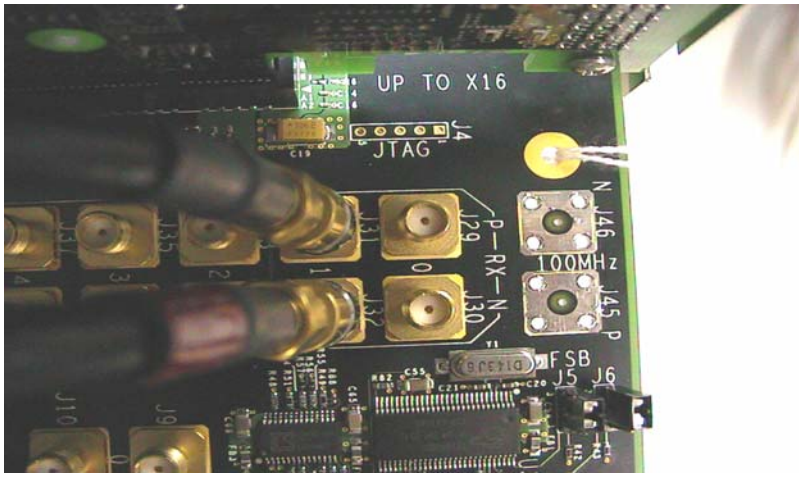


Figure 84 Compliance Base Board (CBB) SMA Probing Option

2 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the TX LANE P under test (where Lane 1 is under test in this example shown in Figure 84 above).

   b Digital Storage Oscilloscope channel 3 to the TX LANE N under test (where Lane 1 is under test in this example shown in Figure 84 above).

NOTE The Compliance Base Board labeled PCITX Rev 02-04-03 silk screen incorrectly labels the add-in card transmitter probing locations as RX.

When SMA probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 626).

Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 85 on page 194). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

3 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

4 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

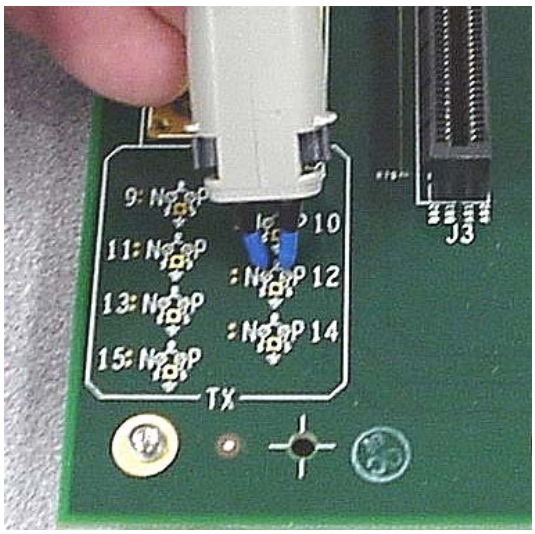


Figure 85 Compliance Base Board (CBB) Active Probing Option

Running Add-In Card Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "Add-In Card (Tx) Tests" group.

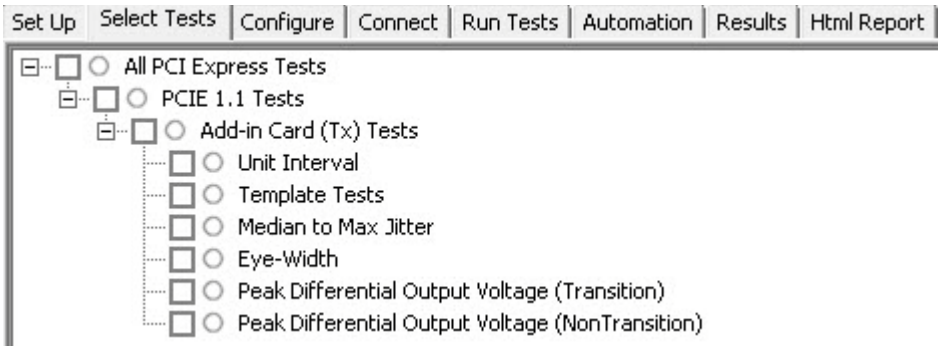


Figure 86 Selecting Add-In Card (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 55 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Add-In Card Tests" on page 195 and select **Unit Interval**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

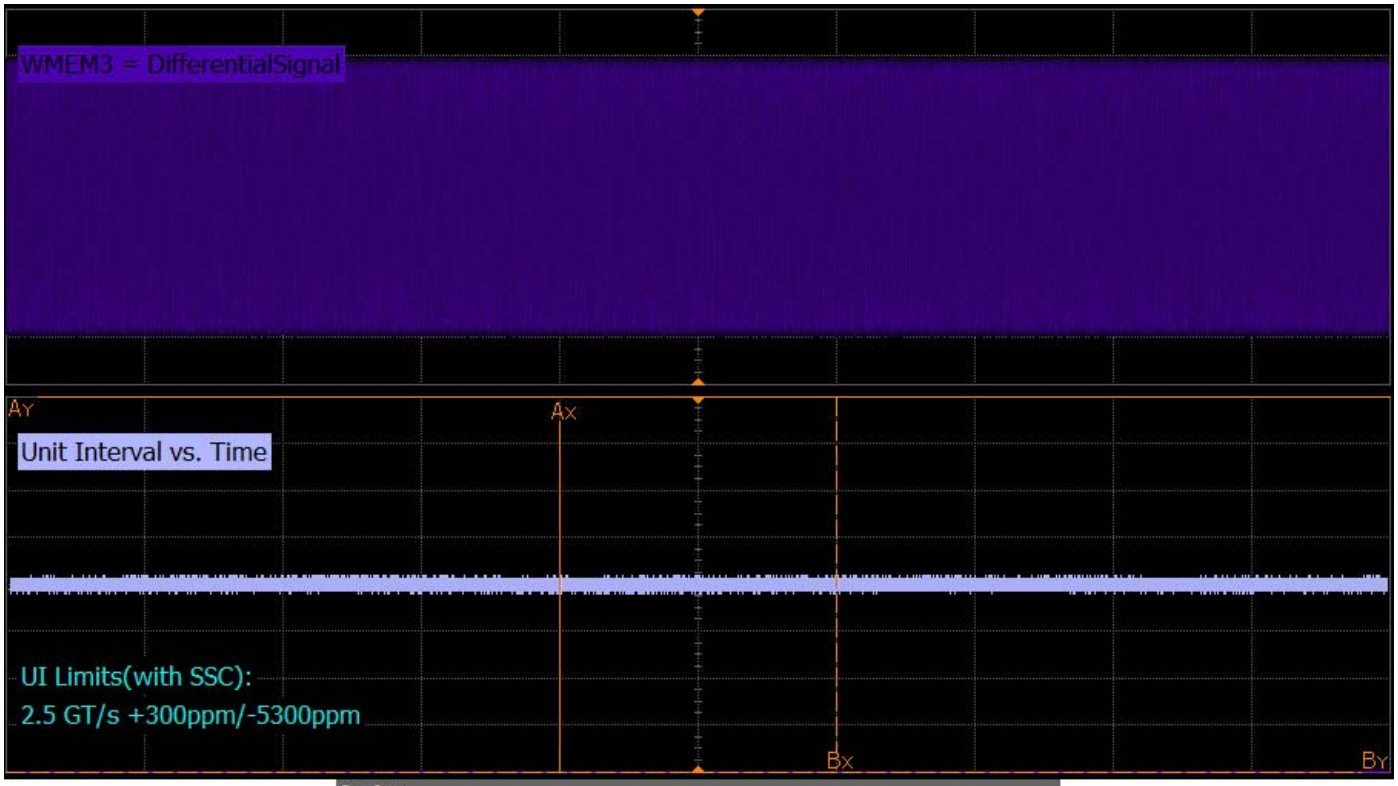
4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `399.88ps < UI < 400.12ps`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	40.00 µs/div	0.000s	20.00 fs/div	400.0 ps
Memory 3	40.00 µs/div	0.000s	162.5 mV/div	3.595 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-40.0000000000000 µs	400 pV
B	Function 3	40.0000000000000 µs	400 pV

Figure 87 Reference Image for Unit Interval Test

Template Test

Add-in cards must meet the **Add-in Card Transmitter Path Compliance Eye-Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 2.0, Section 4.7.1, Table 4-7 as measured at the card edge-fingers. This test does not validate the receiver's tolerance, rather it validates that the signal at the receiver meets the specifications in Figure 4-6.

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.1 is used as reference to check the compliance of the DUT.

Table 56 Template Test Details

Symbol	Value
Vtx_A	>= 514 mV
$Vtx_{A\_}d$	>= 360 mV
Ttx_A	>= 287 ps

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram.
- An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
- The values in Table 4-7 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

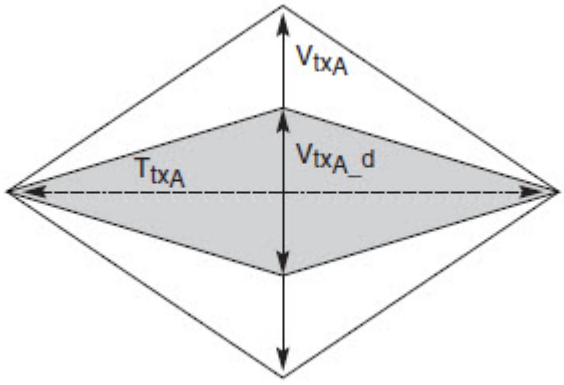


Figure 88 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Add-In Card Tests" on page 195 and select **Template Tests**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the mean differential voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 2.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

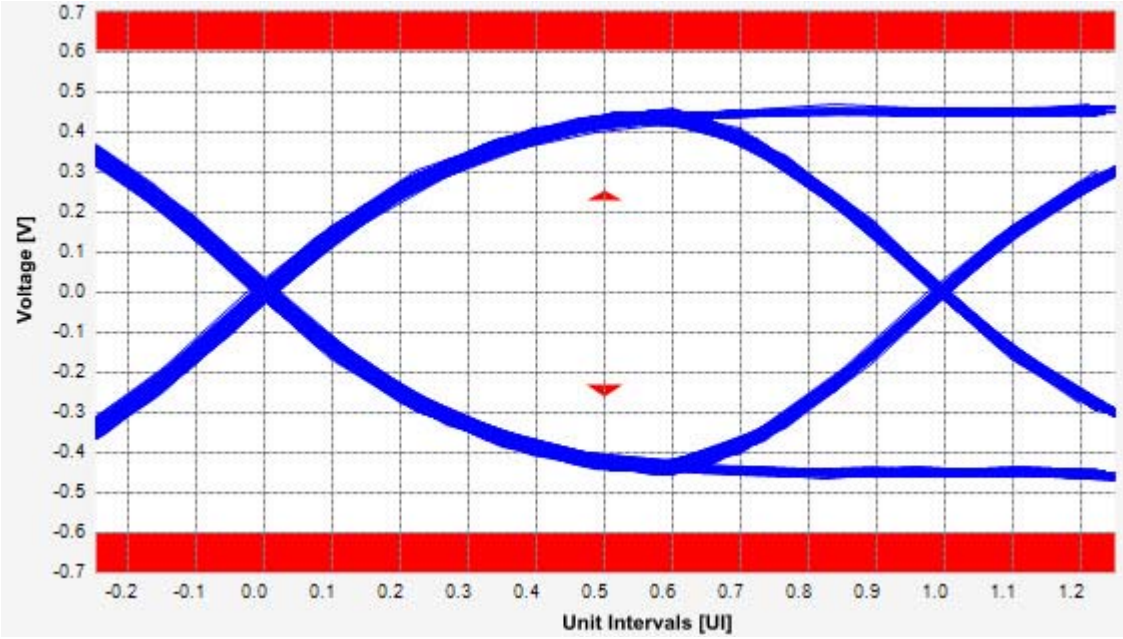


Figure 89 Reference Image for Template (Transition) Test

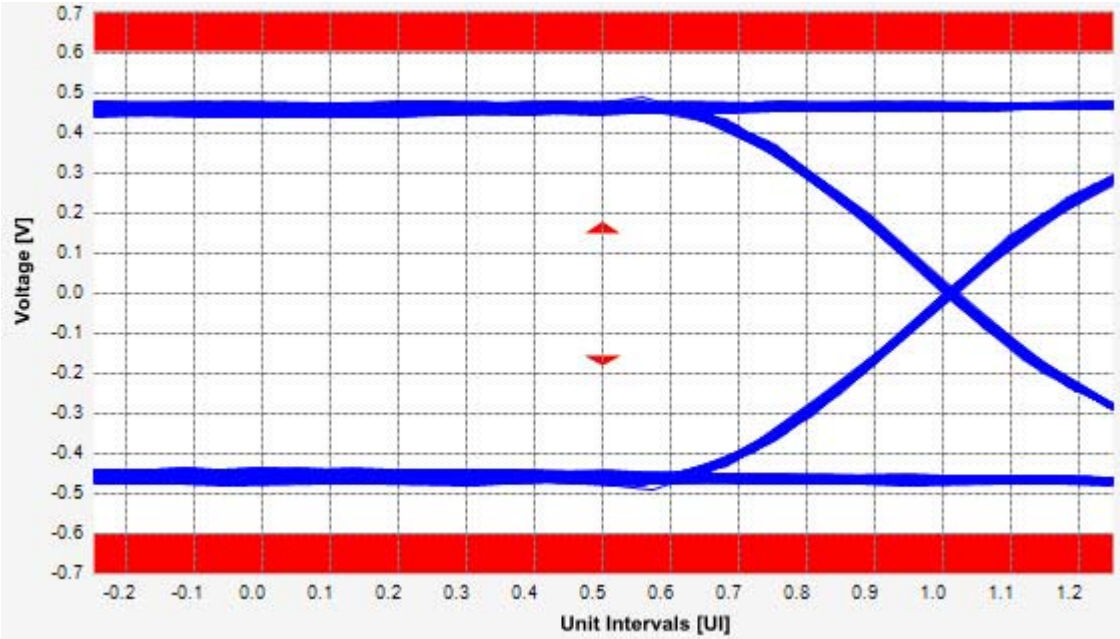


Figure 90 Reference Image for Template (Non-Transition) Test

Median to Max Jitter Test

Median to max jitter test measures the median to max jitter between the jitter median and max deviation from the median.

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.1 is used as reference to check the compliance of the DUT.

Table 57 Median to Max Jitter Test Details

Symbol	Value
Vtx_A	>= 514 mV
$Vtx_{A\_}d$	>= 360 mV
Ttx_A	>= 287 ps
$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	<=56.5ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
- The values in Table 4-7 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

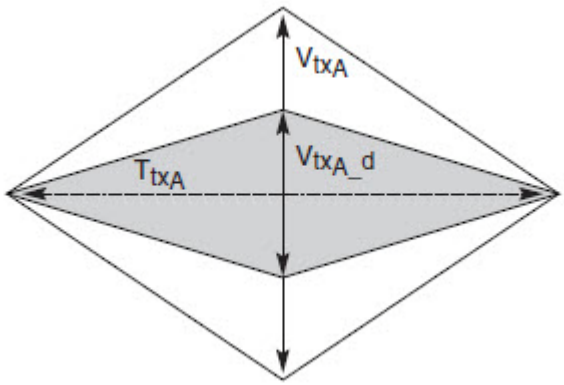


Figure 91 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 195 and select **Median to Max Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTestWrapper.dll file.

2 Computes the median to max jitter using the following formula:

Median to max jitter = Maximum peak to peak jitter after filter / 2

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 2.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is

captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.1 is used as reference to check the compliance of the DUT.

Table 58 Eye Width Test Details

Symbol	Value
Vtx_A	>= 514 mV
$Vtx_{A\_}d$	>= 360 mV
Ttx_A	>= 287 ps
$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	<=56.5ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
- The values in Table 4-7 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

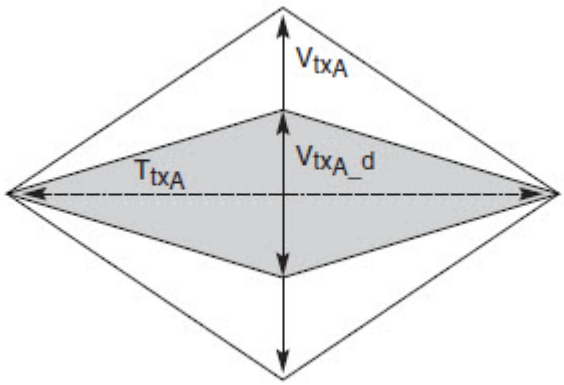


Figure 92 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 195 and select **Eye Width**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 1.0a.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits as T_{txA} >287ps.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to

view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.1 is used as reference to check the compliance of the DUT.

Table 59 Peak Differential Output Voltage Test Details

Symbol	Value
Vtx_A	>= 514 mV
Vtx_{A_d}	>= 360 mV
Ttx_A	>= 287 ps
$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	<=56.5ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
- The values in Table 4-7 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

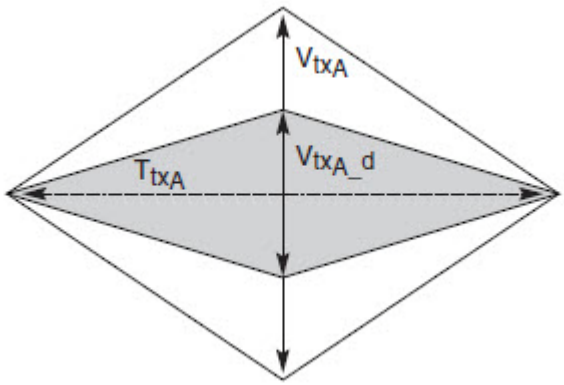


Figure 93 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 195 and select **Peak Differential Output Voltage Transition**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

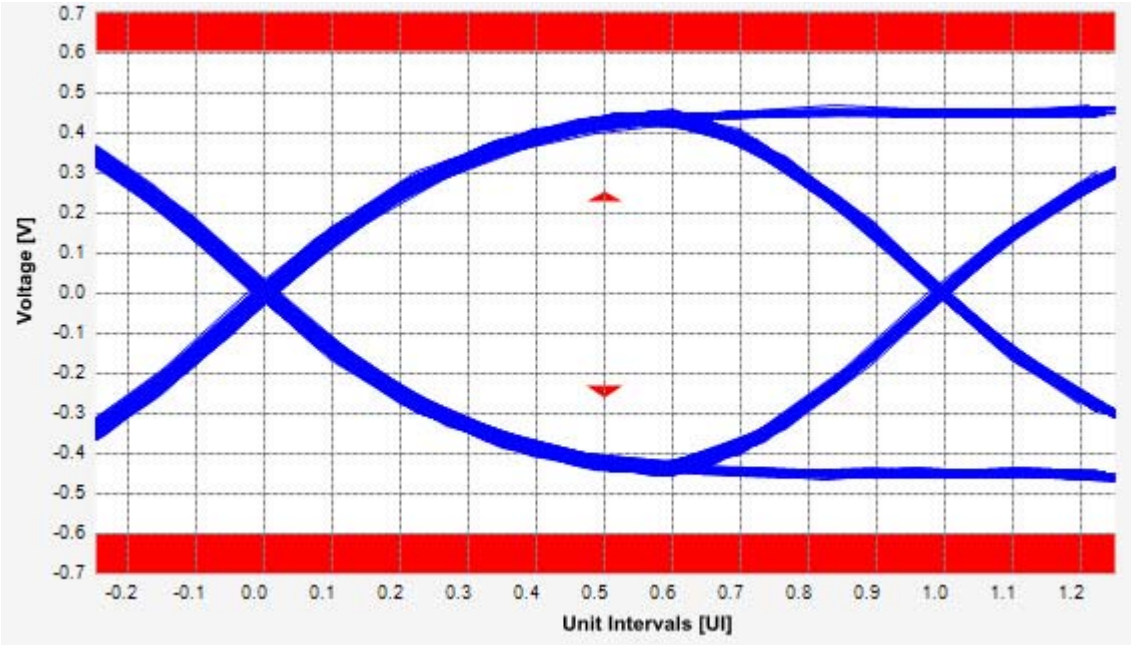


Figure 94 Reference Image for Peak Differential Output Voltage (Transition) Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 1.0a, Section 4.7.1 is used as reference to check the compliance of the DUT.

Table 60 Peak Differential Output Voltage (Non Transition) Test Details

Symbol	Value
Vtx_A	>= 514 mV
$Vtx_{A\_}d$	>= 360 mV
Ttx_A	>= 287 ps
$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	<=56.5ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
- The values in Table 4-7 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

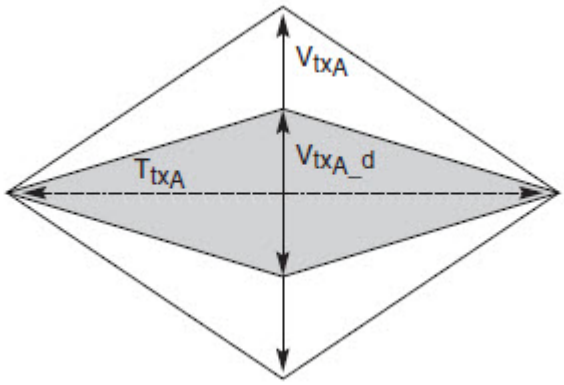


Figure 95 Add-in card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 195 and select **Peak Differential Output Voltage NonTransition**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE

This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (non transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

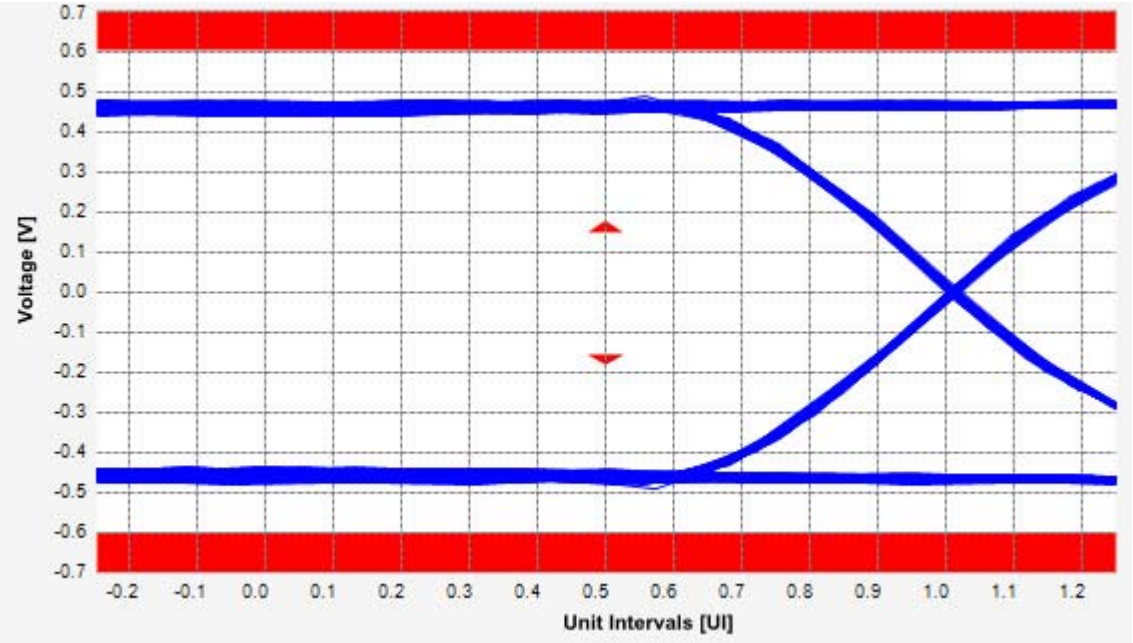


Figure 96 Reference Image for Peak Differential Output Voltage (Non-Transition) Test

12
System Board (Tx) Tests, PCI-E 1.1

This Section provides the Methods of Implementation (MOIs) for System Board Transmitter tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for System Board Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The PCI Express Signal Quality Load Board has edge fingers for x1, x4, x8 and x16 connectors.

   The PCI Express Signal Quality Load Board will cause a PCI Express 1.1 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

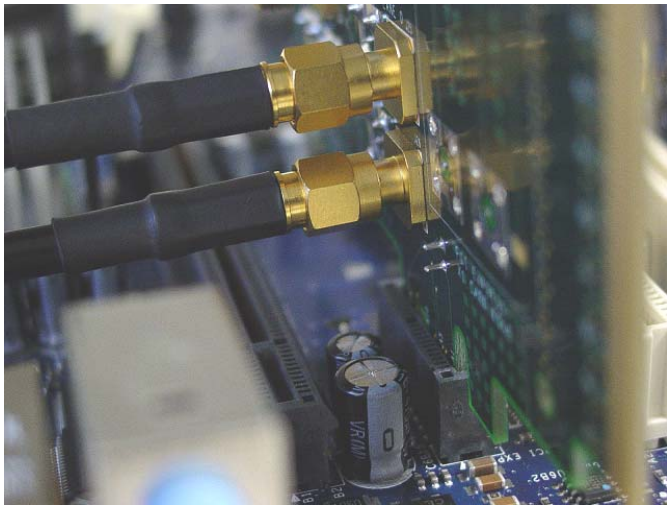


Figure 97 SMA Probing Option

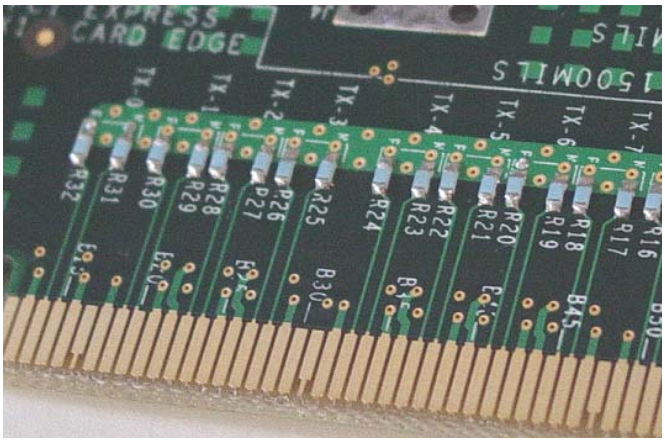


Figure 98 Resistor Terminations for Lanes without SMA Probing

2 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to TX LANE 1 P (where Lane 1 is under test).

   b Digital Storage Oscilloscope channel 3 to TX LANE 1 N (where Lane 1 is under test).

   When SMA probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 626).

   Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 85 on page 194). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

   When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

   When using a single differential probe head, use oscilloscope channel 2.

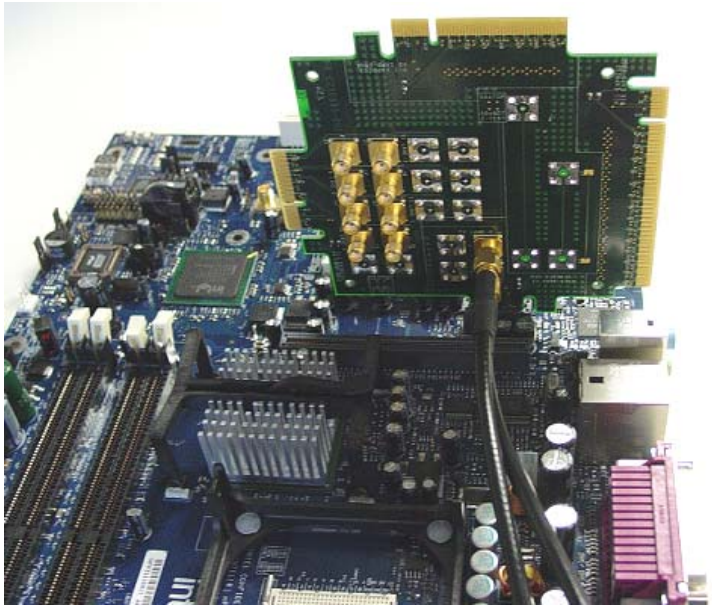


Figure 99 Connecting the PCI Express Signal Quality Test Fixture

Running System Board Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "System Board (Tx) Tests" group.

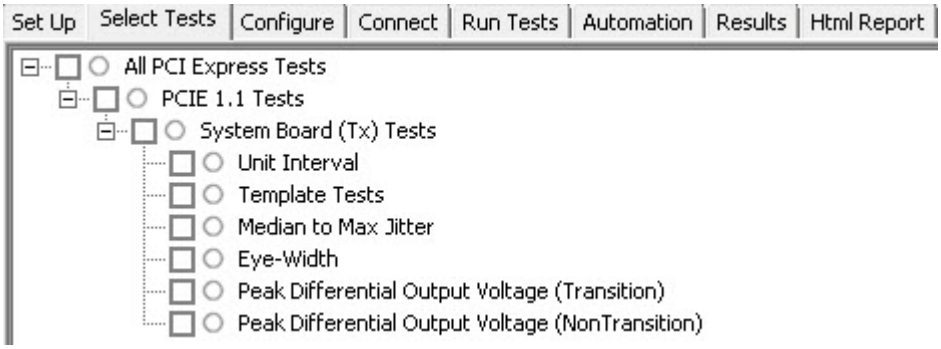


Figure 100 Selecting System Board (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI measurement is not required at this point. It is provided as an informative test only.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 61 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running System Board Tests" on page 216 and select **Unit Interval**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

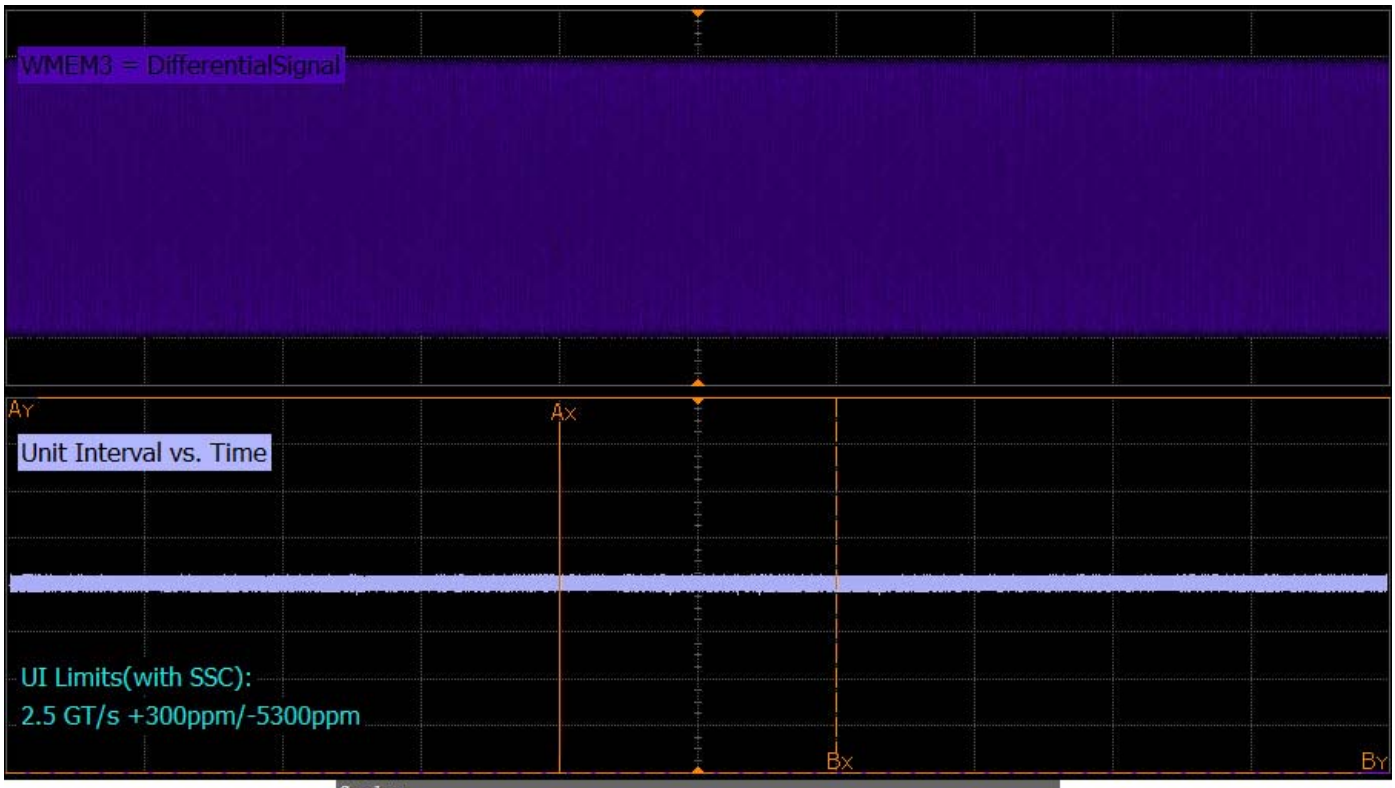
4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as `399.88ps < UI < 400.12ps`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	40.00 µs/div	0.000s	20.00 fs/div	400.0 ps
Memory 3	40.00 µs/div	0.000s	162.5 mV/div	2.849 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-39.9999999936000 µs	400 pV
B	Function 3	39.9999999936000 µs	400 pV

Figure 101 Reference Image for Unit Interval Test

Template Test

System boards must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 2.0, Section 4.7.5, table 4-14 as measured after the connector with an ideal load.

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.5, Table 4-14 is used as reference to check the compliance of the DUT.

Table 62 Template Test Details

Symbol	Min	Max
V_{TXS}	274 mV	1200mV
V_{TXS_d}	253 mV	1200mV
T_{TXS}	246 ps	
$J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$		77ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification, All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
- T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. The value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.
- $J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-max jitter outlier as defined in the PCI Express Base Specification, Revision 2.0. The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purpose at BER 10^{-12}.
- The values in Table 4-14 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary of an add-in card when mated with a connector (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

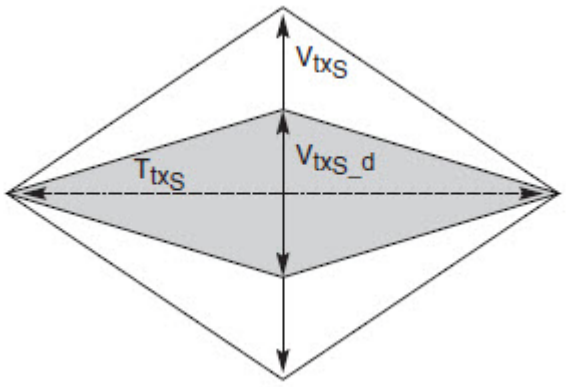


Figure 102 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running System Board Tests" on page 216 and select **Template Tests**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs compliance testing using the SigTestWrapper.dll file.
   a. Calls the system board compliance test function from the SigTestWrapper.dll file.
   b. Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.
3. Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.
4. Reports the mean differential voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 1.0a and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

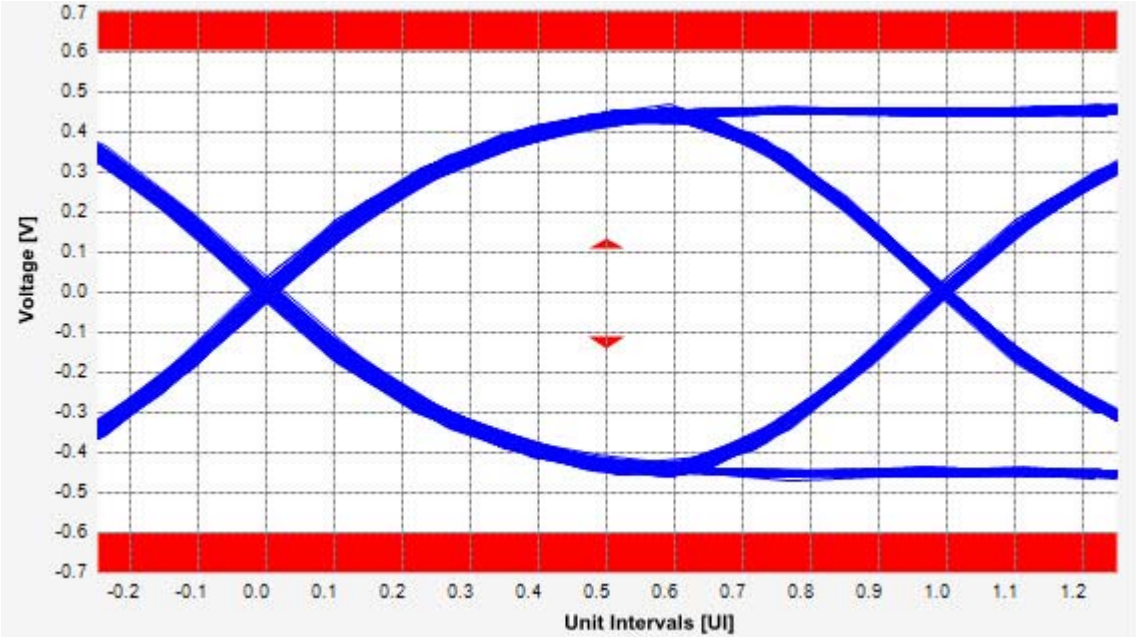


Figure 103 Reference Image for Template (Transition) Test

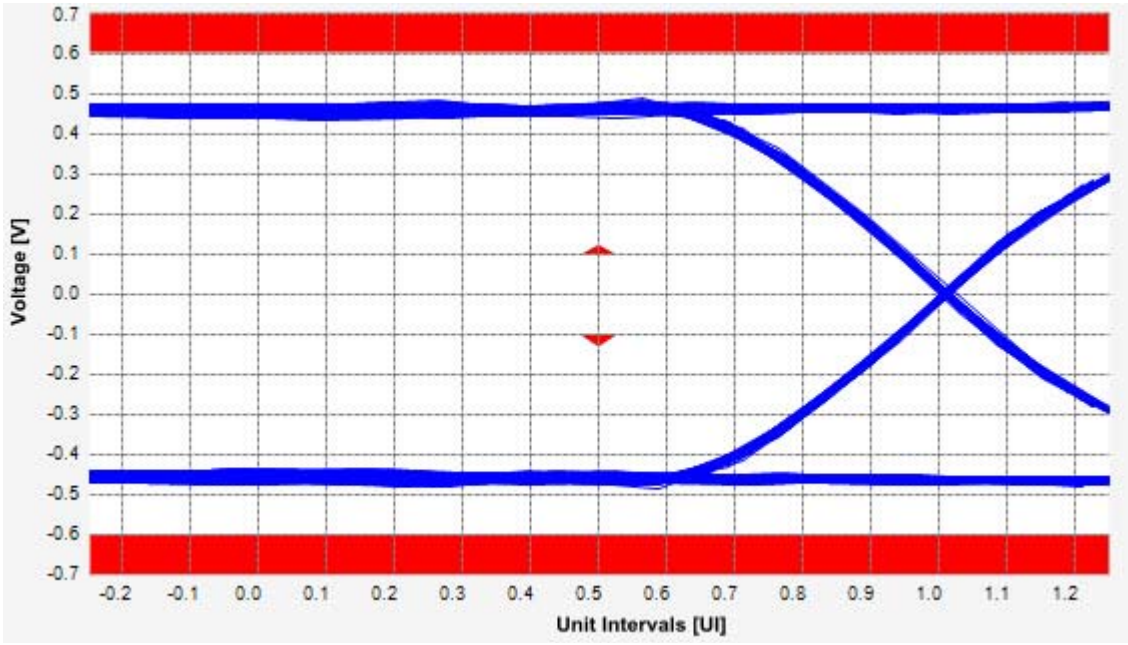


Figure 104 Reference Image for Template (Non-Transition) Test

Median to Max Jitter Test

Median to max jitter test measures the median to max jitter between the jitter median and max deviation from the median. The limit for the median to max jitter is calculated by the following equation:

$$\text{Median to max jitter} = (1\ UI - \text{Eye Width})/2$$

Where,

1 UI = 400ps

Eye Width = 183ps

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.5, Table 4-14 is used as reference to check the compliance of the DUT.

Table 63 Median To Max Jitter Test Details

Symbol	Min	Max
V_{TXS}	274 mV	1200mV
V_{TXS_d}	253 mV	1200mV
T_{TXS}	246 ps	
$J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$		77ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification, All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
- T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. The value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.
- $J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-max jitter outlier as defined in the PCI Express Base Specification, Revision 2.0. The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purpose at BER 10^{-12}.

- The values in Table 4-14 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary of an add-in card when mated with a connector (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

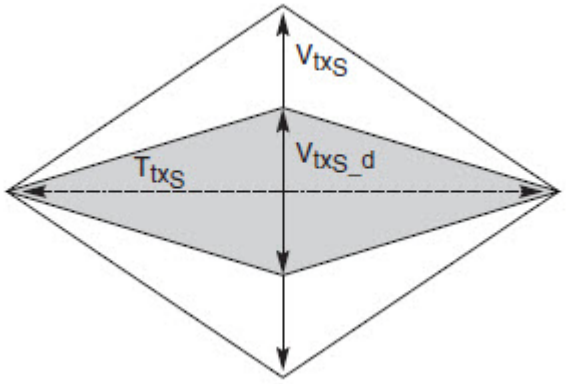


Figure 105 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 216 and select **Median to Max Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Obtains the value for the maximum peak to peak jitter after filter parameter from the SigTestWrapper.dll file.

2 Computes the median to max jitter using the following formula:

Median to max jitter = Maximum peak to peak jitter after filter / 2

3 Reports the median to max jitter as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 1.0a as 108.5ps.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.5, Table 4-14 is used as reference to check the compliance of the DUT.

Table 64 Eye Width Test Details

Symbol	Min	Max
V_{TXS}	274 mV	1200mV
V_{TXS_d}	253 mV	1200mV
T_{TXS}	246 ps	
$J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$		77ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification, All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
- T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. The value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.
- $J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-max jitter outlier as defined in the PCI Express Base Specification, Revision 2.0. The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purpose at BER 10^{-12}.

- The values in Table 4-14 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary of an add-in card when mated with a connector (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

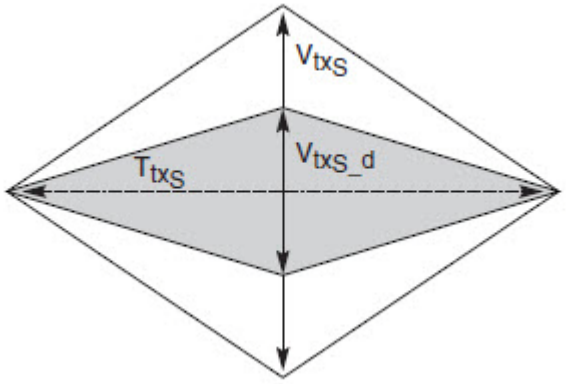


Figure 106 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 216 and select **Eye Width**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits as T_{txS} >246ps.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.5, Table 4-14 is used as reference to check the compliance of the DUT.

Table 65 Peak Differential Output Voltage Test Details

Symbol	Min	Max
V_{TXS}	274 mV	1200mV
V_{TXS_d}	253 mV	1200mV
T_{TXS}	246 ps	
$J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$		77ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification, All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
- T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. The value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.

- $J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-max jitter outlier as defined in the PCI Express Base Specification, Revision 2.0. The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purpose at BER 10^{-12}.
- The values in Table 4-14 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary of an add-in card when mated with a connector (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

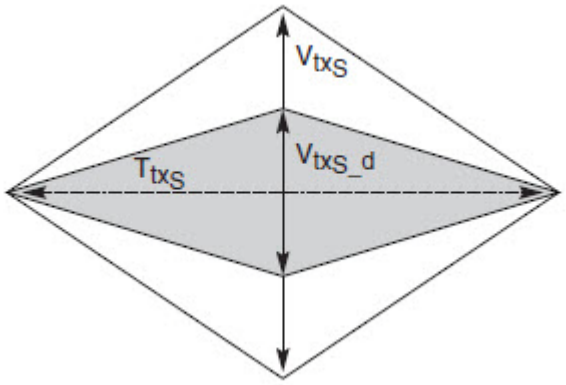


Figure 107 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 216 and select **Peak Differential Output Voltage (Transition)**.

he PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

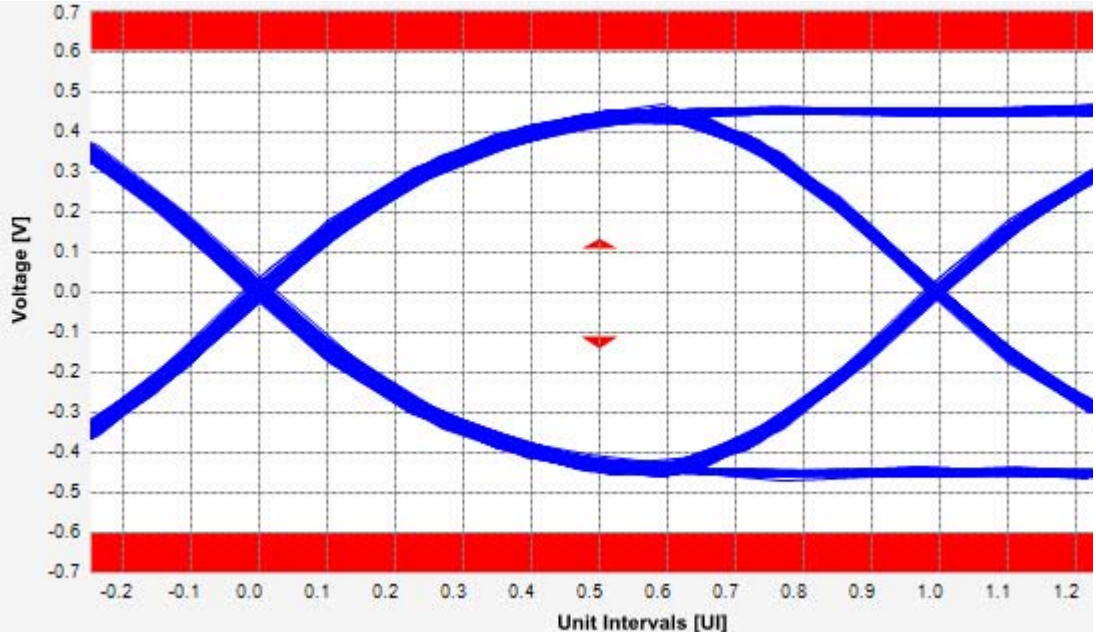


Figure 108 Reference Image for Peak Differential Output Voltage (Transition) Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.5, Table 4-14 is used as reference to check the compliance of the DUT.

Table 66 Peak Differential Output Voltage (Non Transition) Test Details

Symbol	Min	Max
V_{TXS}	274 mV	1200mV
V_{TXS_d}	253 mV	1200mV
T_{TXS}	246 ps	
$J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$		77ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification, All links are assumed active while generating this eye diagram.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
- T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. The value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.
- $J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-max jitter outlier as defined in the PCI Express Base Specification, Revision 2.0. The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purpose at BER 10^{-12}.

- The values in Table 4-14 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary of an add-in card when mated with a connector (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

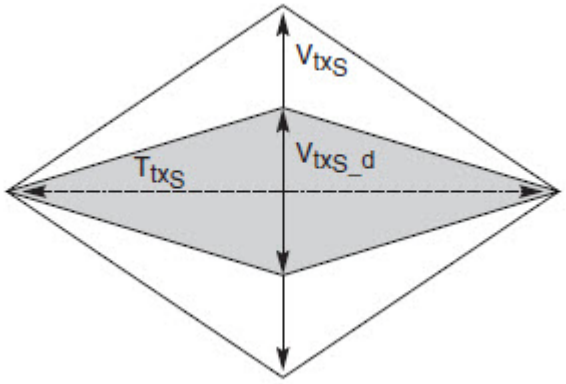


Figure 109 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 216 and select **Peak Differential Output Voltage NonTransition**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1. Extracts the non transition eye diagram data from the SigTestWrapper.dll file.
2. Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.
3. Finds the peak differential output voltage (non transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

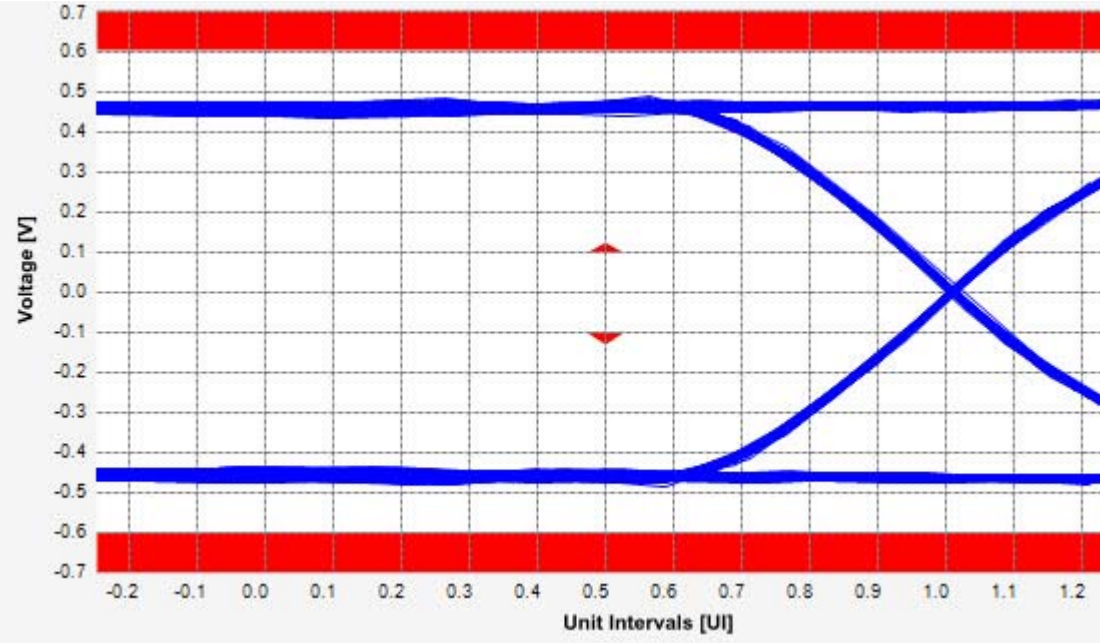


Figure 110 Reference Image for Peak Differential Output Voltage (Non-Transition) Test

13
Reference Clock Tests, PCI-E 1.1

This section provides the Methods of Implementation (MOIs) for Reference Clock tests using an Agilent 90000X Series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Reference Clock Compliance

Reference Clock tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the reference clock link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Card Electromechanical Specification) will be transmitted.

Table 67 Probing Options for Reference Clock Testing

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended SMA Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1-Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

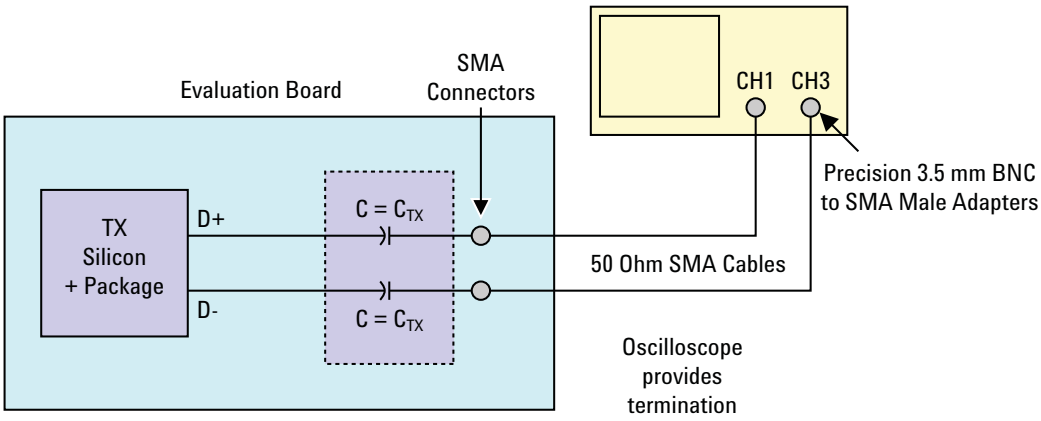


Figure 111 Single-Ended SMA Probing using Channel 1 and Channel 3

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the reference clock, as close as possible to the reference clock. Place single-ended grounds as close to the signal line's reference ground as possible. Channel-to-Channel deskew is required using this probing technique because two channels are used.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

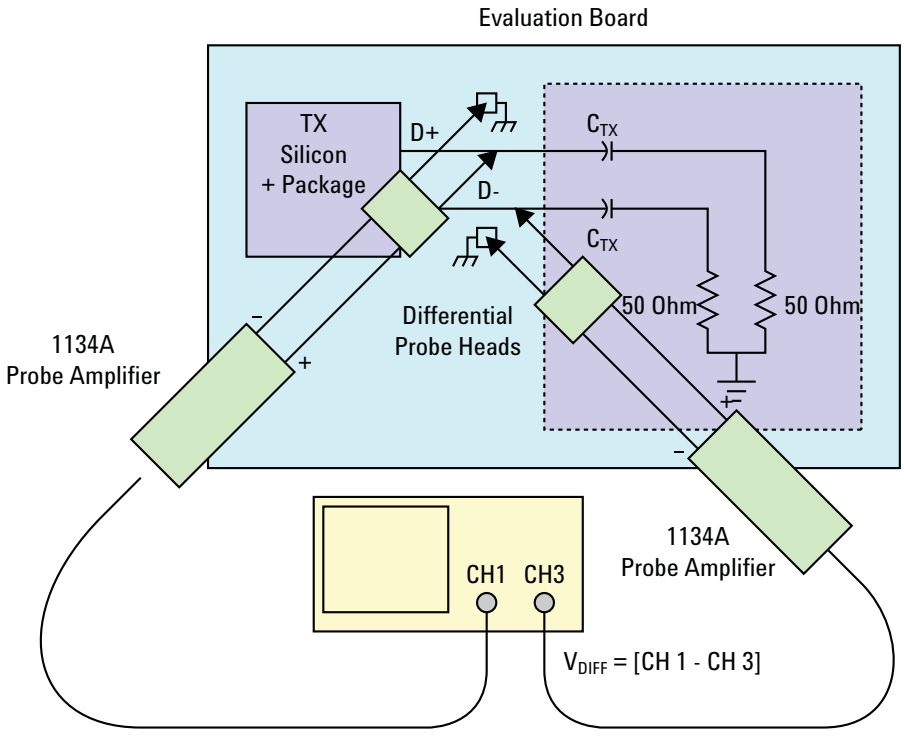


Figure 112 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the reference clock, as close as possible to the reference clock.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

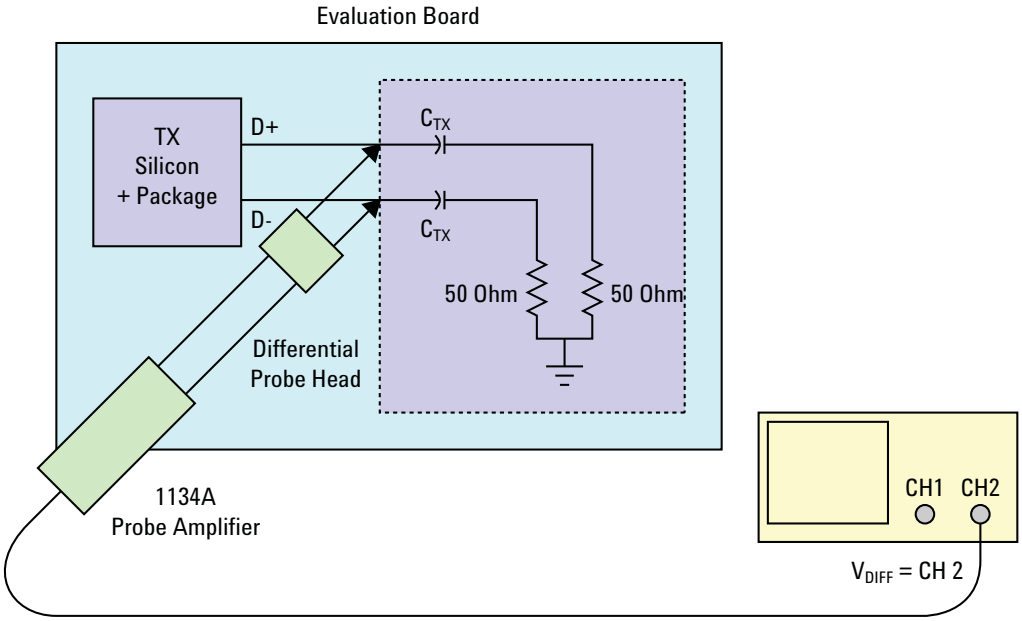


Figure 113 Differential Probing

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in Figure 4-25 of the Card Electromechanical Specification.

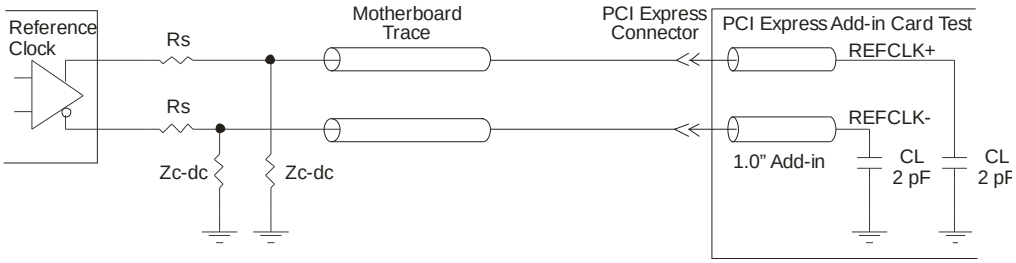


Figure 114 Driver Compliance Test Load.

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "Reference Clock Tests" group.

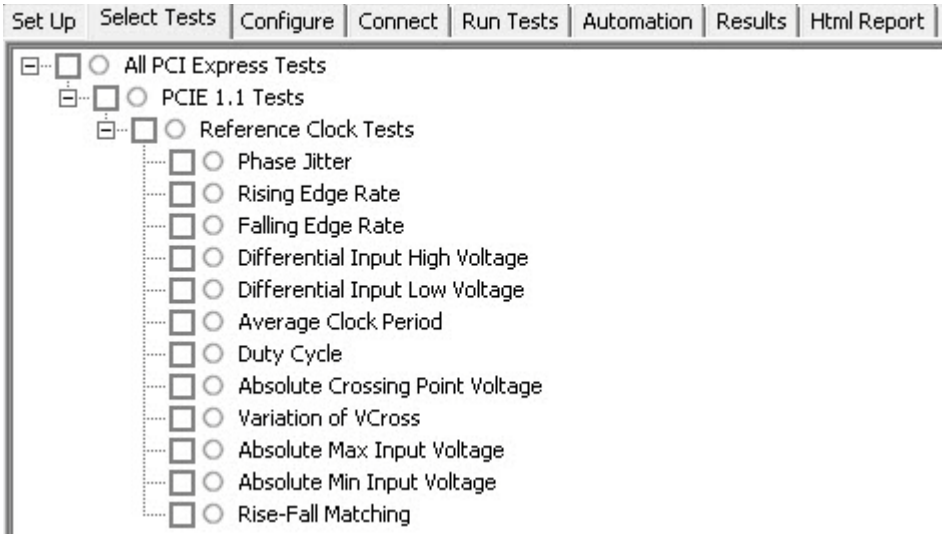


Figure 115 Selecting Reference Clock Tests

Phase Jitter Test

Phase jitter is measured using the clock time interval error measurement with a bit error rate of 10^{-6}.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.4, Table 2-2 is used as reference to check the compliance of the DUT.

Table 68 Maximum Allowed Phase Jitter When Applied to Fixed Filter Characteristic.

BER	Maximum Peak-Peak Phase Jitter Value (ps)
10^{-6}	86

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Phase Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Verifies that the signal period is ~ $100MHz$.

3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

5 Configures **Memory Depth** to **20.0000Mpts** as **Manual** using **Acquisition Setup**.

6 Fits and displays all sample data on screen.

7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.

8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

9 Stitches each acquired acquisition to make a continuous TIE data.

NOTE

You can use the **Stitch Method** configuration setting on scope to select the method used to stitch the waveform for the reference clock phase jitter test. The stitch method configuration setting applies only when the Spread Spectrum Clocking is enabled.

- Absolute - this method stitches the waveform based on absolute data.
- Dynamic - this method aligns waveform data to have common offset before stitching.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies the PLL filter using parameters for common clocked architecture.

   c Converts back the frequency domain TIE data to time domains.

   d Computes the filtered peak-peak jitters.

11 Reports filtered peak-peak jitter as phase jitter and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as less than or equal to `86ps`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

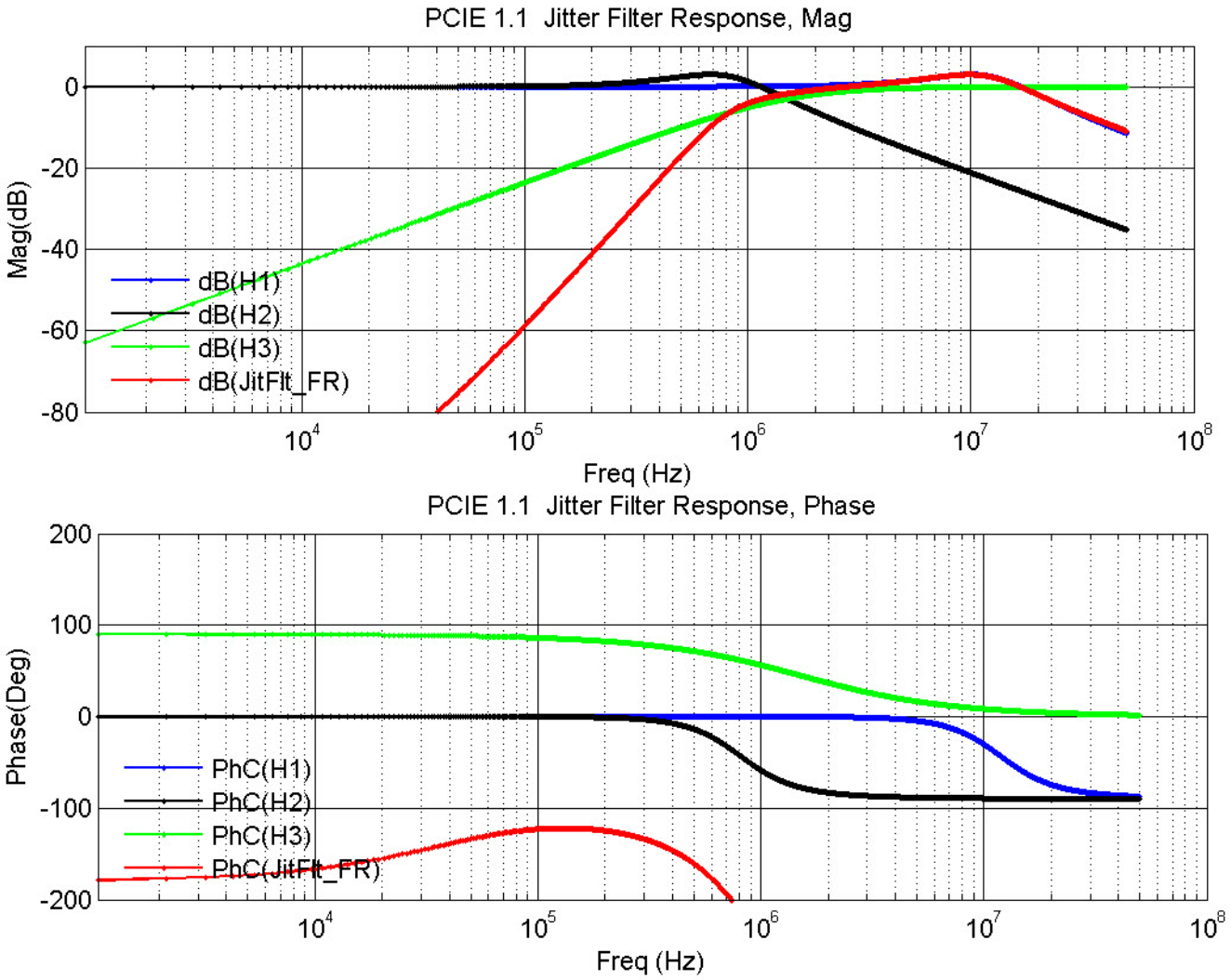


Figure 116 Reference Image for Jitter Filter Response

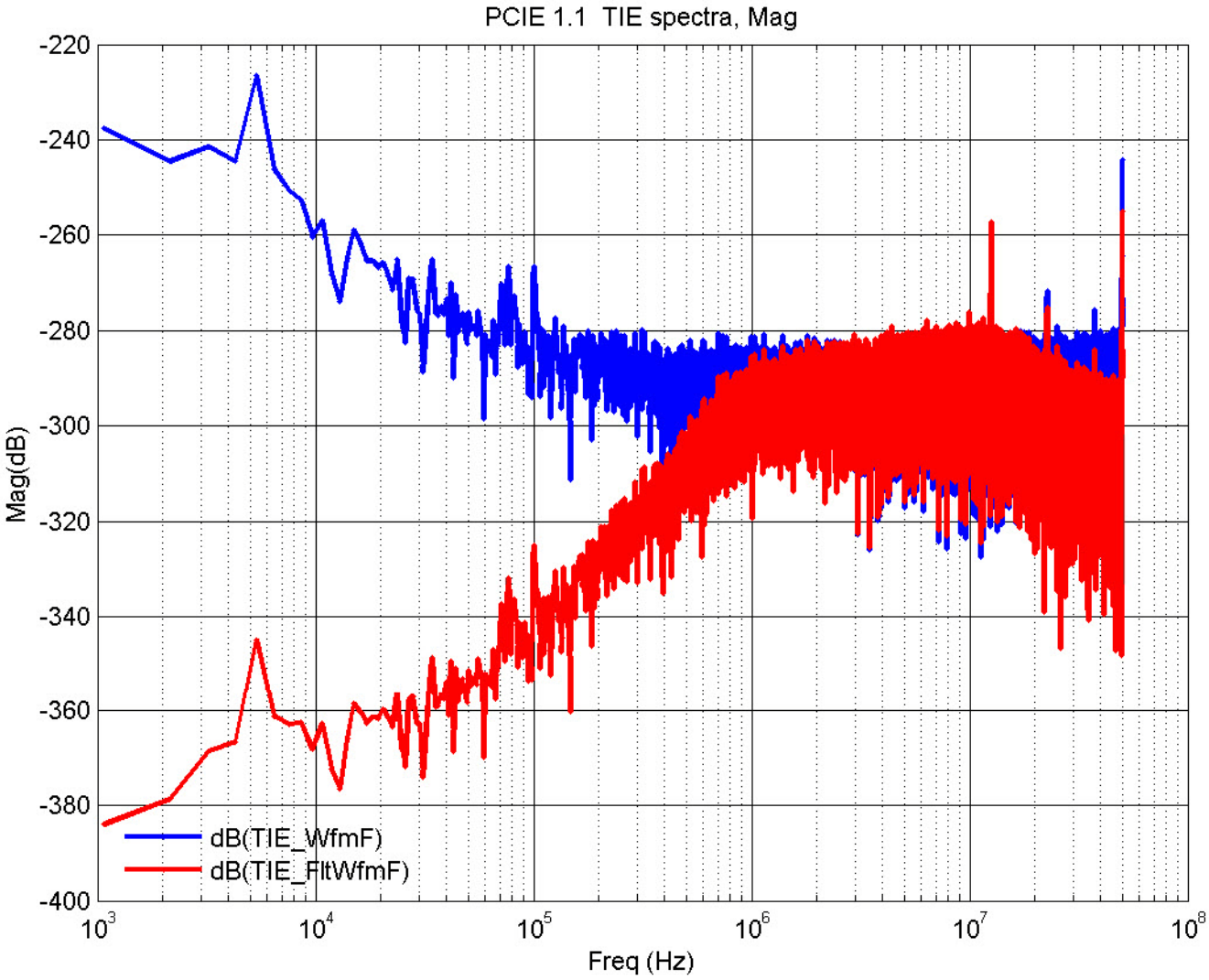


Figure 117 Reference Image for TIE Spectra, Mag

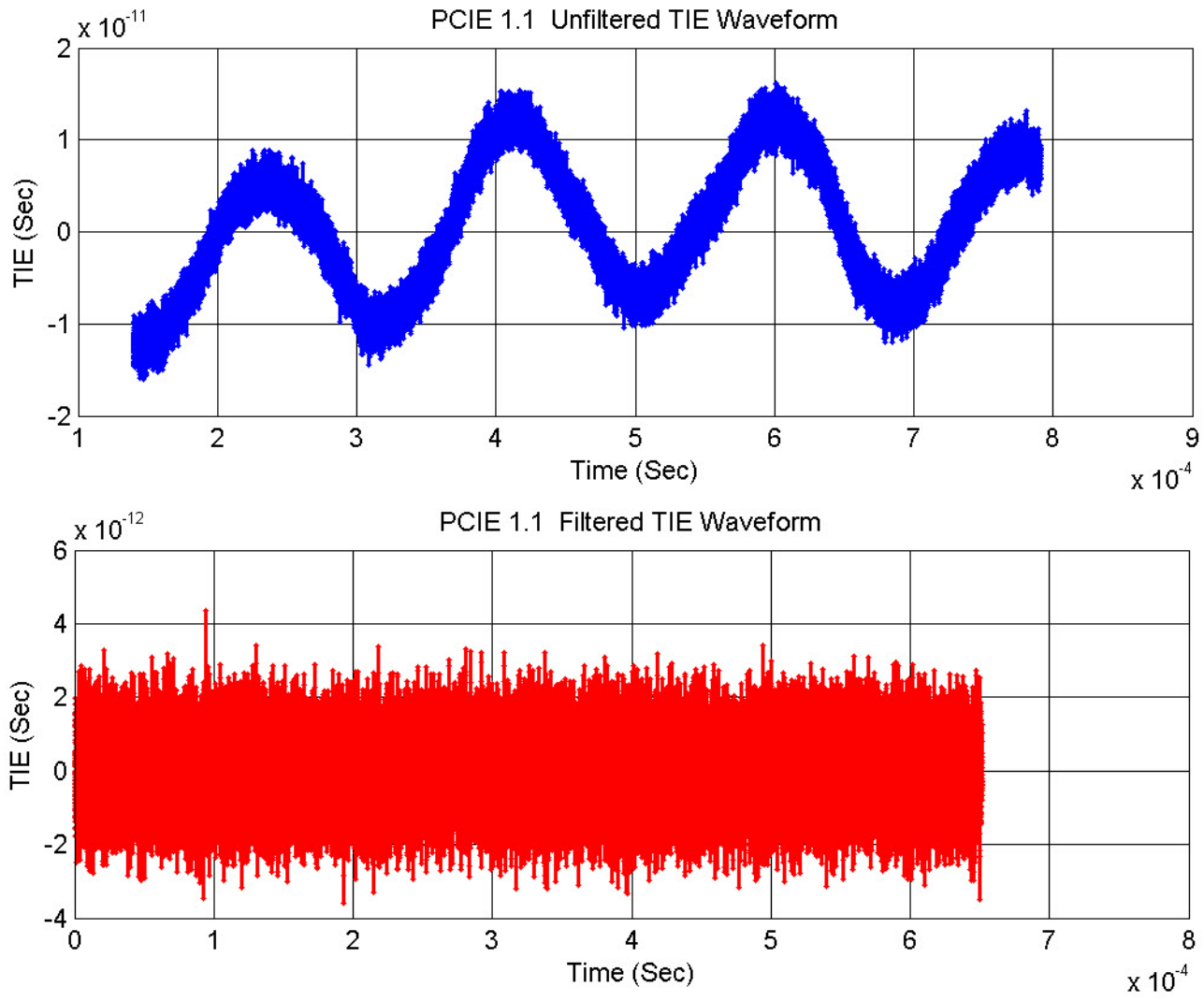


Figure 118 Reference Image for Unfiltered TIE Waveform

Rising Edge Rate Test

The rising edge rate test is measured from -150mV to +150mV on the differential waveform which is derived from RefClk+ minus RefClk-. The signal must be monotonic through the measurement region for rise time and 300mV measurement window is centered on the differential zero crossing.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 69 Rise Edge Rate Test Details

Symbol	Parameter	Min	Max
Rise Edge Rate	Rising Edge Rate	0.6 V/ns	4.0 V/ns

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 2-7.

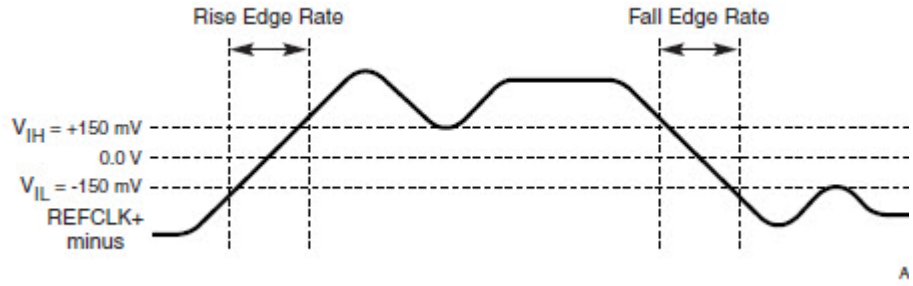


Figure 119 Differential Measurement Points for Rise and Fall Time

Understanding the Test Flow

NOTE

To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Rising Edge Rate**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Fits and displays all sample data on screen.

4 Configures the **Top Level** threshold to 150mV and **Base Level** threshold to -150mV using **Threshold Setup**.

5 Measures the maximum rise time using **Rise time** measurement.

6 Zoom to maximum value of rise time.

7 Converts the maximum rise time to units of V/ns as given in the PCIE spec. [0.0000000003 / Maximum Rise Time value].

8 Reports the rising edge rate value and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as `0.6 V/ns` ≥ Rising Edge Rate ≤ 4.0 V/ns.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

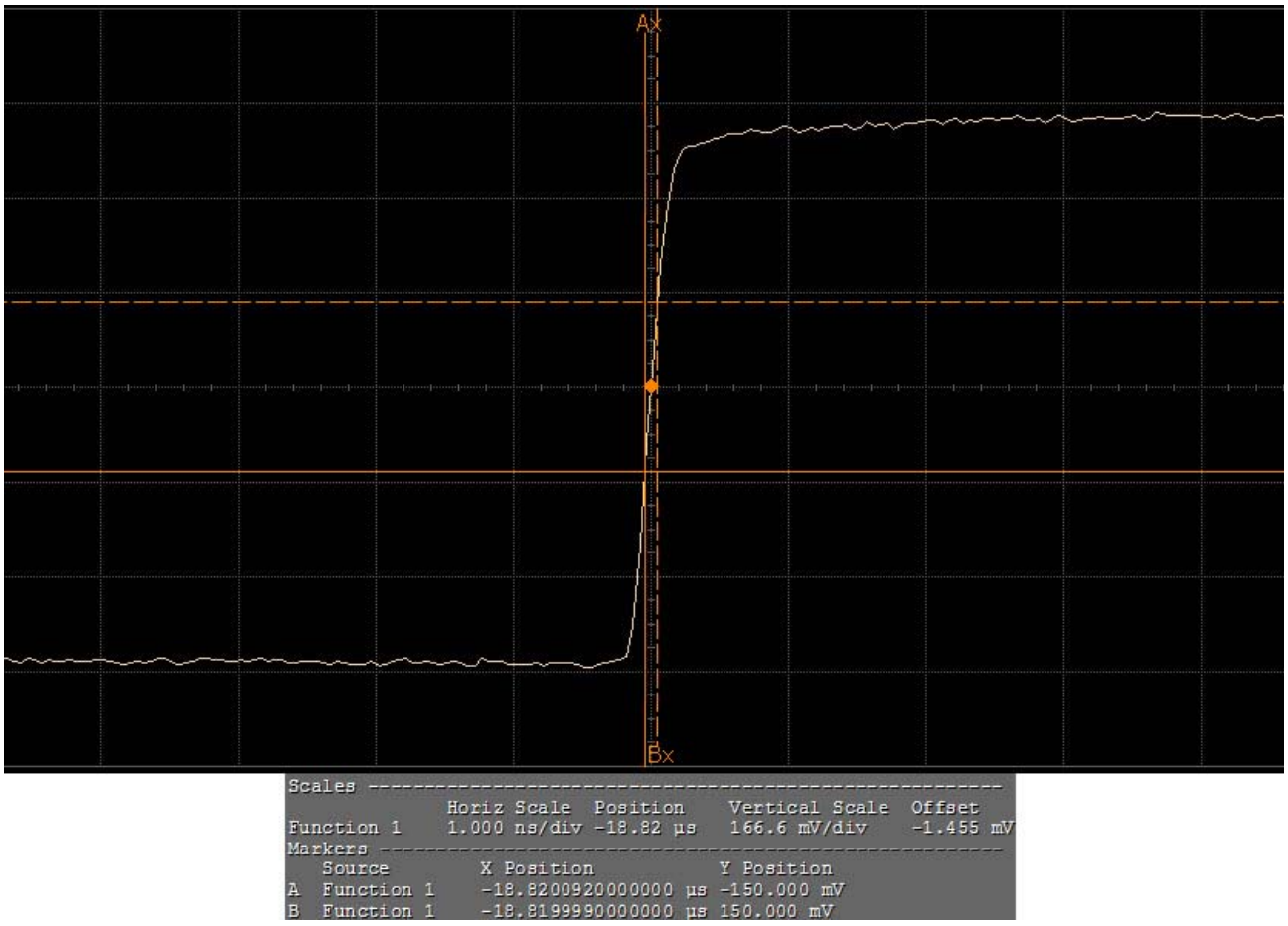


Figure 120 Reference Image for Rising Edge Rate

Falling Edge Rate Test

The falling edge rate test is measured from -150mV to +150mV on the differential waveform which is derived from RefClk+ minus RefClk-. The signal must be monotonic through the measurement region for fall time and 300mV measurement window is centered on the differential zero crossing.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 70 Falling Edge Rate Test Details

Symbol	Parameter	Min	Max
Fall Edge Rate	Falling Edge Rate	0.6 V/ns	4.0 V/ns

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 2-7.

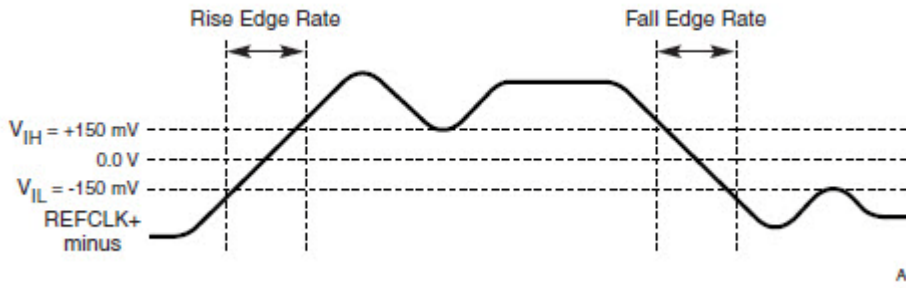


Figure 121 Differential Measurement Points for Rise and Fall Time

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Falling Edge Rate**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Fits and displays all sample data on screen.
4. Configures the **Top Level** threshold to 150mV and **Base Level** threshold to -150mV using **Threshold Setup**.
5. Measures the maximum fall time using **Fall time** measurement.

6 Zoom the resultant waveform to maximum value of fall time.

7 Converts the maximum fall time to units of V/ns as given in the PCIE specification [0.0000000003 / Maximum Fall Time value].

8 Reports the falling edge rate value and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as 0.6 V/ns ≤ Falling Edge Rate ≤ 4.0 V/ns.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

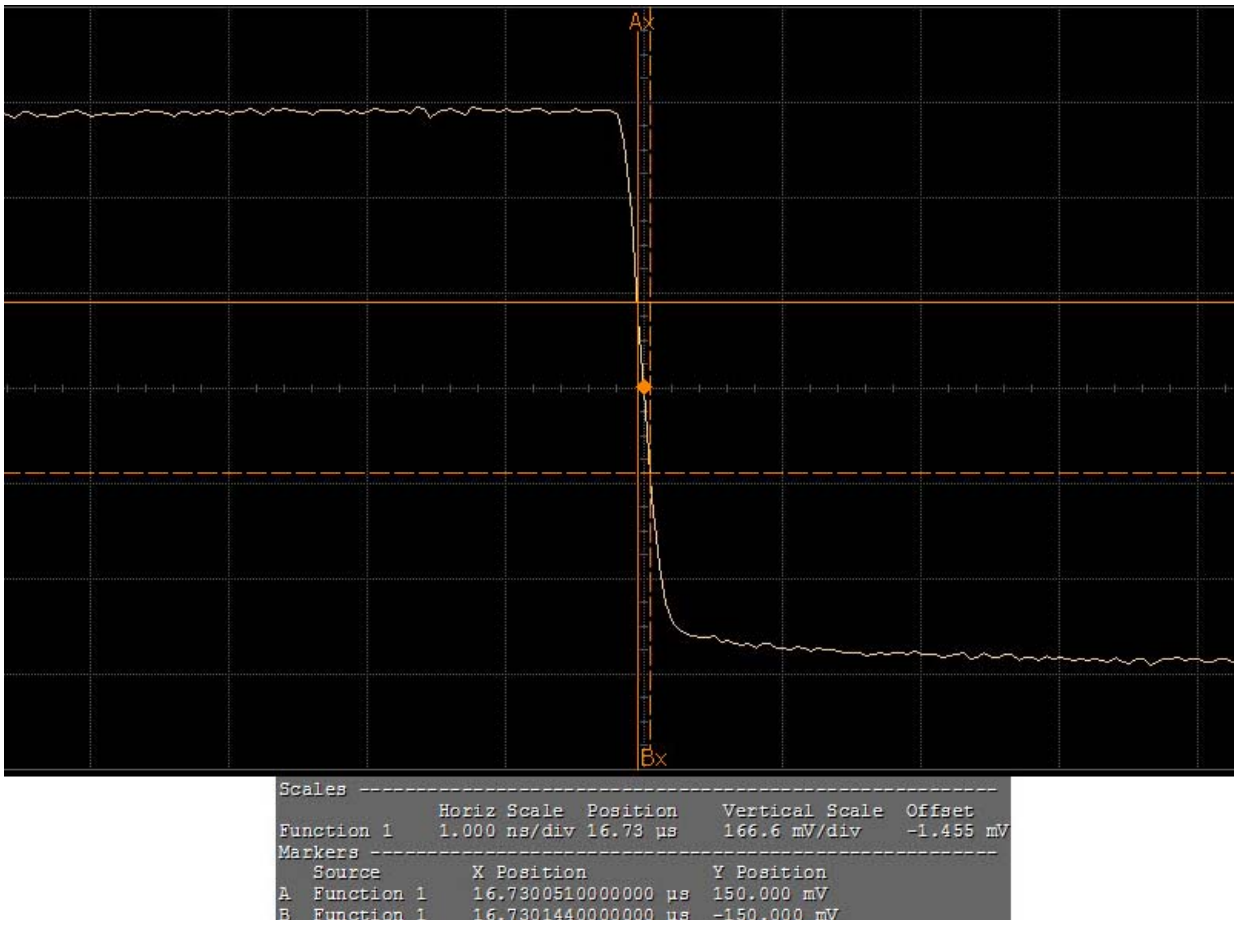


Figure 122 Reference Image for Falling Edge Rate

Differential Input High Voltage Test

The differential input high voltage test verifies that the reference clock differential input high voltage is within the conformance limits specified in Table 2-1 of the PCI Express CEM Specifications v1.1.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 71 Differential Input High Voltage Test Details

Symbol	Parameter	Min
V_{IH}	Differential Input High Voltage	150 mV

Test Definition Notes from the Specification

Measurement taken from differential waveform.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Differential Input High Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Fits and displays all sample data on screen.
4. Configures the **Top Level** threshold to 150mV and **Base Level** threshold to -150mV using **Threshold Setup**.
5. Measures the maximum voltage using **V max** measurement.
6. Reports the maximum voltage value as differential input high voltage and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as $V_{IH} > 150$ mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

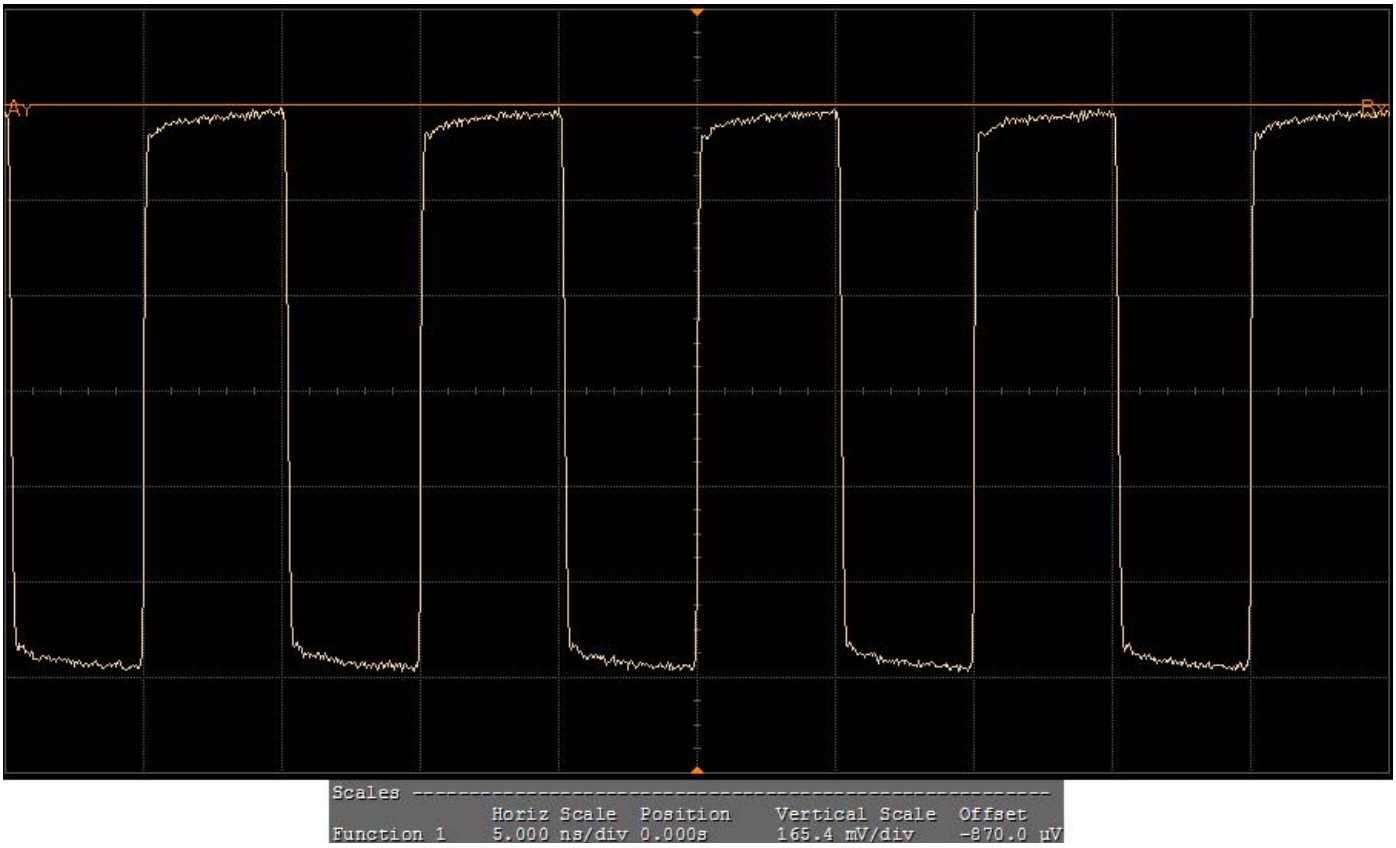


Figure 123 Reference Image for Differential Input High Voltage Test

Differential Input Low Voltage Test

The differential input low voltage test verifies that the reference clock differential input low voltage is within the conformance limits specified in Table 2-1 of the PCI Express CEM Specifications v1.1.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 72 Differential Input Low Voltage Test Details

Symbol	Parameter	Max
V_{IL}	Differential Input High Voltage	150 mV

Test Definition Notes from the Specification

Measurement taken from differential waveform.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Differential Input Low Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Fits and displays all sample data on screen.
4. Configures the **Top Level** threshold to 150mV and **Base Level** threshold to -150mV using **Threshold Setup**.
5. Measures the minimum voltage using **V min** measurement.
6. Reports the minimum voltage value as differential input low voltage and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as $V_{IL} < 150$ mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

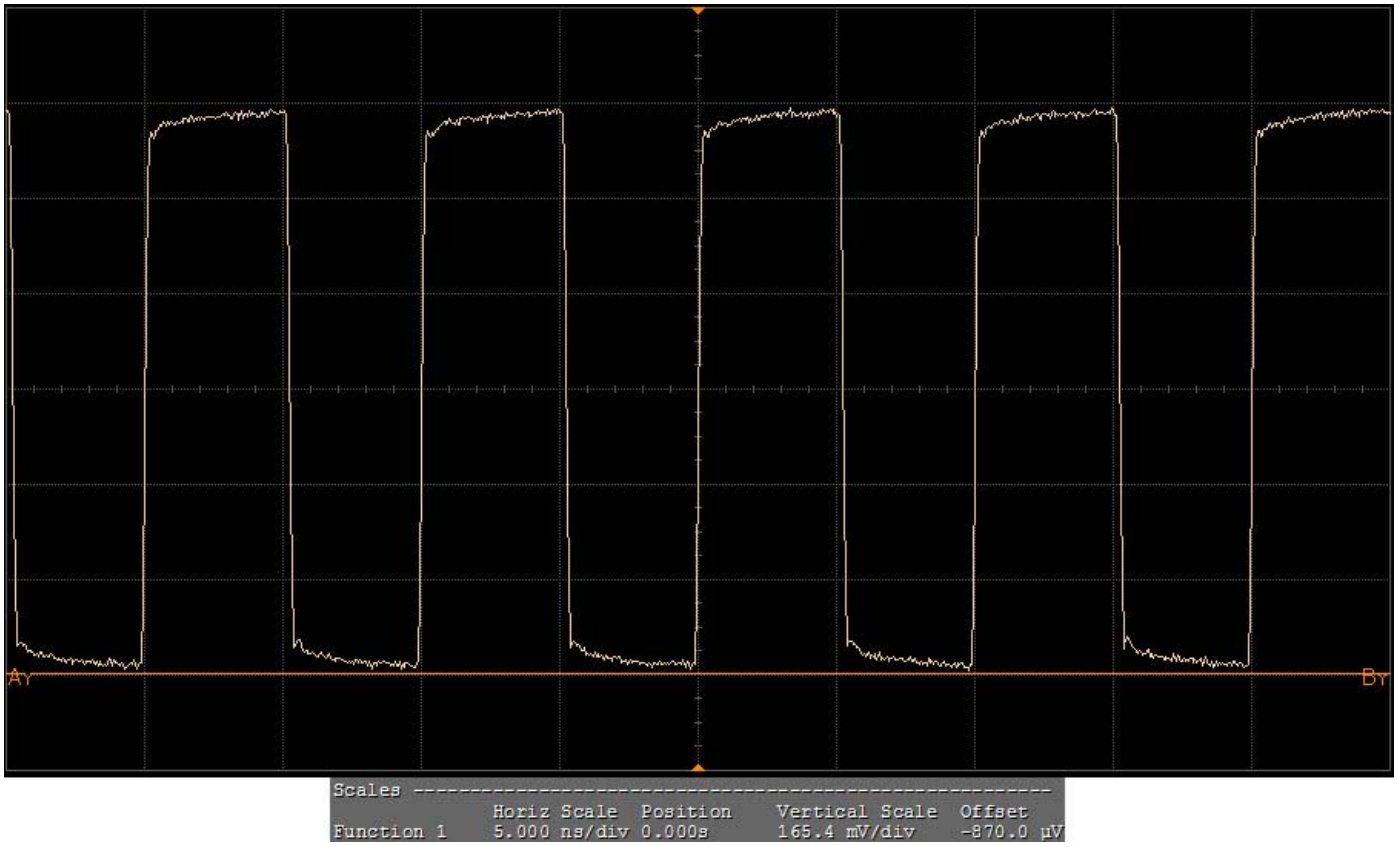


Figure 124 Reference Image for Differential Input Low Voltage Test

Average Clock Period

The average clock period measures that the average clock period accuracy is within the range -300ppm to 2800ppm. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100 Hz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 73 Average Clock Period Test Details

Symbol	Parameter	Min	Max
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	2800 ppm

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding PPM considerations.
- PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000MHz exactly or 100MHz. For 300 PPM then we have a error budget of 100Hz/PPM * 300 PPM = 30KHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The +-300 PPM applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800PPM.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Average Clock Period**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Fits and displays all sample data on screen.
4. Measures the average voltage using **V average** measurement.
5. Configures the **Top Level** threshold to +150mV and **Base Level** threshold to -150mV using **Threshold Setup**.
6. Measures the average frequency using **Frequency** measurement of **Clock**.
7. Measures the average period using **Period** measurement of **Clock**.
8. Computes the difference between ideal and actual frequency in terms of parts per million of 100MHz as follows:

$$\text{Difference between ideal and actual frequency} = [100MHz - AverageFrequency]/100$$

9. Reports the average clock period accuracy and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1.

For SSC,

-300 ppm ≤ Average Clock Period Accuracy ≤ 2.8 kppm

For clean clock,

-300 ppm ≤ Average Clock Period Accuracy ≤ 300 ppm

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

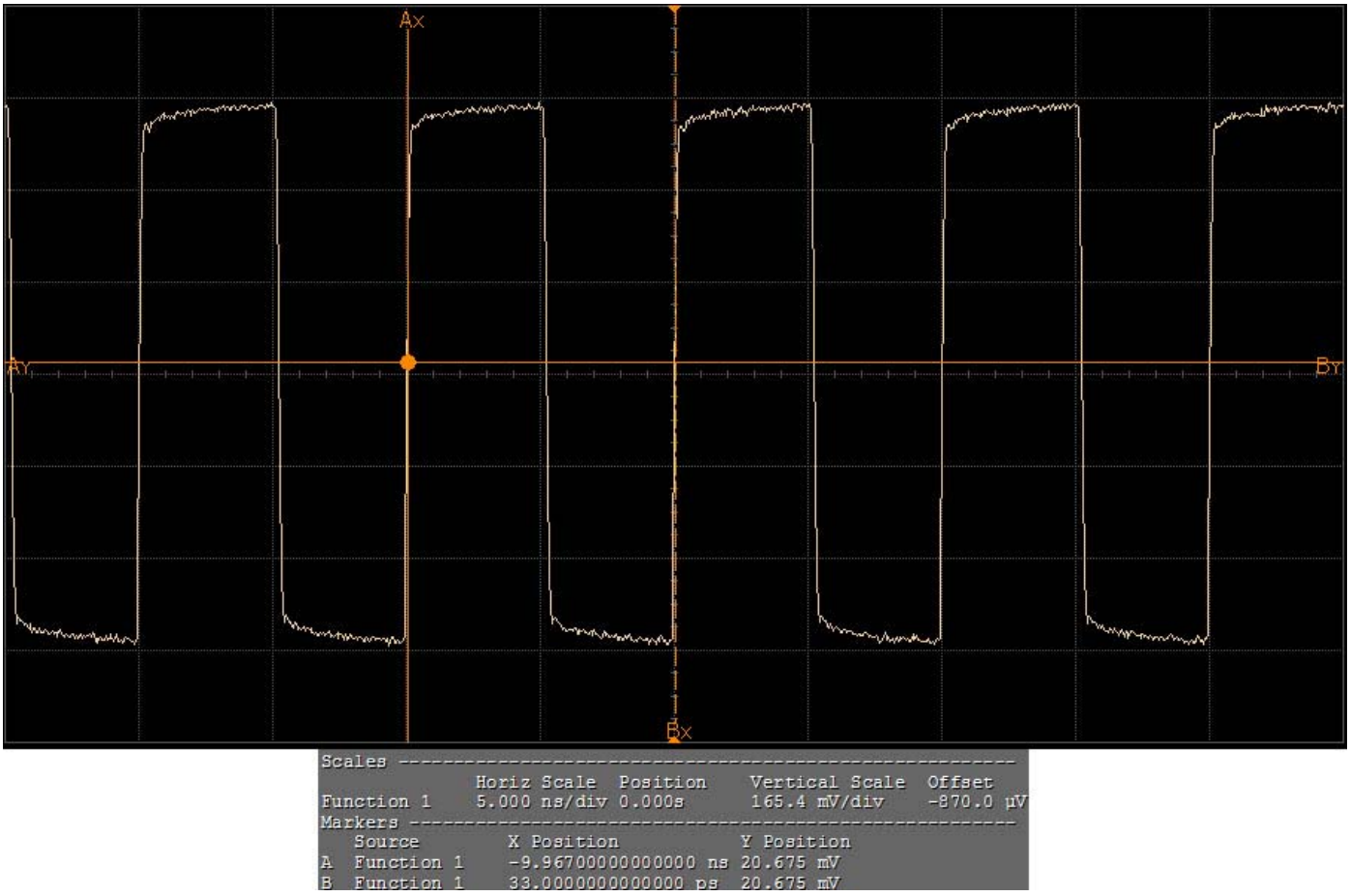


Figure 125 Reference Image for Average Clock Period

Duty Cycle Test

The duty cycle test verifies that the reference clock average clock period is within the conformance limits specified in Table 2-1 of the PCI Express CEM Specifications v1.1.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 74 Duty Cycle Test Details

Symbol	Parameter	Min	Max
Duty Cycle	Duty Cycle	40%	60%

Test Definition Notes from the Specification

Measurement taken from differential waveform.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Duty Cycle**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Fits and displays all sample data on screen.
4. Measures the average voltage using **V average** measurement.
5. Configures the **Top Level** threshold to 150mV and **Base Level** threshold to -150mV using **Threshold Setup**.
6. Measures the duty cycle using the **Duty cycle** measurement.
7. Finds the margin for maximum duty cycle and minimum duty cycle.
8. Compares the margin and choose the largest margin to report the value (worst value) as duty cycle.
9. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express

Card Electromechanical Specification Rev. 1.1 as `40% ≤ Duty Cycle ≤ 60%`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

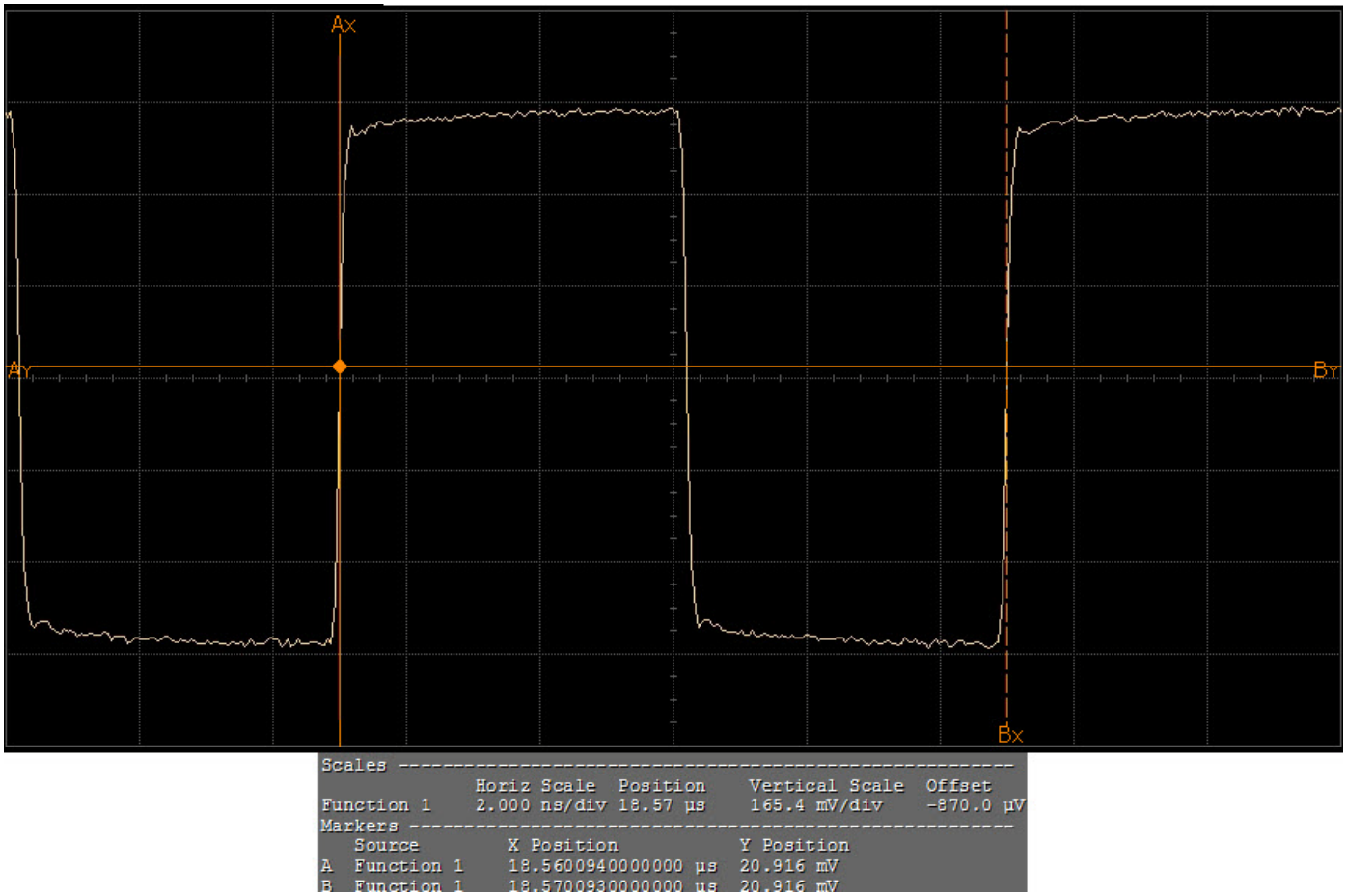


Figure 126 Reference Image for Duty Cycle

Absolute Crossing Point Voltage Test

The absolute crossing point voltage test is measured at crossing point where the instantaneous voltage value of the rising edge of RefClk+ equals the falling edge of RefClk-. It refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 75 Absolute Crossing Point Voltage Test Details

Symbol	Parameter	Min	Max
V_{CROSS}	Absolute Crossing Point Voltage	+250mV	+550mV

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 2-3.
- Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 2-3.

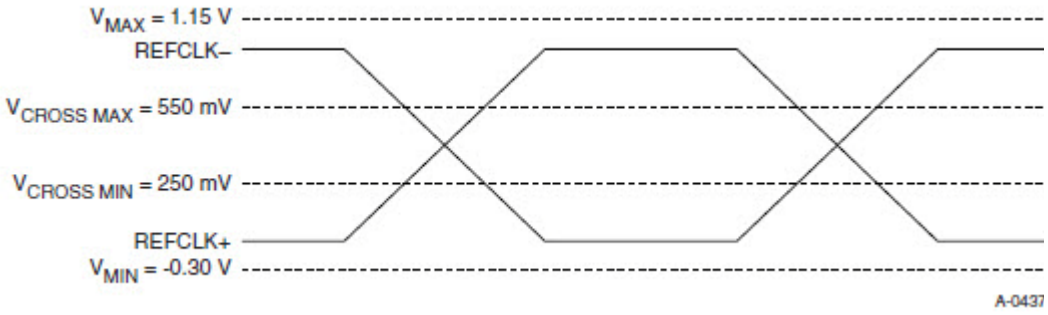


Figure 127 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in section 4.2.8 of the PCI Express Base Specification, To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Absolute Crossing Point Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Uses MATLAB function to find the absolute crossing point voltage. The MATLAB function does the following:

   a Finds crossing edges for rising and falling edges.

   b Finds delta crossing for rising edge of RefClk+ and falling edge of RefClk-.

4 Computes the margin for minimum crossing point voltage and margin of maximum crossing point voltage.

5 Compares the margin and choose the smallest margin to report the value (worst value) as absolute crossing point voltage.

6 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as `250mV ≤ Absolute Crossing Point Voltage ≤ 550mV`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Variation of V_{Cross} Test

The variation of V_{Cross} test is measured at crossing point where the instantaneous voltage value of the rising edge of Refclk+ equals the falling edge of Refclk-. It is defined as the total variation of all voltages of rising Refclk+ and falling Refclk-.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 76 Variation of V_{CROSS} Test Details

Symbol	Parameter	Max
V_{CROSS} Delta	Variation of V_{CROSS} over all rising clock edges	+140mV

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 2-3.
- Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 2-4.

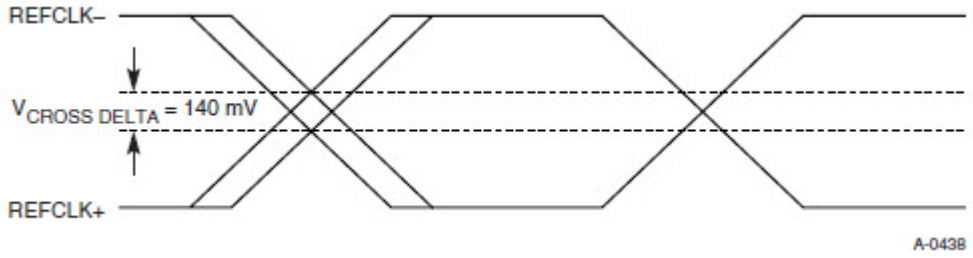


Figure 128 Single-Ended Measurement Points for Delta Cross Point

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Variation of VCross**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the absolute crossing point voltage test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Fits and displays all sample data on screen.

2 Uses MATLAB function to find the variation of V_{CROSS}. The MATLAB function does the following:

   a Finds crossing edges for rising and falling edges.

   b Finds delta crossing for rising edge of RefClk+ and falling edge of RefClk- .

3 Finds the differential value between maximum crossing rising edge and minimum crossing rising edge as variation of V_{Cross}.

4 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as variation of V_{Cross} < 140mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Max Input Voltage Test

The absolute max input voltage test verifies that the reference clock average clock period is within the conformance limits specified in Table 2-1 of the PCI Express CEM Specifications v1.1.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 77 Absolute Max Input Voltage Test Details

Symbol	Parameter	Max
V_{MAX}	Absolute Max Input Voltage	+1.15V

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Defined as the maximum instantaneous voltage including overshoot. See Figure 2-3.

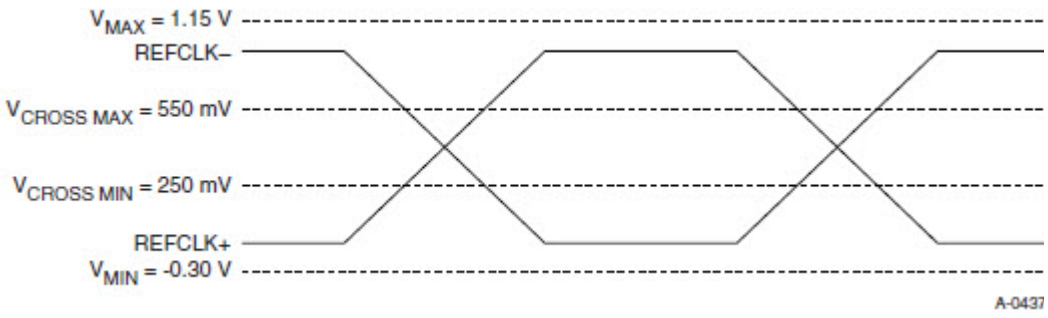


Figure 129 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Absolute Max Input Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the **Sample Rate** to 20GSa/s and **Memory Depth** to 1Mpts using **Acquisition Setup**.

3 Fits and displays all sample data on screen.

4 Turns on the **Measurement Analysis (EZJIT)** and checks **Measure All Edges**.

5 Measures the RefClk+ maximum voltage using **V max** measurement.

6 Measures the RefClk- maximum voltage using **V max** measurement.

7 Compares the RefClk+ maximum voltage and the RefClk- maximum voltage.

8 Reports the largest value (worst value) as the Absolute Max Input Voltage.

9 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as variation of V_{MAX} < +1.15V.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

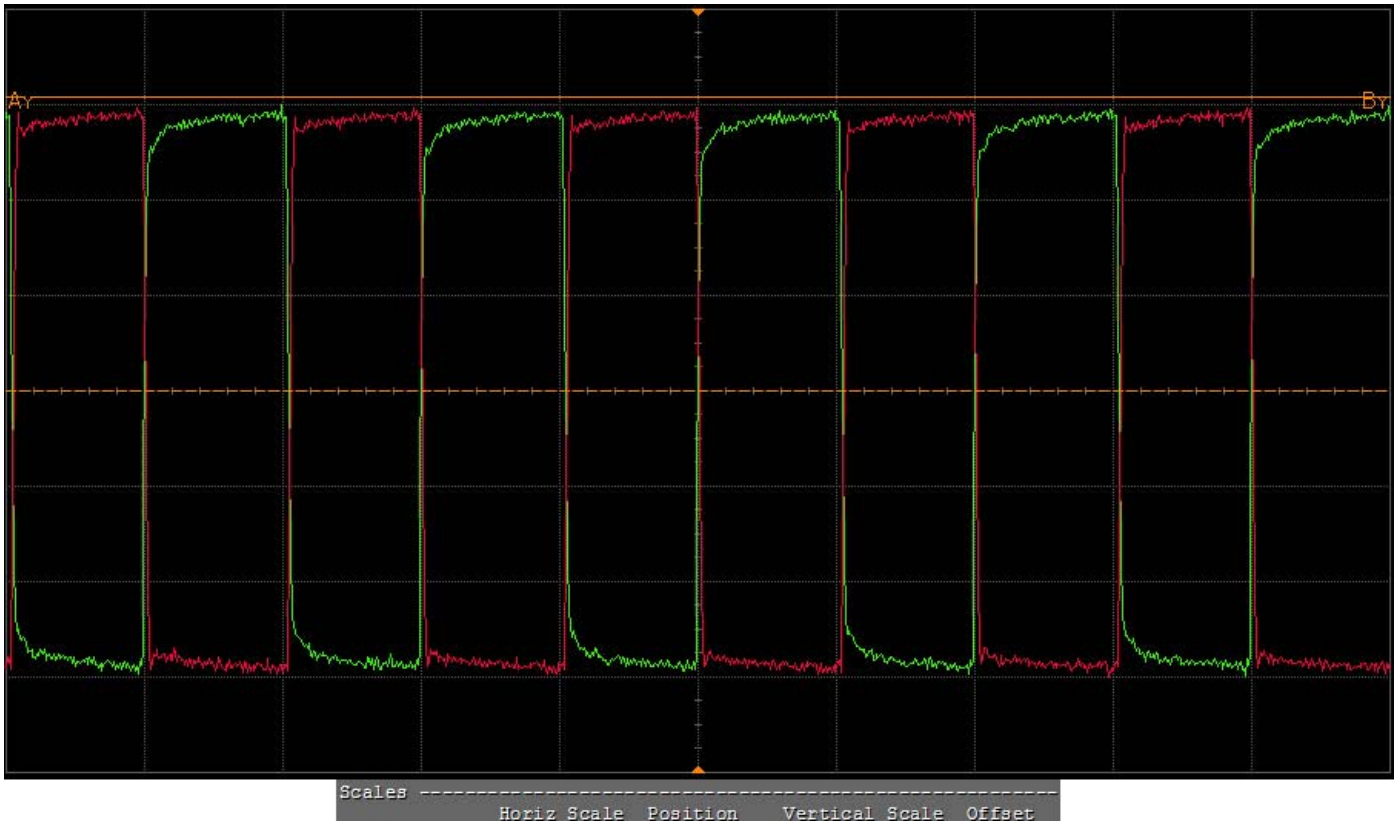


Figure 130 Reference Image for Absolute Max Input Voltage Test

Absolute Min Input Voltage Test

The absolute min input voltage test verifies that the reference clock average clock period is within the conformance limits specified in Table 2-1 of the PCI Express CEM Specifications v1.1.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 78 Absolute Min Input Voltage Test Details

Symbol	Parameter	Max
V_{MIN}	Absolute Min Input Voltage	-0.3V

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Defined as the minimum instantaneous voltage including undershoot. See Figure 2-3.

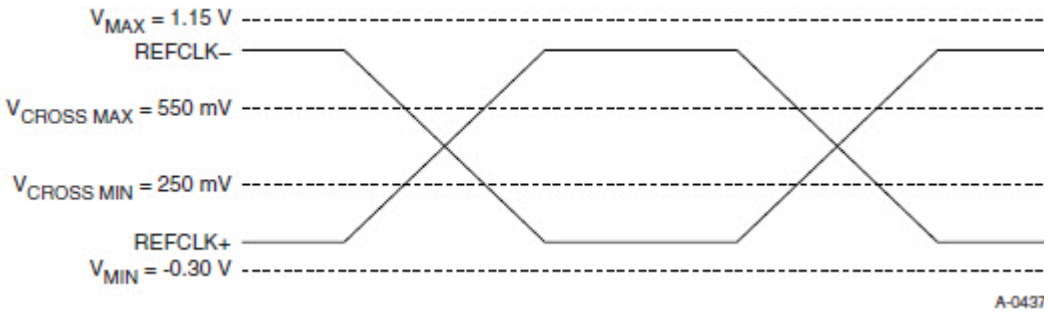


Figure 131 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Absolute Min Input Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the **Sample Rate** to 20GSa/s and **Memory Depth** to 1Mpts using **Acquisition Setup**.

3 Fits and displays all sample data on screen.

4 Turns on the **Measurement Analysis (EZJIT)** and checks **Measure All Edges**.

5 Measures the RefClk+ minimum voltage using **V min** measurement.

6 Measures the RefClk- minimum voltage using **V min** measurement.

7 Compares the RefClk+ minimum voltage and the RefClk- minimum voltage.

8 Reports the smallest value (worst value) as the Absolute Min Input Voltage.

9 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as variation of V_{MIN} < -0.3V.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

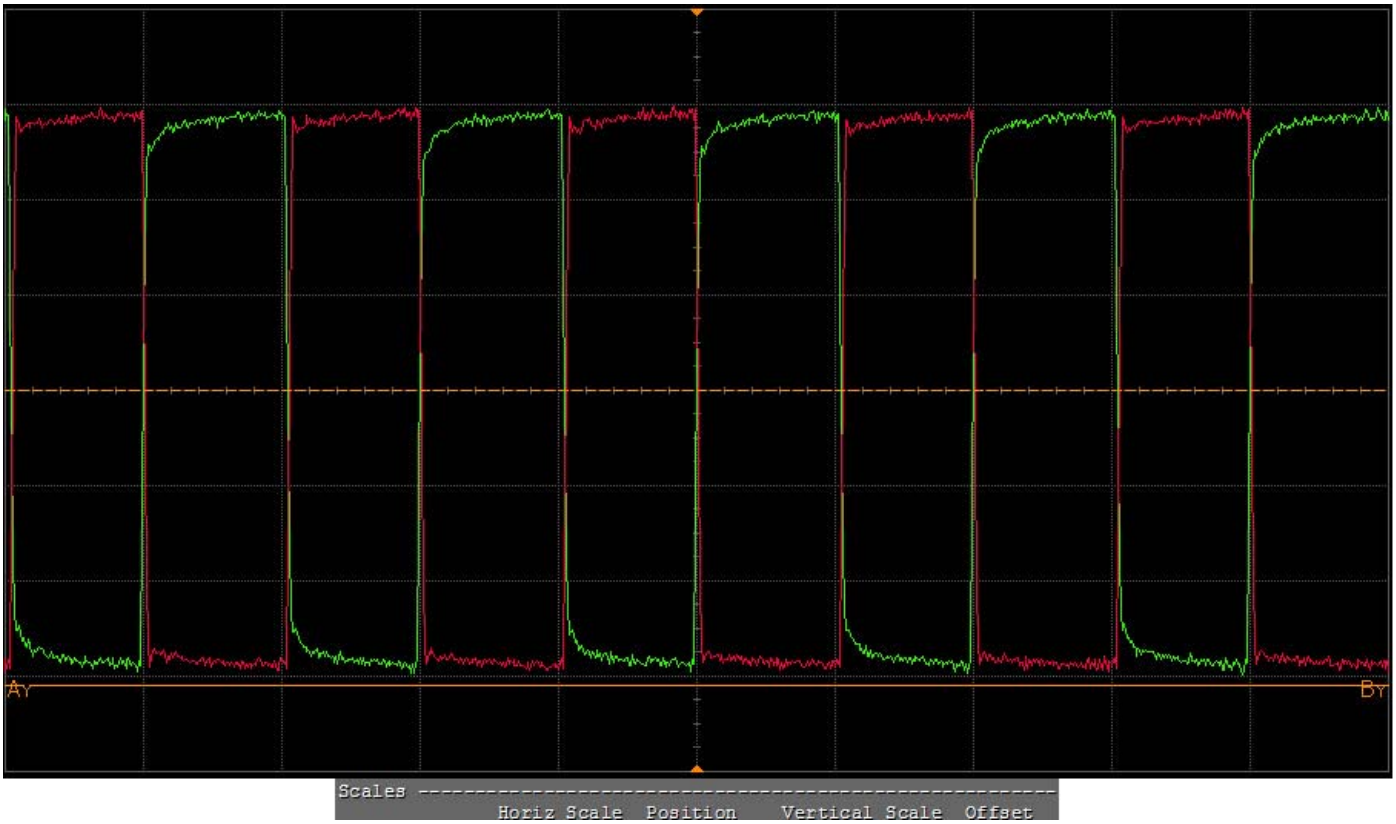


Figure 132 Reference Image for Absolute Min Input Voltage Test

Rise-Fall Matching Test

The rise-fall matching test matching applies to rising edge rate for RefClk+ and falling edge rate for RefClk-. It is measured using +/-75mV window centered on the median cross point where RefClk+ rising meets RefClk- falling. The median cross point is used to calculate the voltage thresholds and oscilloscope is used to calculate the edge rate calculations. The rise edge rate of RefClk+ should be compared to the fall edge rate of RefClk-, the maximum allowed difference should not exceed 20% of the slowest edge rate.

Test Reference

PCI Card Electromechanical Specification Rev. 1.1, Section 2.1.3, Table 2-1 is used as reference to check the compliance of the DUT.

Table 79 Rise-Fall Matching Test Details

Symbol	Parameter	Max
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching	-20%

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a +-75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 2-5.

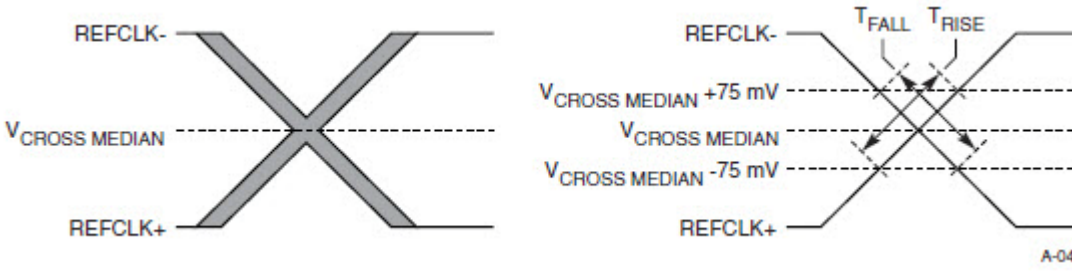


Figure 133 Single-Ended Measurement Points for Rise and Fall Time Matching

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Reference Clock Tests" on page 238 and select **Rise-Fall Matching**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the absolute crossing point voltage test with the following specifications:

Device: PCIE1.1

Data Rate: 2.5GT/s

1 Configures the **Sample Rate** to 20GSa/s and **Memory Depth** to 1Mpts using **Acquisition Setup**.

2 Fits and displays all sample data on screen.

3 Sets the Middle Threshold by ([maximum crossing rising edge value +minimum crossing rising edge value] / 2).

4 Sets the **Upper Level** of **Custom Thresholds** as **Middle Level** of **Custom Thresholds** + 75mV].

5 Sets the **Lower Level** of **Custom Thresholds** as **Middle Level** of **Custom Thresholds** - 75mV].

6 Measures RefClk+ rise time using **Rise time** measurement.

7 Measures the RefClk- fall time using **Fall time** measurement.

8 Finds the slowest edge between RefClk+ rise time and RefClk- fall time.

9 Computes the Rise-Fall matching value as follows:

$$\text{.Rise-Fall Matching} = \frac{Abs|\text{RefClk+ rise time} - \text{RefClk- fall time}|}{\text{Slowest Edge Value} \times 100}$$

10 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as variation of `Rise-Fall Matching < 20%.`

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

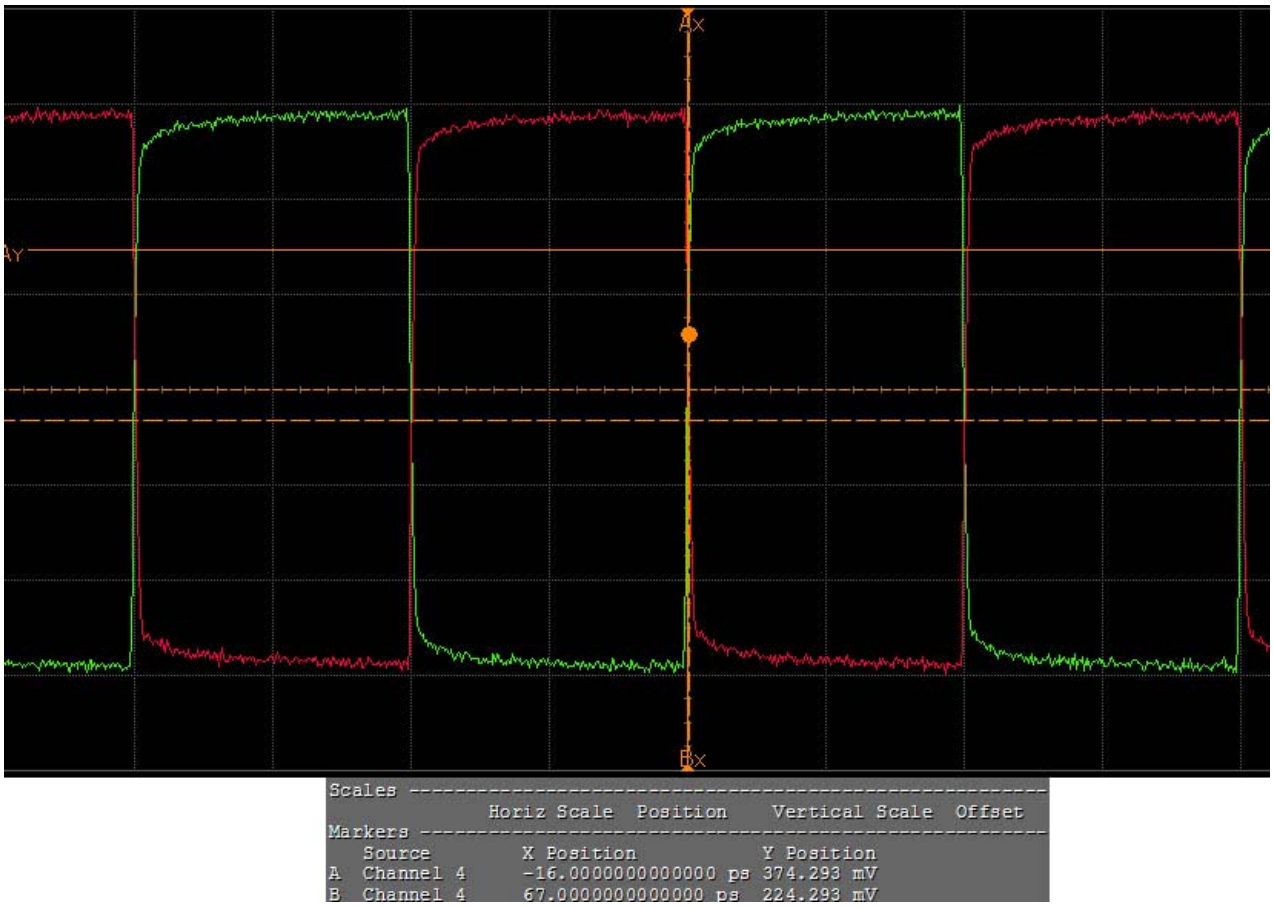


Figure 134 Reference Image for Rise-Fall Matching

Part IV
2.5 GT/s PCI Express Version 2.0

Agilent Technologies

Part IV

14 Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 2.0, Full Power

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Tx Compliance

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Base Specification) will be transmitted.

Table 80 Probing Options for Transmitter Testing

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended SMA Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

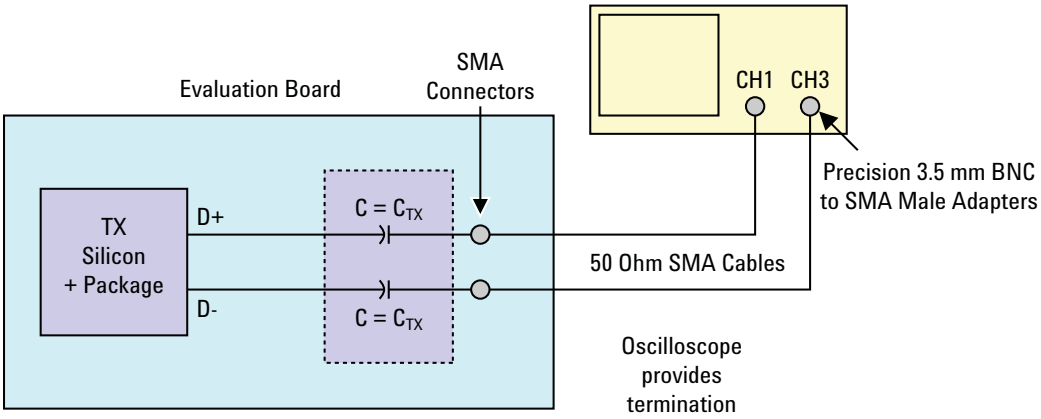


Figure 135 Single-Ended SMA Probing

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

For more information on the probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

Place single-ended grounds as close to the signal line’s reference ground as possible.

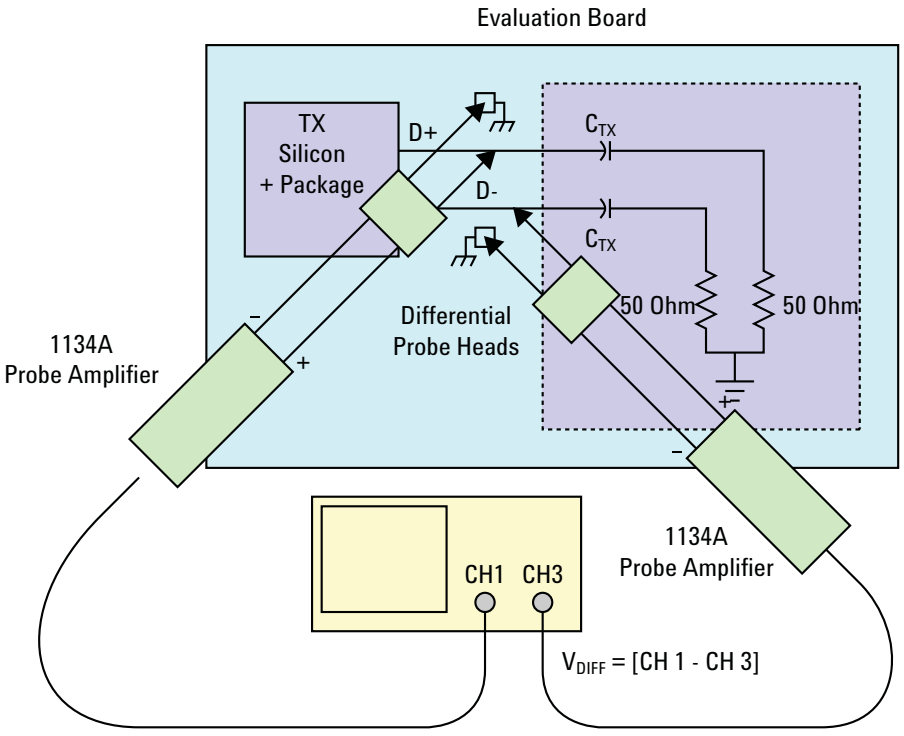


Figure 136 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

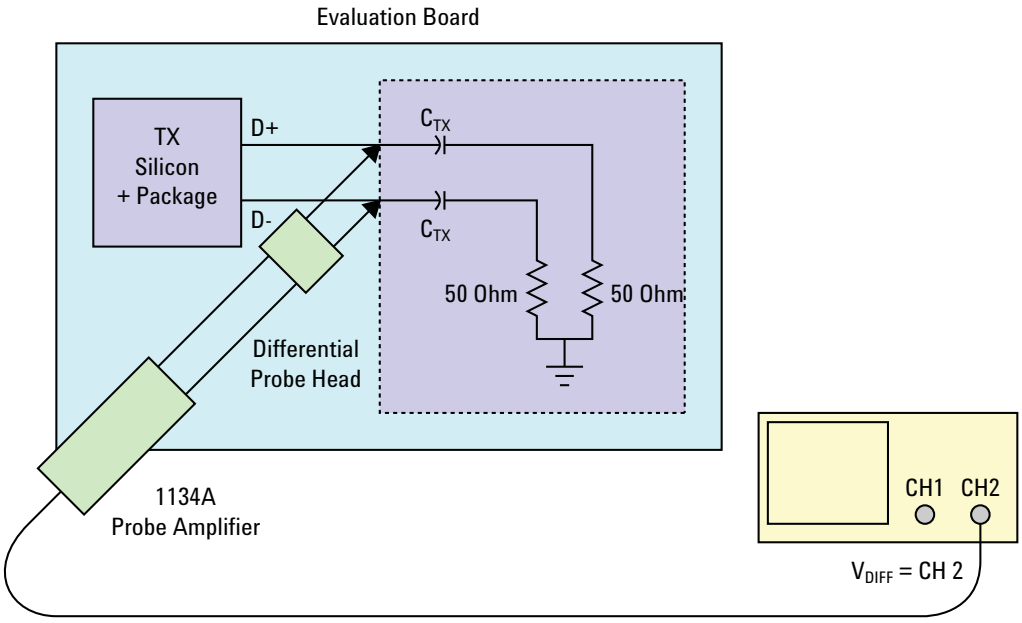


Figure 137 Differential Probing

Tx Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification)

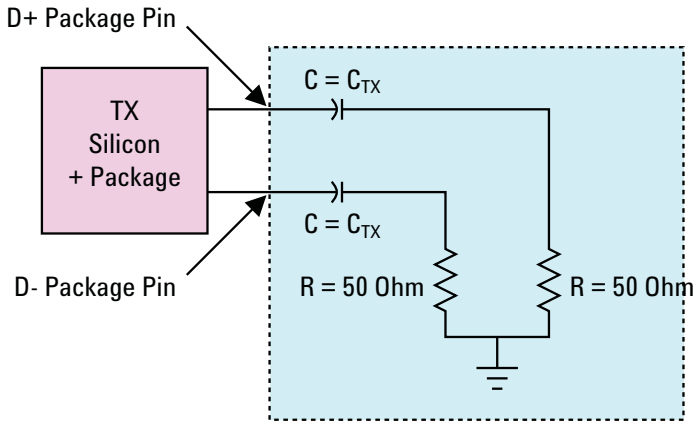


Figure 138 Driver Compliance Test Load.

Running Signal Quality Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to "Signal Quality" in the "Transmitter (Tx) Tests" group.

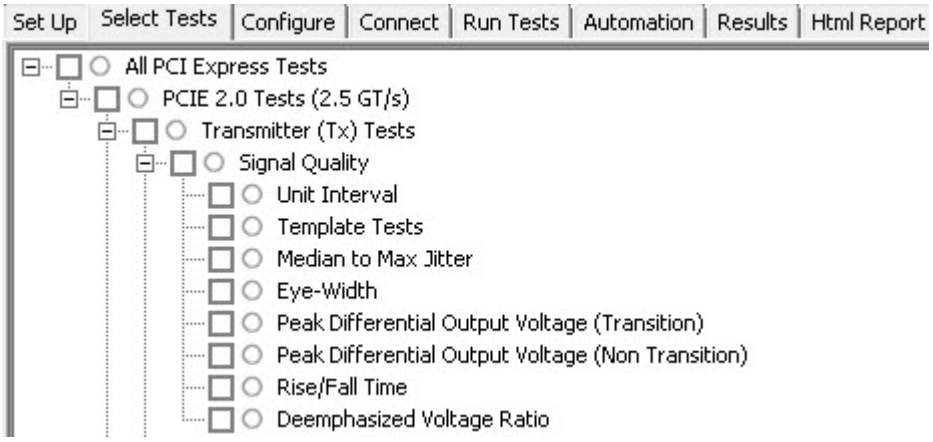


Figure 139 Selecting Transmitter (Tx) Signal Quality Tests

Unit Interval Test

When performing PCIE 2.0 transmitter tests, the **Unit Interval** test is same as PCIE 1.0 transmitter tests. See "Unit Interval Test" on page 39.

Template Tests

When performing PCIE 2.0 transmitter tests, the **Template** test is same as PCIE 1.0 transmitter tests. See "Template Test" on page 41.

Median to Max Jitter Test

When performing PCIE 2.0 transmitter tests, the **Median to Max Jitter** test is same as PCIE 1.0 transmitter tests. See "Median to Max Jitter Test" on page 45.

Eye-Width Test

When performing PCIE 2.0 transmitter tests, the **Eye-Width** test is same as PCIE 1.0 transmitter tests. See "Eye-Width Test" on page 46.

Peak Differential Output Voltage (Transition) Test

When performing PCIE 2.0 transmitter tests, the **Peak Differential Output Voltage** test is same as PCIE 1.0 transmitter tests. See "Peak Differential Output Voltage (Transition) Test" on page 48.

Peak Differential Output Voltage (Non-transition) Test

When performing PCIE 2.0 transmitter tests, the **Peak Differential Output Voltage (Non-transition)** test is same as PCIE 1.0 transmitter tests. See "Peak Differential Output Voltage (Transition) Test" on page 48.

Rise/Fall Time

When performing PCIE 2.0 transmitter tests, the **Rise/Fall Time** test is same as PCIE 1.0 transmitter tests. See "Rise/Fall Time Test" on page 53.

De-emphasized Voltage Ratio Test

When performing PCIE 2.0 transmitter tests, the **De-emphasized Voltage Ratio** test is same as PCIE 1.0 transmitter tests. See "Deemphasized Voltage Ratio Test" on page 57.

Running Common Mode Voltage Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to “Common Mode Voltage” in the “Transmitter (Tx) Tests” group.

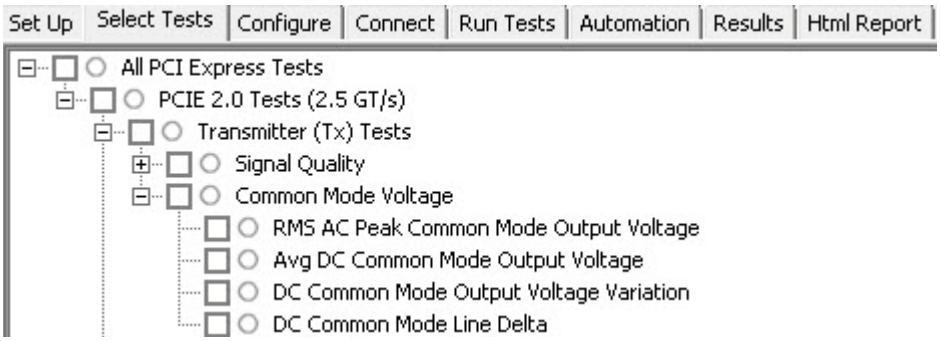


Figure 140 Selecting Transmitter (T_x) Common Mode Voltage Tests

RMS AC Peak Common Mode Output Voltage

When performing PCIE 2.0 transmitter tests, the **RMS AC Peak Common Mode Output Voltage** test is same as PCIE 1.0 transmitter tests. See “RMS AC Peak Common Mode Output Voltage Test" on page 61.

Avg DC Common Mode Output Voltage

When performing PCIE 2.0 transmitter tests, the **Average DC Common Mode Output Voltage** test is same as PCIE 1.0 transmitter tests. See “Avg DC Common Mode Output Voltage Test" on page 63.

DC Common Mode Output Voltage Variation

When performing PCIE 2.0 transmitter tests, the **DC Common Mode Output Voltage Variation** test is same as PCIE 1.0 transmitter tests. See “DC Common Mode Output Voltage Variation Test" on page 66.

DC Common Mode Line Delta

When performing PCIE 2.0 transmitter tests, the **DC Common Mode Line Delta** test is same as PCIE 1.0 transmitter tests. See “DC Common Mode Line Delta Test" on page 68.

15 Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 2.0, Low Power

This section provides the Methods of Implementation (MOIs) for Transmitter tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

The PCIe 2.0 base specification describes the Low Power specification as optional. From “4.3.3.2. Low and Full Swing Transmitter Output Levels”:

> Both the 2.5 GT/s and 5.0 GT/s PCI Express specifications define two voltage swing levels: full swing and low swing. Full swing signaling implements de-emphasis, while low swing does not. Typically, low swing is specified for power sensitive applications where a shorter channel is acceptable. The requirement as to whether a Transmitter need support full swing, low swing, or both modes, is dependent on its usage model. The method by which the output mode is selected is not explicitly defined in this specification, and may be implementation dependent. Note: All PCI Express device Transmitters must support full swing signaling, while support for half swing signaling is optional.
>
> While two different Transmitter output signaling levels are defined, only a single Receiver specification is defined; this implies that margins (as specified at the Receiver) are identical regardless of the Transmitter's output swing capabilities. It also implies that the channel’s characteristics need to be matched to the Transmitter output swing. Typically, low swing output is utilized for short channels, such as would occur in mobile platforms.

PCIe 2.0 Low Power Transmitter Tests consist of all tests from PCIe 2.0 Full (Standard) Power Tests except de-emphasis Tests. The following table shows all the PCIe 2.0 Low Power Tests:

Table 81 PCIE 2.0 Low Power Transmitter Tests

Test Name	Remarks	See
Unit Interval	Same as Full Power	page 277.
Template Tests	Different	page 277.
Median to Max Jitter	Different	page 277.
Eye-Width	Different	page 277.
Peak Differential Output Voltage	Different	page 277.
Rise/Fall Time	Same as Full Power	page 277.
RMS AC Peak Common Mode Output Voltage	Same as Full Power	page 277.
Avg DC Common Mode Output Voltage	Same as Full Power	page 278.
DC Common Mode Output Voltage Variation	Same as Full Power	page 278.
DC Common Mode Line Delta	Same as Full Power	page 278.

All the tests above remarked with “Same as Full Power” share the same Method of Implementation (MOI) with PCIE 2.0 Full Power (refer to the page numbers shown). The differences in the test method are described in this chapter.

Probing the Link for Tx Compliance

When performing low-power transmitter tests, probing is the same as for full-power tests. See “Probing the Link for Tx Compliance" on page 272.

Tx Compliance Test Load

When performing low-power transmitter tests, the compliance test load is the same as for full-power tests. See “Tx Compliance Test Load" on page 276.

Running Signal Quality Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to “Signal Quality” in the “Transmitter (Tx) Tests” group.

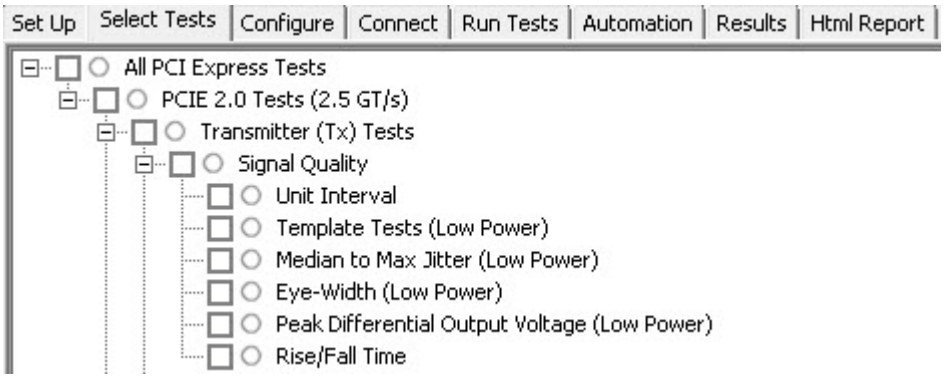


Figure 141 Selecting Transmitter (Tx) Signal Quality Tests

Unit Interval Test

When performing low-power transmitter tests, the **Unit Interval** test is the same as for full-power tests. See "Unit Interval Test" on page 277.

Template Tests (Low Power)

Test Definition/Reference

PCIE base specification 2.0 section 4.3.3.5.

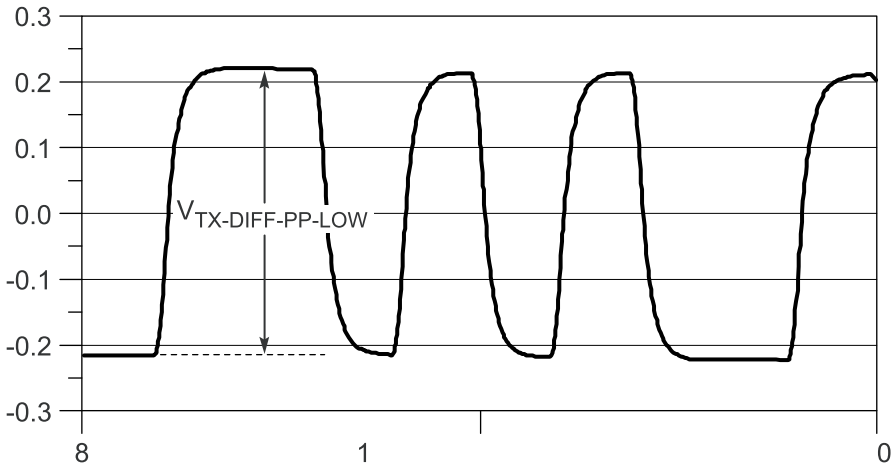


Figure 142 Low Swing Tx Parameters, Figure 4-27 in Base Specification v2.0

Difference in Test Procedure Compared to Full Power

- Different Eye diagram used. The Eye diagram can be found in Figure 2.2 of Mobile Low Power PCIE Specification.

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also

"Template Tests" on page 277.

Median to Max Jitter (Low Power) Test

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also

"Median to Max Jitter Test" on page 277.

Eye-Width (Low Power) Test

Difference in Test Procedure Compared to Full Power

- Eye diagram only runs once with both transition and non-transition bits since de-emphasis is no longer needed for low power specification.

See Also

"Eye-Width Test" on page 277.

Peak Differential Output Voltage (Low Power) Test

Difference in Test Procedure Compared to Full Power

- Different specification used:

Table 82 Peak Differential Output Voltage from Table 4-9 of the Base Specification: 2.5 and 5.0 GT/s Transmitter Specifications

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$T_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	As measured with compliance test load. Defined as $2^* \mid V_{TXD+} - V_{TXD-} \mid$.

- Low swing output, defined by VTX-DIFF-PP-LOW must be implemented as shown in Figure 4-27 (Base Specification) with no de-emphasis.

See Also

"Peak Differential Output Voltage (Transition) Test" on page 277.

Rise/Fall Time

When performing low-power transmitter tests, the Tx Rise/Fall Time test is the same as for full-power tests. See “Rise/Fall Time" on page 277.

Running Common Mode Voltage Tests

When performing low-power transmitter tests, the common mode voltage tests are the same as for full-power tests. See “Running Common Mode Voltage Tests" on page 278.

16
Receiver (Rx) Tests, 2.5 GT/s, PCI-E 2.0

This section provides the Methods of Implementation (MOIs) for Receiver tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

NOTE

None of the included receiver tests validate the receiver's ability to correctly receive data (also known as receiver tolerance). Rather, they validate that the signal as seen by the receiver meets or exceeds various parameters (maximum voltage, jitter, eye width, etc.). These tests validate the transmitter and interconnect. Separate receiver tolerance testing is required to ensure the receiver is correctly receiving data.

Probing the Link for Rx Compliance

Receiver tests are done by probing the link as close as is feasibly possible to the pins of the receiver device. Alternatively, a dummy load can be used for the termination of the link. To probe the receiver link, you can:

- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

Table 83 Probing Options for Receiver Testing

	Probing Configurations			Captured Waveforms	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**
DUT Connection	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 - Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

Channel-to-channel deskew is required using this technique because two channels are used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

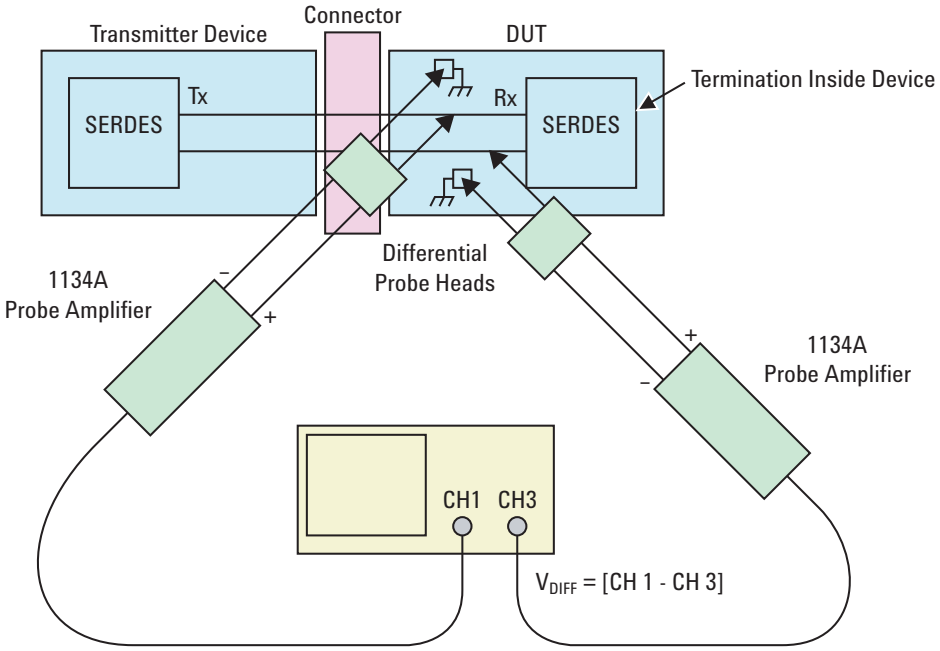


Figure 143 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

A single channel of the oscilloscope is used, so de-skew is not necessary.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

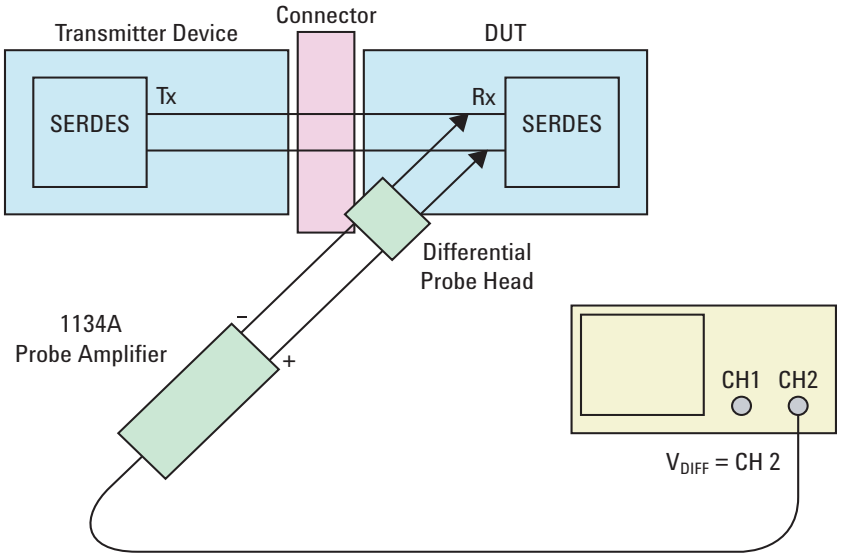


Figure 144 Differential Probing

Running Receiver Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the “Receiver (Rx) Tests” group.

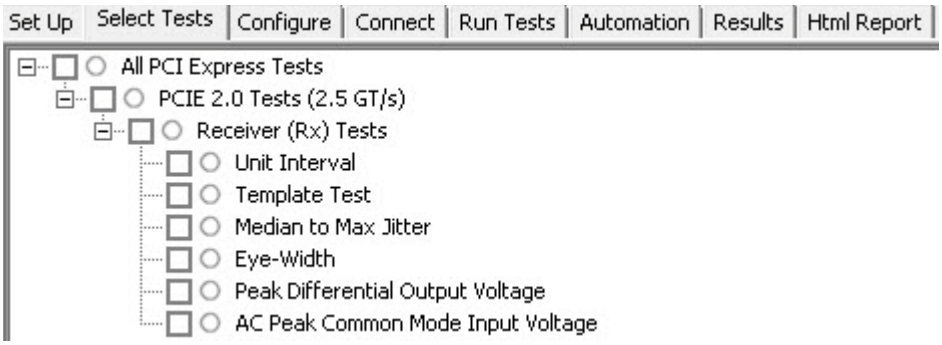


Figure 145 Selecting Receiver (Rx) Tests

Unit Interval

When performing PCIE 2.0 receiver tests, the **Unit Interval** test is same as PCIE 1.0 receiver tests. See “Unit Interval Test" on page 81.

Template Test

When performing PCIE 2.0 receiver tests, the **Template** test is same as PCIE 1.0 receiver tests. See “Template Test" on page 83.

Median to Max Jitter Test

When performing PCIE 2.0 receiver tests, the **Median to Max Jitter** test is same as PCIE 1.0 receiver tests. See “Median to Max Jitter Test" on page 87.

Eye-Width Test

When performing PCIE 2.0 receiver tests, the **Eye-Width** test is same as PCIE 1.0 receiver tests. See “Eye-Width Test" on page 88.

Peak Differential Output Voltage Test

When performing PCIE 2.0 receiver tests, the **Peak Differential Output Voltage** test is same as PCIE 1.0 receiver tests. See “Peak Differential Output Voltage Test" on page 89.

AC Peak Common Mode Input Voltage Test

When performing PCIE 2.0 receiver tests, the **AC Peak Common Mode Input Voltage** test is same as PCIE 1.0 receiver tests. See “AC Peak Common Mode Input Voltage Test" on page 91.

17
Add-In Card (Tx) Tests, 2.5 GT/s, PCI-E 2.0

This section provides the Methods of Implementation (MOIs) for Add-In Card Transmitter tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Add-In Card Compliance

Connecting the Signal Quality Load Board for Add-in Card Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 or by-1 connector slot.

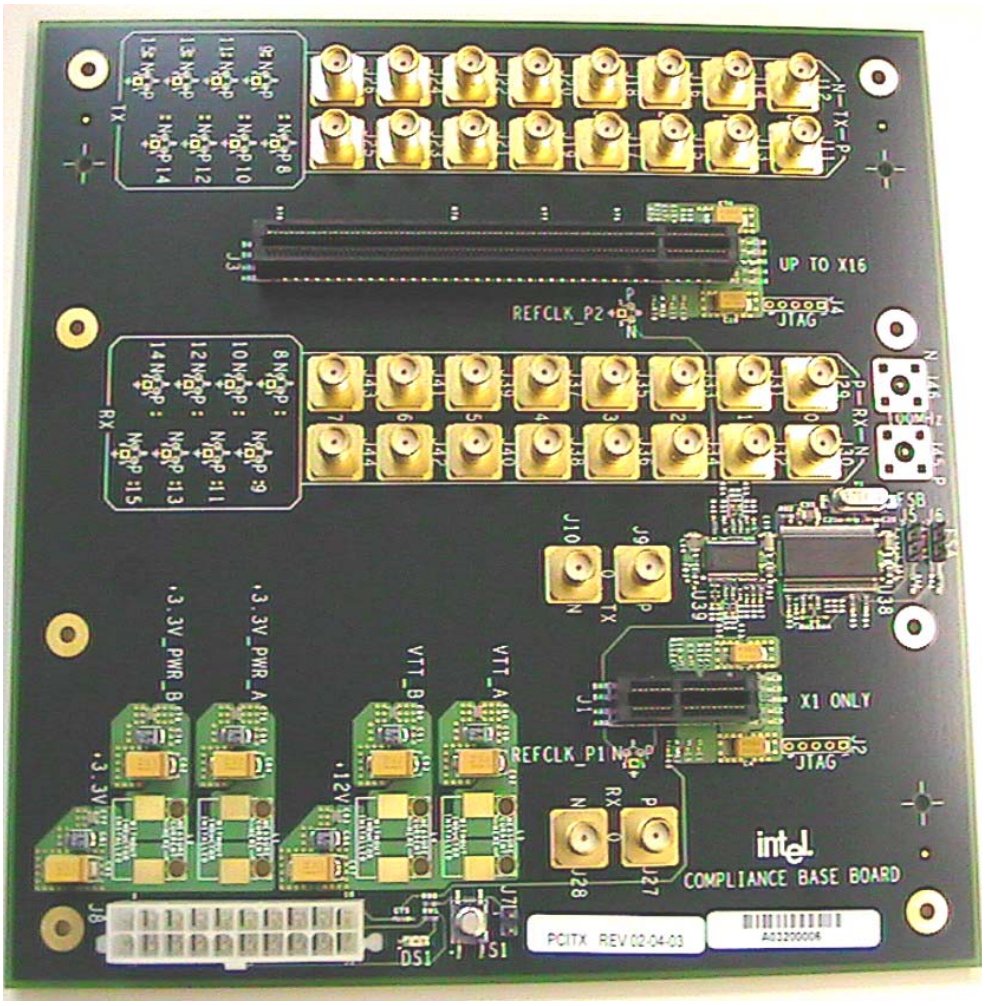


Figure 146 Compliance Base Board (CBB) Add-in Card Fixture

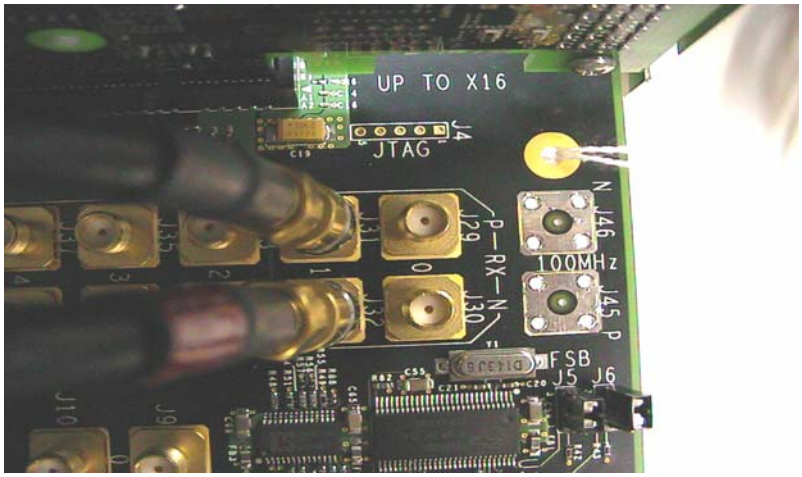


Figure 147 Compliance Base Board (CBB) SMA Probing Option

2 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the TX LANE P under test (where Lane 1 is under test in this example shown in Figure 147 above).

   b Digital Storage Oscilloscope channel 3 to the TX LANE N under test (where Lane 1 is under test in this example shown in Figure 147 above).

NOTE The Compliance Base Board labeled PCITX Rev 02-04-03 silk screen incorrectly labels the add-in card transmitter probing locations as RX.

When SMA probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 626).

Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 148 on page 294). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

3 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

4 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

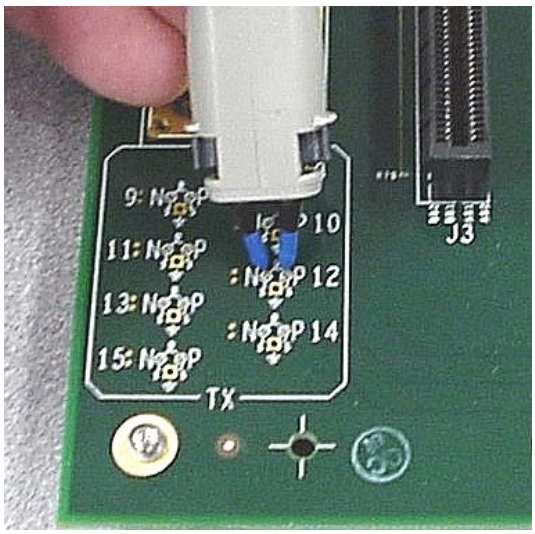


Figure 148 Compliance Base Board (CBB) Active Probing Option

Running Add-In Card Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the “Add-In Card (Tx) Tests” group.

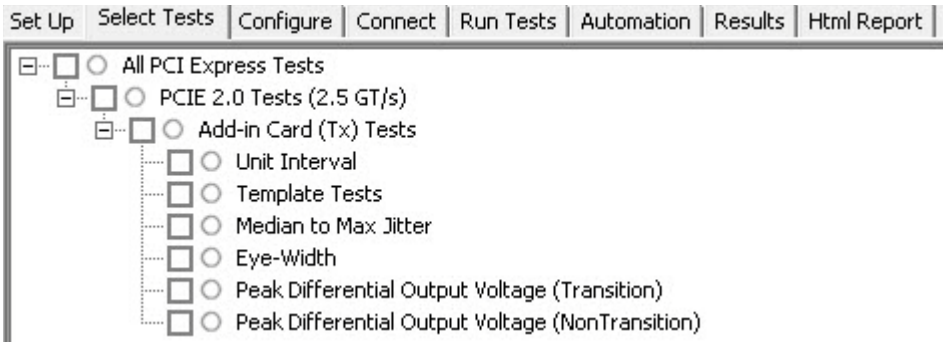


Figure 149 Selecting Add-In Card (Tx) Tests

Unit Interval Test

When performing PCIE 2.0 add-in card tests, the **Unit Interval** test is same as PCIE 1.0 add-in card tests. See “Unit Interval Test" on page 99.

Template Tests

When performing PCIE 2.0 add-in card tests, the **Template** test is same as PCIE 1.0 add-in card tests. See “Template Test" on page 101.

Median to Max Jitter Test

When performing PCIE 2.0 add-in card tests, the **Median to Max Jitter** test is same as PCIE 1.0 add-in card tests. See “Median to Max Jitter Test" on page 105.

Eye-Width Test

When performing PCIE 2.0 add-in card tests, the **Eye-Width** test is same as PCIE 1.0 add-in card tests. See “Eye-Width Test" on page 107.

Peak Differential Output Voltage (Transition) Test

When performing PCIE 2.0 add-in card tests, the **Peak Differential Output Voltage (Transition)** test is same as PCIE 1.0 add-in card tests. See “Peak Differential Output Voltage Test" on page 109.

Peak Differential Output Voltage (Non-Transition) Test

When performing PCIE 2.0 add-in card tests, the **Peak Differential Output Voltage (Non-Transition)** test is same as PCIE 1.0 add-in card tests. See “Peak Differential Output Voltage Test" on page 109.

18 System Board (Tx) Tests, 2.5 GT/s, PCI-E 2.0

This section provides the Methods of Implementation (MOIs) for System Board Transmitter tests using an Agilent 90000X series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for System Board Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMA connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The PCI Express Signal Quality Load Board has edge fingers for x1, x4, x8 and x16 connectors.

   The PCI Express Signal Quality Load Board will cause a PCI Express 1.1 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

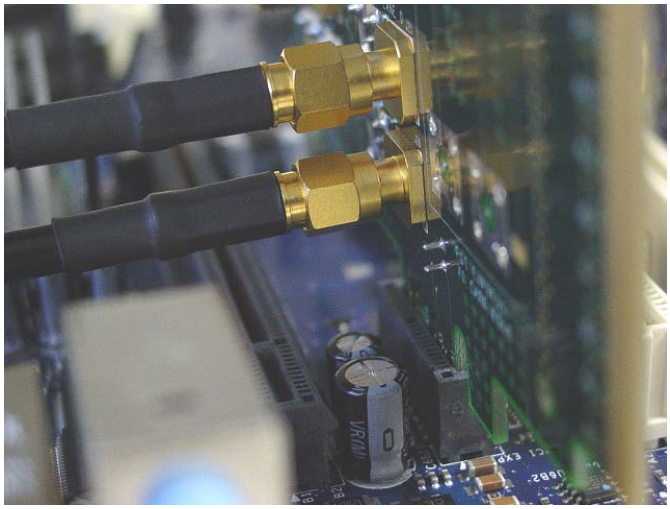


Figure 150 SMA Probing Option

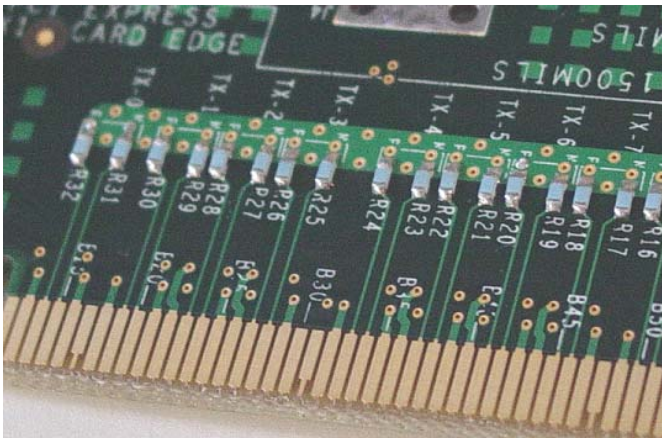


Figure 151 Resistor Terminations for Lanes without SMA Probing

2 Connect cables up as follows:

a Digital Storage Oscilloscope channel 1 to TX LANE 1 P (where Lane 1 is under test).

b Digital Storage Oscilloscope channel 3 to TX LANE 1 N (where Lane 1 is under test).

When SMA probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 626).

Not all lanes have SMA probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes (see Figure 85 on page 194). For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the 1134A probe amplifier.

When using a single differential probe head, use oscilloscope channel 2.

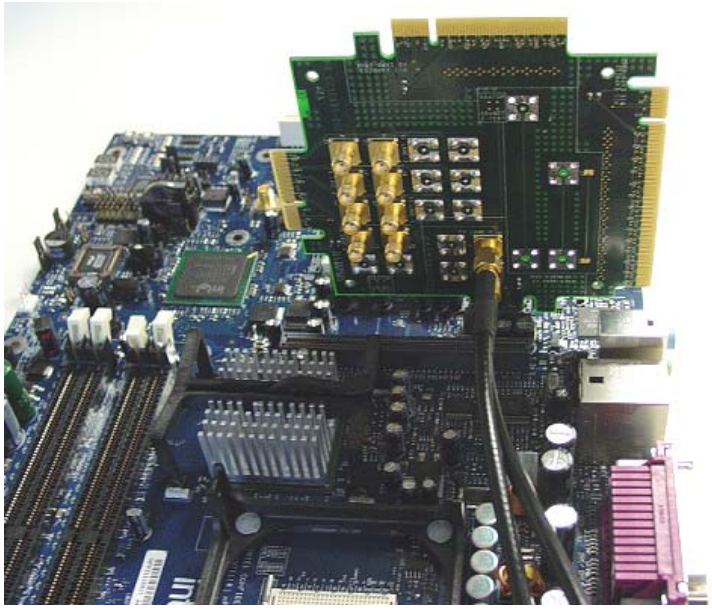


Figure 152 Connecting the PCI Express Signal Quality Test Fixture

Running System Board Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the “System Board (Tx) Tests” group.

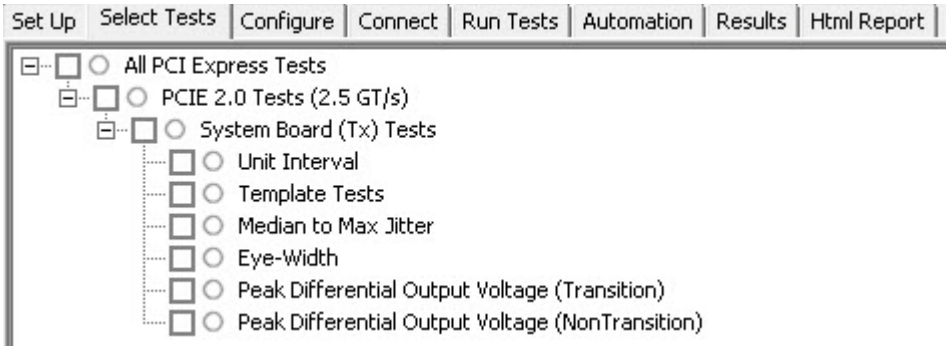


Figure 153 Selecting System Board (Tx) Tests

Unit Interval Test

When performing PCIE 2.0 system board tests, the **Unit Interval** test is same as PCIE 1.0 system board tests. See “Unit Interval Test" on page 116.

Template Tests

When performing PCIE 2.0 system board tests, the **Template** test is same as PCIE 1.0 system board tests. See “Template Test" on page 118.

Median to Max Jitter Test

When performing PCIE 2.0 system board tests, the **Median to Max Jitter** test is same as PCIE 1.0 system board tests. See “Median to Max Jitter Test" on page 122.

Eye-Width Test

When performing PCIE 2.0 system board tests, the **Eye-Width** test is same as PCIE 1.0 system board tests. See “Eye-Width Test" on page 124.

Peak Differential Output Voltage (Transition) Test

When performing PCIE 2.0 system board tests, the **Peak Differential Output Voltage** test is same as PCIE 1.0 system board tests. See “Peak Differential Output Voltage Test" on page 126.

Peak Differential Output Voltage (Non-transition) Test

When performing PCIE 2.0 system board tests, the **Peak Differential Output Voltage (Non-transition)** test is same as PCIE 1.0 system board tests. See “Peak Differential Output Voltage Test" on page 126.

Part V
5.0 GT/s PCI Express Version 2.0

Agilent Technologies

Part V

19 Transmitter (T_x) Tests, 5.0 GT/s, PCI-E 2.0

This section provides the Methods of Implementation (MOIs) for Transmitter (Tx) 5.0 GT/s tests of PCI-E 2.0 using an Agilent 90000X series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Tx Compliance

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1169A probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of an oscilloscope that has 40 GS/s sample rate available on two channels.
- Use one differential probe head with the 1169A probe amplifier and the Ch2 input of an oscilloscope that has 40 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in Section 4.2.8 (Base Specification) will be transmitted.

Table 84 Probing Options for Transmitter Testing

	Probing Configurations			Captured Waveforms		System Specifications	
						90000X	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	12 GHz	70 ps
	Single-Ended (2 x 1169A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	12 GHz	70 ps
	Differential (1 x 1169A w/ Differential Probe Head)	Y/N	1	True	No	12 GHz	70 ps

*Typical

Single-Ended SMA Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel de-skew is required using this technique because two channels are used.

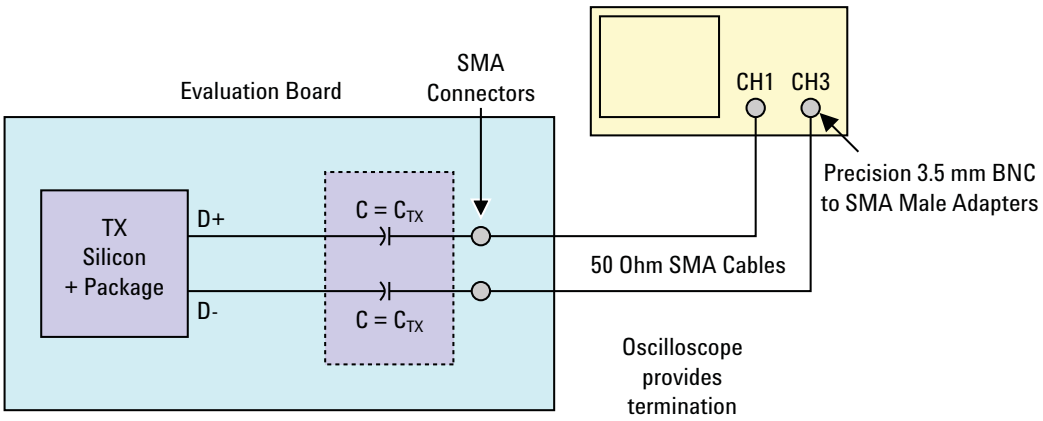


Figure 154 Single-Ended SMA Probing

Single-Ended Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel de-skew is required using this technique because two channels are used.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

Place single-ended grounds as close to the signal line's reference ground as possible.

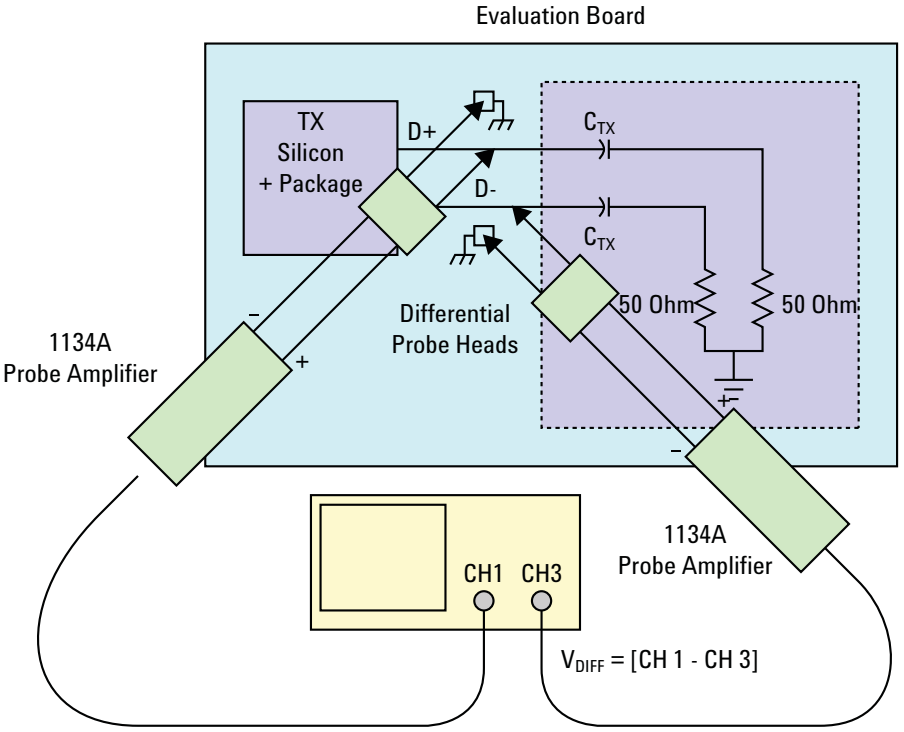


Figure 155 Single-Ended Probing

Differential Probing (Ch2)

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

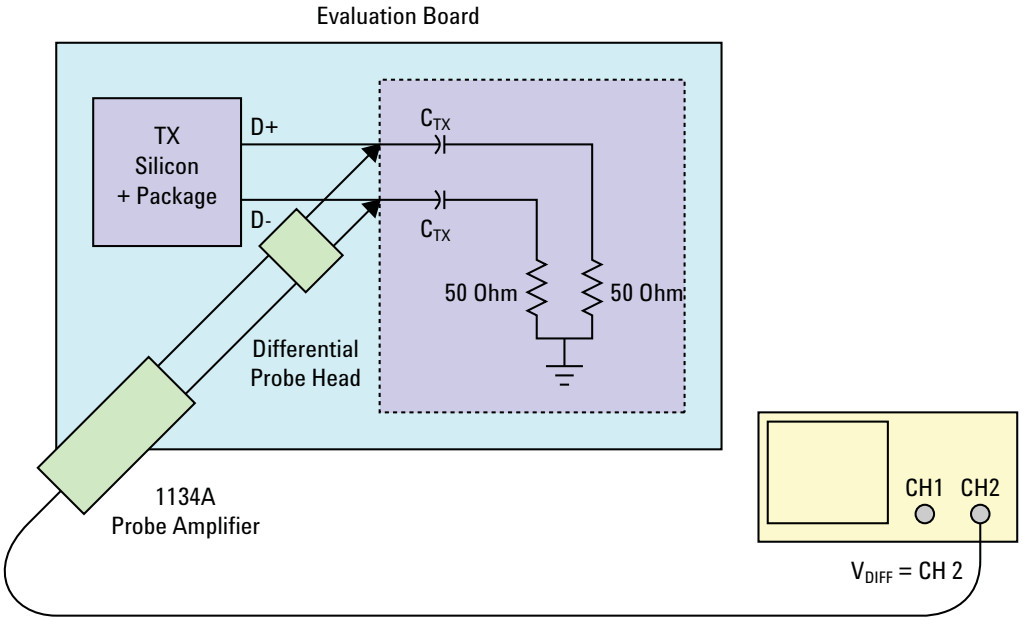


Figure 156 Differential Probing

Tx Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification)

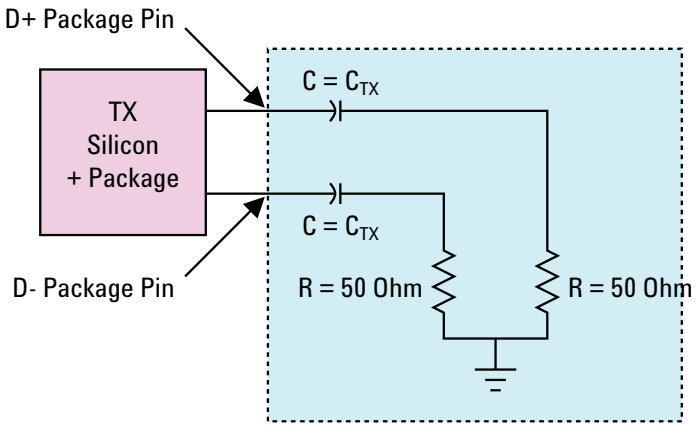


Figure 157 Driver Compliance Test Load.

Running T_x Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to "Transmitter (Tx) Tests" in the "PCIE 2.0 Tests" group.

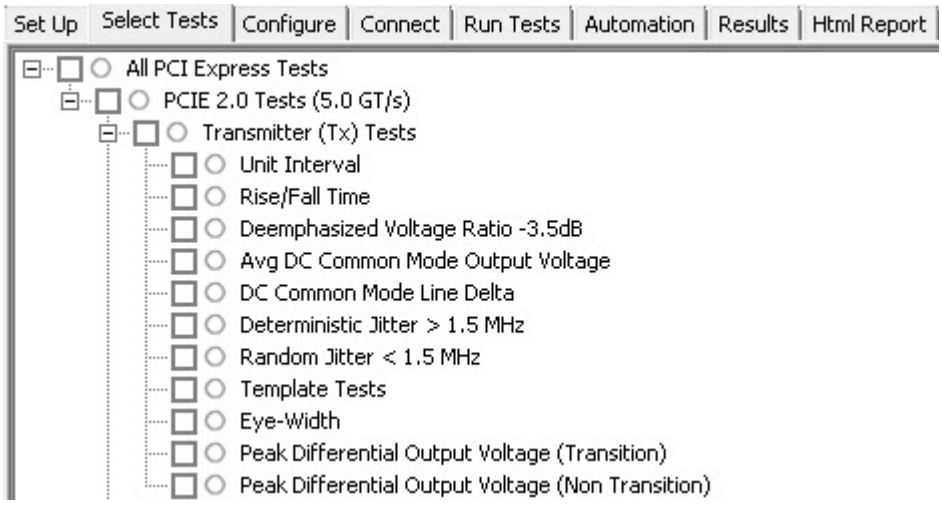


Figure 158 Selecting Transmitter (T_x) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 85 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	199.94 ps	200.06 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Tx Tests" on page 310 and select **Unit Interval**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.

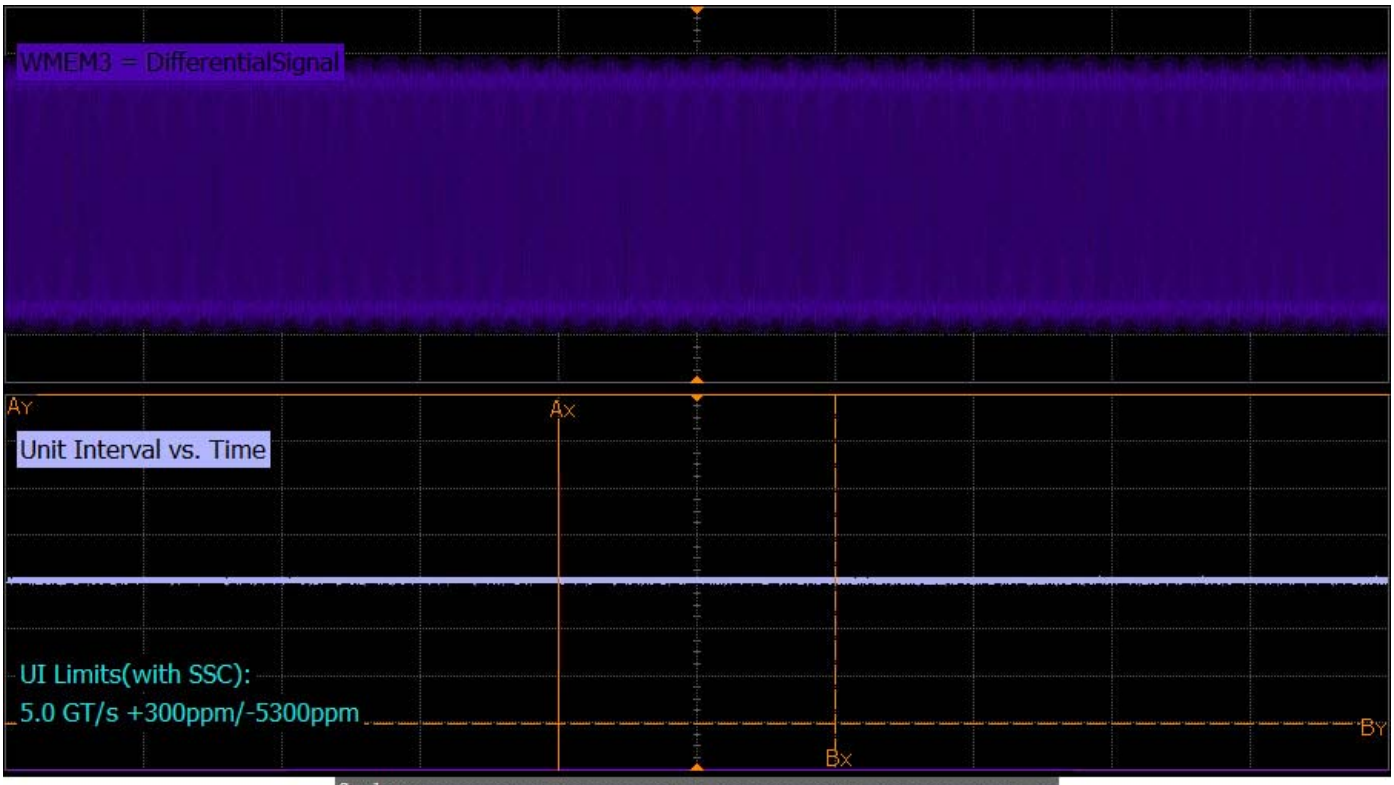
4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	32.00 µs/div	0.000s	20.00 fs/div	200.0 ps
Memory 3	32.00 µs/div	0.000s	183.8 mV/div	3.950 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-32.0000000000000 µs	200 pV
B	Function 3	32.0000000000000 µs	200 pV

Figure 159 Reference Image for Unit Interval Test

Rise/Fall Time Test

Rise/fall time is taken independently on each single ended waveform source when you use two single ended probes or two SMA cables as the signal source. Differential signal rise/fall time show up when you select differential probe type.

Rise Time. This measurement is the time difference of the values observed when the V_{REF-HI} and the V_{REF-LO} reference level are crossed on the rising edge of the waveform.

$$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$$

Where:

't_{RISE}' is a rise time measurement.

't_{HI+}' is a set of t_{HI} for rising edges only.

't_{LO+} is a set of t_{LO} for rising edges only.

'i' and 'j' are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}.

'n' is the index of rising edges in the waveform.

Rise time for $v_{D+}(t)$ is as follows:

$$t_{D+RISE}(n) = t_{D+HI+}(i) - t_{D+LO+}(j)$$

and for $v_{D-}(t)$:

$$t_{D-FALL}(n) = t_{D-LO-}(i) - t_{D-HI-}(j)$$

Fall Time. This measurement is the time difference of the values observed when the V_{REF-HI} and the V_{REF-LO} reference level are crossed on the falling edge of the waveform.

$$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$$

Where:

't_{FALL}' is a fall time measurement.

't_{HI-}' is set of t_{HI} for falling edge only.

't_{LO-}' is set of t_{LO} for falling edge only.

'i' and j' are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

'n' is the index of falling edges in the waveform.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 86 Rise/Fall Time Test Details

Symbol	Parameter	Min	Comments
$T_{TX\text{-}RISE\text{-}FALL}$	Transmitter rise and fall time	0.15 UI	This parameter is measured differentially from 20% to 80% of the swing.

NOTE The rise/fall time test is limited to only rising or falling edges of the consecutive transitions for transmitter measurements (TF2 and TR2 as shown in Figure 4-28). TF1 and TR1 are not covered in the current test procedure.

Test Definition Notes from the Specification

Measurements at 5.0GT/s require an oscilloscope with a bandwidth of >= 12.5 GHz, or equivalent, while measurements made at 2.5GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5GT/s may be measured within 200mils of Tx device's pins although deconvolution is recommended. For measurement setup details, refer to Figure 4-23 and Figure 4-24. At least 10^6 UI of data must be acquired.

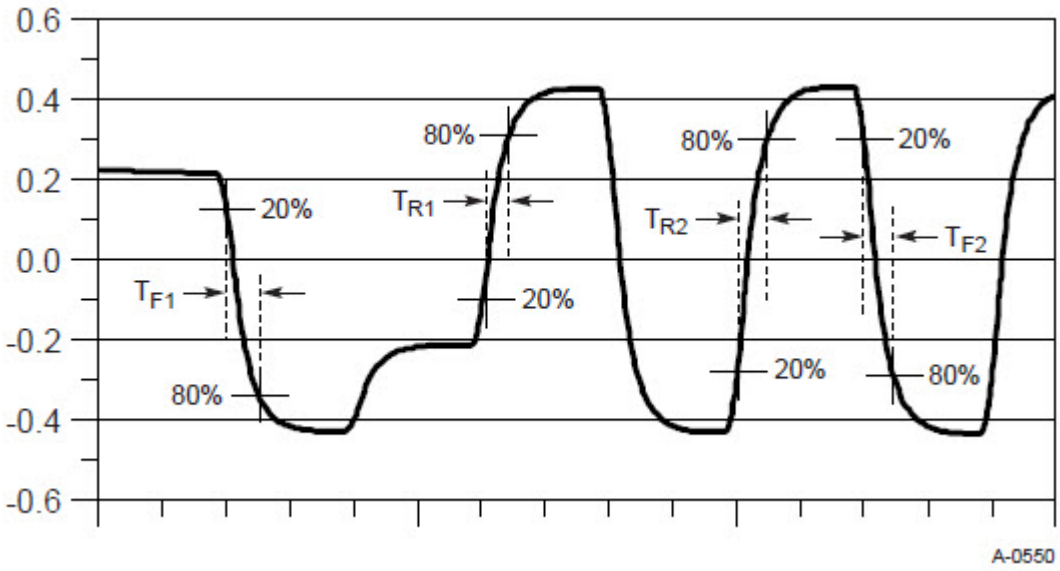


Figure 160 Rise and Fall Time Definition

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Tx Tests" on page 310 and select **Rise/Fall Time**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   a. Sets the value of **Clock Recovery Method** as **First Order PLL**.
   b. Sets the value of **Nominal Data Rate** as **5.000000000Gb/s**.
   c. Sets the value of **Loop Bandwidth** as **1.500MHz**.
3. Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.
4. Measures the non - transition bits eye top and base.
5. Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.
6. Measures the transition bits eye top and base.
7. Configures **Thresholds** using **Measurement Analysis (EZJIT)** as follows:
   a. Sets **Thresholds** as **20%,50%,80% of Top, Base**.
   b. Defines **Top/Base** values using the previously measured eye top and base as **Histogram**.

8 If the **Transition Time Threshold** is configured as **Variable** using Automated Test Engine, then:

   a Configures the value for **Setup Horizontal** to 50ps and **Center Reference** to 180ps.

   b Configures **Real-Time Eye Setup** using Serial Data.

   c Selects **Real-Time Eye Bits** as **Pattern Qualify** and measures the fall time de-emphasis bits.

   d Selects **Real-Time Eye Bits** as **Pattern Qualify** and measures the rise time de-emphasis bits.

   e Selects **Real-Time Eye Bits** as **Pattern Qualify** and measures the fall time transition bits.

   f Selects **Real-Time Eye Bits** as **Pattern Qualify** and measures the rise time transition bits.

   g Reports the maximum and minimum value for rise and fall time.

   h Reports the worst value as actual result.

9 Finds the minimum value from the minimum rise time and the minimum fall time. Compares the obtained value with the value as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $0.15\ UI < T_{TX\text{-}RISE}, T_{TX\text{-}FALL}$.

10 Reports the worst case measured rise/fall time value as the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deemphasized Voltage Ratio Test

Deemphasized voltage ratio is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. There are two different tests for the deemphasized voltage ratio. The test procedure is same for these tests with the exception of the compliance test limits used for the -3.5dB and the-6.0dB.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 87 Deemphasized Voltage Ratio Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0 dB	-4.0 dB
$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	De-Emphasized Differential Output Voltage (Ratio)	-5.5 dB	-6.5 dB

Test Definition Notes from the Specification

Root complex Tx de-emphasis is configured from Upstream controller. Downstream Tx de-emphasis is set via a command, issued at 2.5GT/s. For details, refer to the appropriate location in Section 4.2.

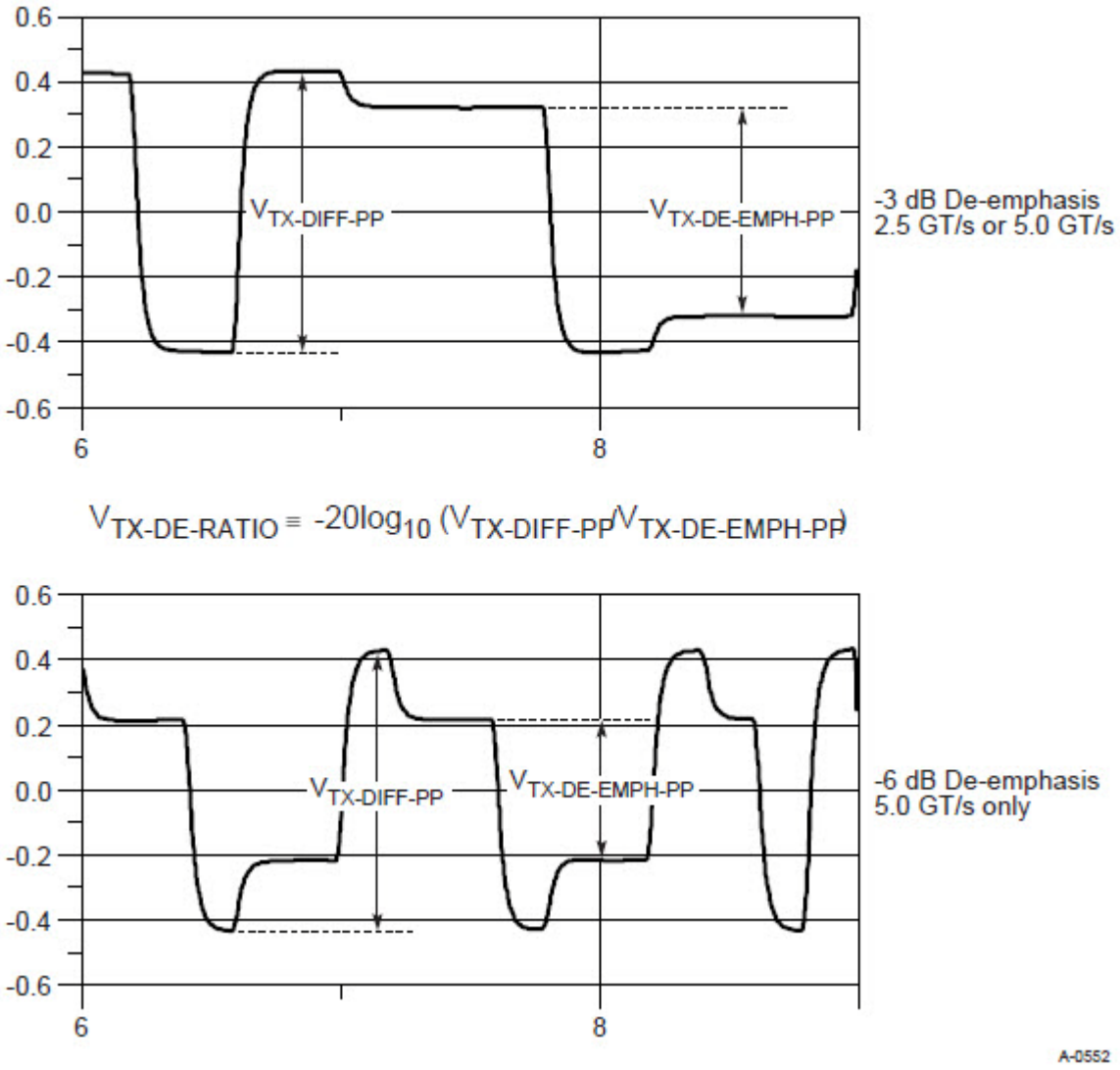


Figure 161 De-emphasized Voltage Ratio

Understanding the Test Flow

NOTE

Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Tx Tests" on page 310 and select **Deemphasized Voltage Ratio -3.5dB/Deemphasized Voltage Ratio -6.0dB**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:

   a Sets the value of **Clock Recovery Method** as **First Order PLL**.

   b Sets the value of **Nominal Data Rate** as **5.000000000Gb/s**.

   c Sets the value of **Loop Bandwidth** as **1.500MHz**.

3 Enables **Real-Time Eye** using **De-emphasis** as **Real-Time Eye Bits**.

4 Measures the non-transition bits eye top and base.

5 Enables **Real-Time Eye** using **Transition** as **Real-Time Eye Bits**.

6 Measures the transition bits eye top and bases.

7 Finds the differential value between the transition bits eye top and base as $V_{TX\text{-}DIFF\text{-}PP}$ using **Histogram**.

8 Finds the differential value between the non-transition bits eye top and base as $V_{TX\text{-}DE\text{-}EMPH\text{-}PP}$ using **Histogram**.

9 Calculates de-emphasis ratio using the following formula:

$$\text{De-emphasis ratio} = -20*\log 10(V_{TX-DIFF-PP}/V_{TX-DE-EMPH-PP})$$

10 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Avg DC Common Mode Output Voltage Test

The **Avg DC Common Mode Voltage** test measurement computes the DC average of the common mode signal:

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCI Express Base Specification, Rev 2.0 states that the transmitter DC common mode voltage ($V_{TX\text{-}DC\text{-}CM}$) must be held at the same value during all states.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 88 Avg DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	The TX DC Common Mode Voltage	0 V	3.6 V

NOTE This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled. For more information, see "Probing the Link for Tx Compliance" on page 306.

Test Definition Notes from the Specification

The allowed DC common mode voltage at the Transmitter pins under any conditions.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Tx Tests" on page 310 and select **Avg DC Common Mode Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Setup DC common mode voltage as follows:

   a Enables and displays common mode measurements.

   b Loads common mode signal to waveform memory.

   c Loads and enhance dynamic range D+ signal and D- signal.

   d Enables the average common mode measurement.

   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).

4 Measures the average value of D+ and D- signal.

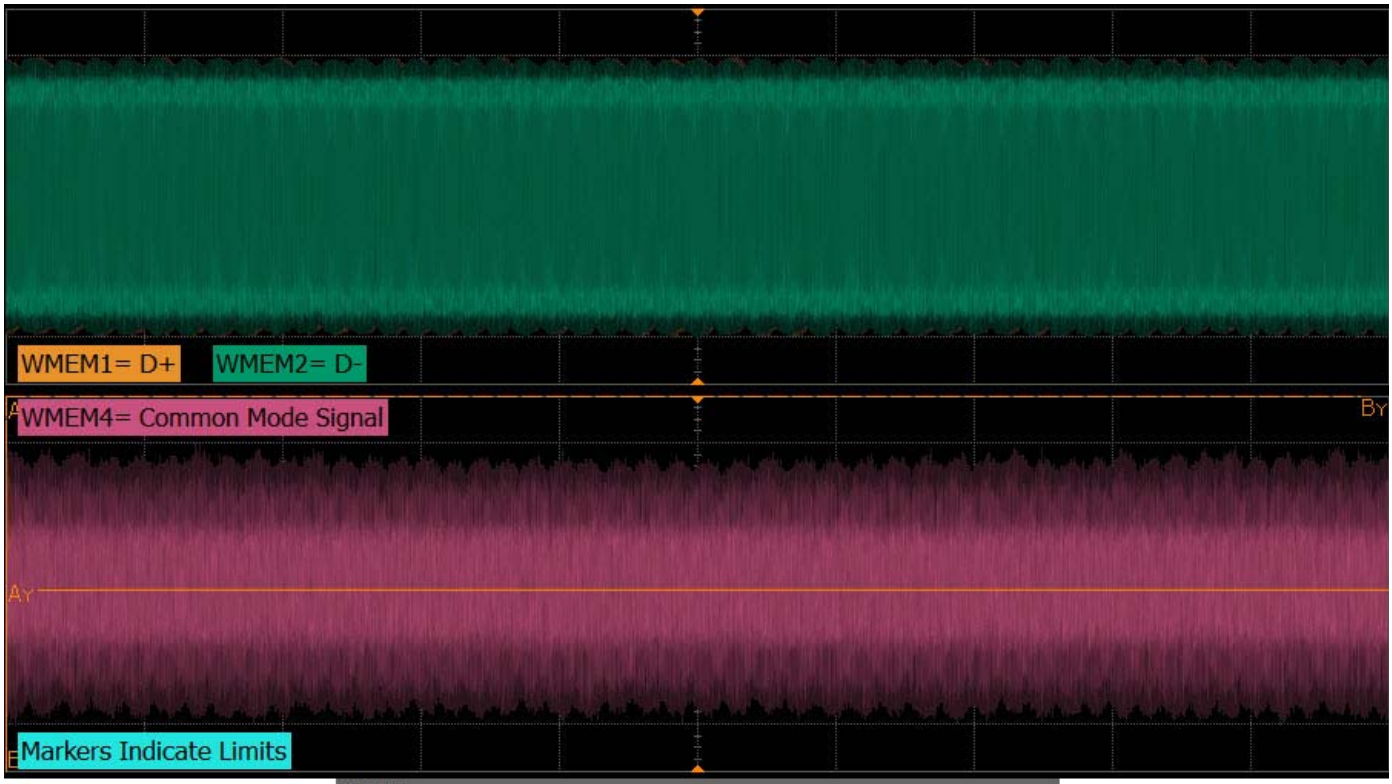
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $V_{TX\text{-}DC\text{-}CM}$ is `0` to `3.6 V (+/- 100mV).`

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to

view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	32.00 µs/div	0.000s	103.0 mV/div	5.560 mV
Memory 2	32.00 µs/div	0.000s	91.75 mV/div	1.084 mV
Memory 4	32.00 µs/div	0.000s	25.88 mV/div	3.470 mV

Markers

	Source	X Position	Y Position
A	Memory 4	-1.00000000000000s	0.000000V
B	Memory 4	-1.00000000000000s	3.600000V

Figure 162 Reference Image for Average DC Common Mode Output Voltage Test

DC Common Mode Line Delta Test

The **DC Common Mode Line Delta** computes the absolute difference between the average value of the D+ and the D- waveforms signals.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 89 DC Common Mode Line Delta Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0m V	25 mV

NOTE This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled. For more information, see "Probing the Link for Tx Compliance" on page 306).

Test Definition Notes from the Specification

$$|V_{TX\text{-}CM\text{-}DC\text{-}D+\ [during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D-\ [during\ L0]}| <= 25mV$$

Where,

$$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}\ of\ |V_{TX\text{-}D+}|\ [during\ L0]$$

$$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}\ of\ V_{TX\text{-}D-}|\ [during\ L0]$$

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Tx Tests" on page 310 and select **DC Common Mode Line Delta**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the average DC common mode output voltage test.

1 Reports the following measurement results obtained from running the average DC common mode output voltage test:
   a DC Common Mode Line Delta
   b Average DC value of D+
   c Average DC value of D-
2 Computes the DC common mode line delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $V_{TX\text{-}CM\text{-}LINE\text{-}DELTA} < 25mV$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic Jitter Test

The **Deterministic Jitter** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal. The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

1 High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.

2 Low frequency jitter (10kHz - 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.

3 Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

This test requires the EZJIT-Plus option to be installed on the scope. The test is disabled if the option is unavailable.

Test Reference

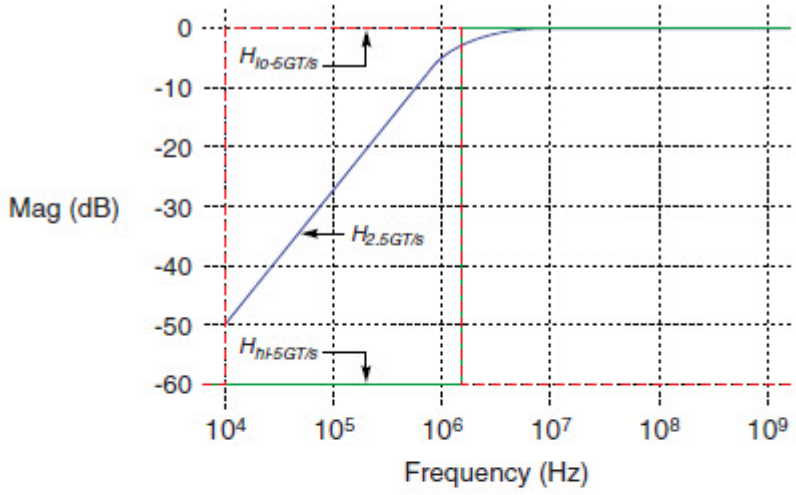
PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 90 Deterministic Jitter Test Details

Symbol	Parameter	Max	Comments
$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	T_X deterministic jitter > 1.5 MHz	0.15 UI	Deterministic Jitter only.

Test Definition Notes from the Specification

- Measurements at 5.0GT/s require an oscilloscope with a bandwidth of >= 12.5 GHz, or equivalent, while measurements made at 2.5GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5GT/s may be measured within 200mils of Tx device's pins although deconvolution is recommended. For measurement setup details, refer to Figure 4-23 and Figure 4-24. At least 10^6 UI of data must be acquired.
- For 5.0GT/s, de-emphasis timing jitter must be removed. An additional HPF function must be applied as shown in Figure 4-21. This parameter is measured by accumulating a record length of 10^6 UI while the DUT outputs a compliance pattern. $T_{MIN\text{-}PULSE}$ is defined to be nominally 1 UI wide and is bordered on both sides by pulses of the opposite polarity. Refer to Figure 4-29.



$$H_{2.5GT/s} = \frac{s}{s + w_c} \qquad w_c = 2\pi f_T$$

$$H_{hi\text{-}5GT/s} = if(f >= f_T)\ then\ 1.0\ else\ 10^{-3}$$

$$H_{lo\text{-}5GT/s} = if(f < f_{10kHz})\ then\ 10^{-3}$$

$$elseif\ (f < f_T)\ then\ 1.0$$

$$else\ 10^{-3}$$

$$f_T = 1.5\ MHz$$

A-0544

Figure 163 Plot of Transmitter HPF Filter Functions

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Tx Tests" on page 310 and select **Deterministic Jitter > 1.5 MHz**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:
   a. Sets the value of **Clock Recovery Method** as **Constant Frequency**, **Semi-Automatic** method and **Nominal Data Rate** to 5.000000000Gb/s.
   b. Turns on **TIE Filter** and configures the **Start Frequency** to **1.50000MHz** and **Stop Frequency** to **13GHz.**
3. Configures the following using the **Jitter / Noise Setup** as:
   a. Configures **Measurement** as **TIE (Phase)**.
   b. Configures **RJ Bandwidth** as **Narrow (Pink)**.
   c. Configures **Units** as **Second**.
   d. Checks **Auto** for **Pattern Length**.
   e. Configures **BER Level** to **1E-12**.
4. Enables the jitter graph.
5. Configures the threshold for upper and lower level.
6. Reads the DJ value from the scope and divides by the unit interval.
7. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test

The **Random Jitter** test is a timing measurement in PCI Express 2.0 that requires separation of the low frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10kHz – 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 91 Random Jitter Test Details

Symbol	Parameter	Max
$T_{TX-LF-RMS}$	T_x RMS Jitter <1.5MHz	3.0ps RMS

Test Definition Notes from the Specification

Total energy measured over a 10KHz - 1.5 MHz range.

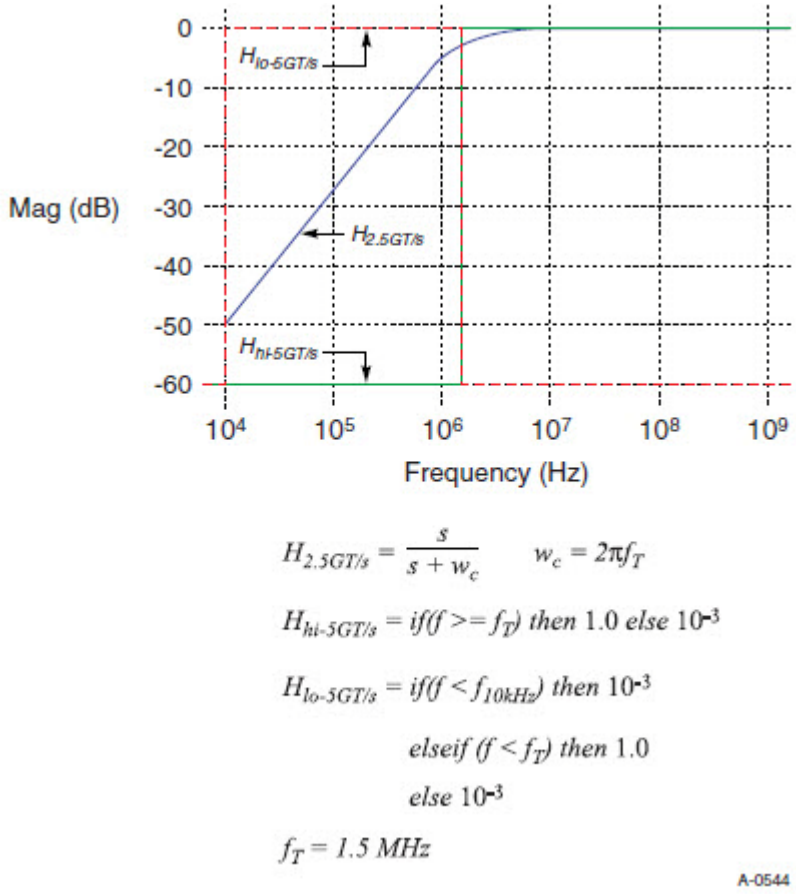


Figure 164 Plot of Transmitter HPF Filter Functions

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Tx Tests" on page 310 and select **Random Jitter < 1.5MHz**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Clock Recovery** using **Measurement Analysis (EZJIT)** as follows:

   a Sets the value of **Clock Recovery Method** as **Constant Frequency**, **Semi-Automatic** method and **Nominal Data Rate** to **5.000000000Gb/s**.

   b Turns on **TIE Filter** and configures the **Start Frequency** to **1.50000MHz** and **Stop Frequency** to **13GHz.**

3 Configures the following using the **Jitter / Noise Setup** as:

   a Configures **Measurement** as **TIE (Phase)**.

   b Configures **RJ Bandwidth** as **Narrow (Pink)**.

   c Configures **Units** as **Second**.

   d Checks **Auto** for **Pattern Length**.

   e Configures **BER Level** to **1E-12**.

4 Enables the jitter graph.

5 Configures the threshold for upper and lower level.

6 Reads the TJ, RJ and DJ values from the scope and divides by the unit interval.

7 Reports the RJ measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Template Tests

All PCIE devices must meet the transmitter eye diagram as specified in the PCI Express Base Specification, Rev 2.0. All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 92 Template Test Details

Symbol	Parameter	Min	Max	Comments
$V_{TX-DIFF-PP}$	Differential p-p T_x voltage swing	0.8V	1.2V	The differential p-p T_x voltage swing

Test Definition Notes from the Specification

As measured with the compliance test load. Defined as $2^*|V_{TXD+}- V_{TXD-}|$.

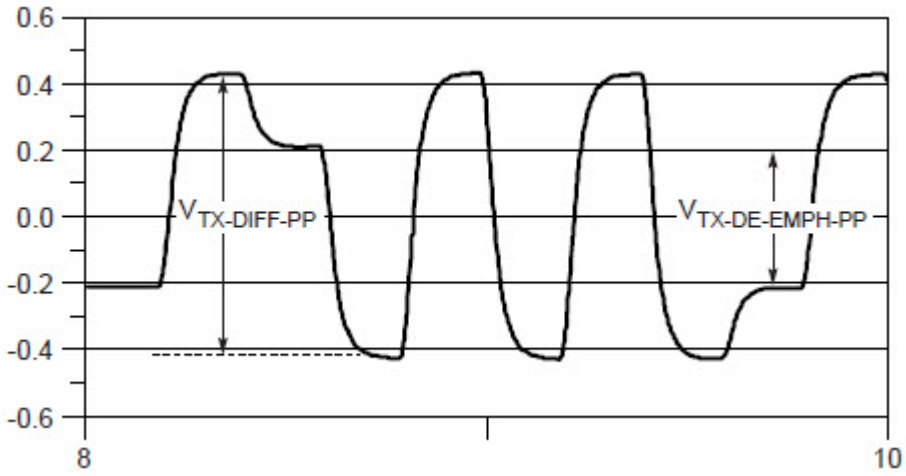


Figure 165 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Tx Tests" **on page 310** and select **Template Tests**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the transmitter compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the mean differential p-p T_x voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $0.8V < V_{TX-DIFF-PP} < 1.2V$ and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER - 12]$$

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 93 Eye Width Test Details

Symbol	Parameter	Min	Comments
T_{TX-EYE}	Minimum T_X Eye Width	0.75 UI	This parameter includes Rj at 10^{-12} and excludes single source clock or reference clock jitter.

Test Definition Notes from the Specification

- Measurements at 5.0GT/s require an oscilloscope with a bandwidth of >= 12.5 GHz, or equivalent, while measurements made at 2.5GT/s require a scope with at least 6.2 GHz bandwidth. Measurement at 5.0GT/s must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. 2.5GT/s may be measured within 200mils of Tx device's pins although deconvolution is recommended. For measurement setup details, refer to Figure 4-23 and Figure 4-24. At least 10^6 UI of data must be acquired.
- Transmitter jitter is measured by driving the Transmitter under test with a low jitter "ideal" clock and connecting the DUT to a reference load.
- Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5GT/s and 5.0GT/s use different filter functions that are defined in Figure 4-21. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.
- For 5.0GT/s, de-emphasis timing jitter must be removed. An additional HPF function must be applied as shown in Figure 4-21. This parameter is measured by accumulating a record length of 10^6 UI while the DUT outputs a compliance pattern. $T_{MIN-PULSE}$ is defined to be nominally 1 UI wide and is bordered on both sides by pulses of the opposite polarity. Refer to Figure 4-29.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Tx Tests" on page 310 and select **Eye-Width**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 5.0GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express Base Specification, Rev 2.0 as $0.75\ UI < T_{TX-EYE}$.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage (Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 94 Peak Differential Output Voltage Test Details

Symbol	Parameter	Min	Max	Comments
$V_{TX-DIFF-PP}$	Differential p-p T_x voltage swing	0.80 V	1.2 V	The differential p-p T_x voltage swing parameter is defined as $2*\lvert V_{TXD+} - V_{TXD-}\rvert$ as measured with the compliance test load.
$V_{TX-DIFF-PP-Low}$	Low power differential p-p T_x voltage swing	0.40 V	1.2 V	The differential p-p T_x voltage swing parameter is defined as $2*\lvert V_{TXD+} - V_{TXD-}\rvert$ as measured with the compliance test load.

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as $2*\lvert V_{TX-D+} - V_{TX-D-}\rvert$

.

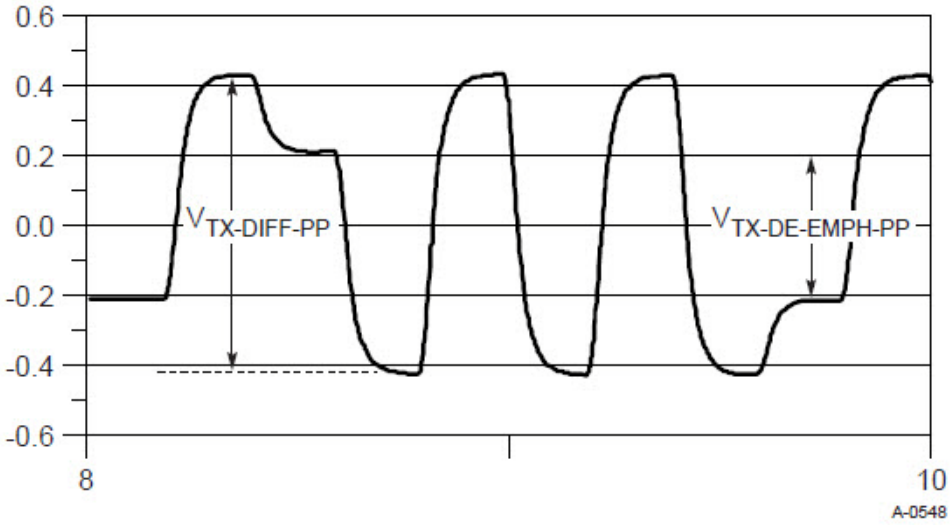


Figure 166 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

- Low swing output, defined by $V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$ must be implemented as shown in Figure 4-27 with no de-emphasis.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Tx Tests" on page 310 and select **Peak Differential Output Voltage (Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE1.0a

Data Rate: 5.0GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

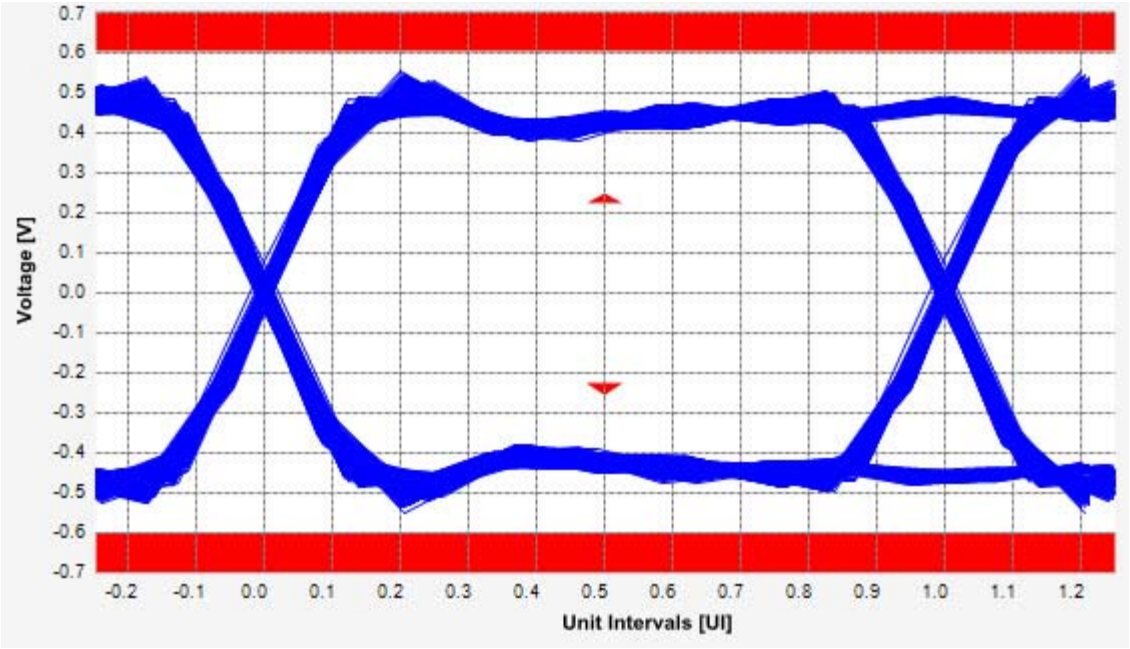


Figure 167 Reference Image for Peak Differential Output Voltage (Transition) Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (Non-Transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 95 Peak Differential Output Voltage Test Details

Symbol	Parameter	Min	Max	Comments
$V_{TX-DIFF-PP}$	Differential p-p T_x voltage swing	0.80 V	1.2 V	The differential p-p T_x voltage swing parameter is defined as $2*\lvert V_{TXD+} - V_{TXD-}\rvert$ as measured with the compliance test load.
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p T_x voltage swing	0.40 V	1.2 V	The differential p-p T_x voltage swing parameter is defined as $2*\lvert V_{TXD+} - V_{TXD-}\rvert$ as measured with the compliance test load.

Test Definition Notes from the Specification

- As measured with compliance test load. Defined as $2*\lvert V_{TX-D+} - V_{TX-D-}\rvert$

.

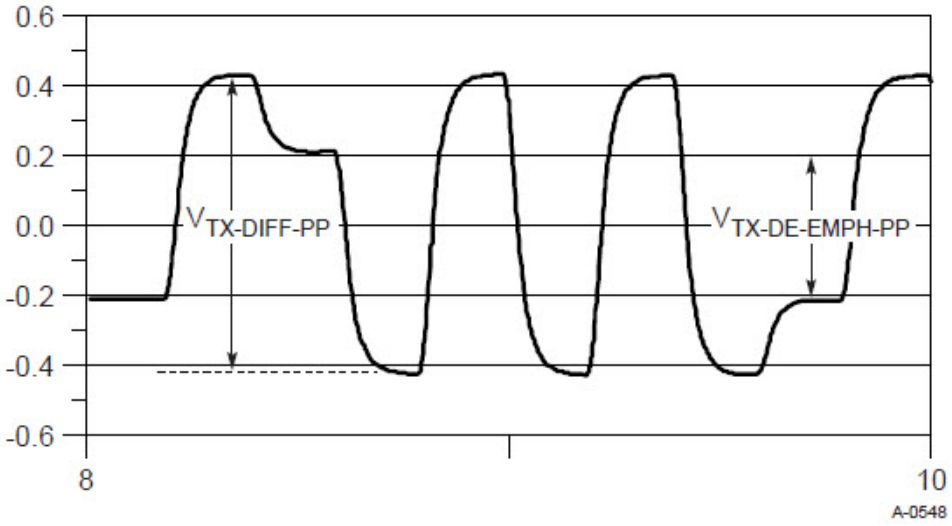


Figure 168 Full Swing Signaling Voltage Parameters Showing -6dB De-emphasis

- Low swing output, defined by $V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$ must be implemented as shown in Figure 4-27 with no de-emphasis.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Tx Tests" on page 310 and select **Peak Differential Output Voltage (Non Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE 2.0

Data Rate: 5.0GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (non transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

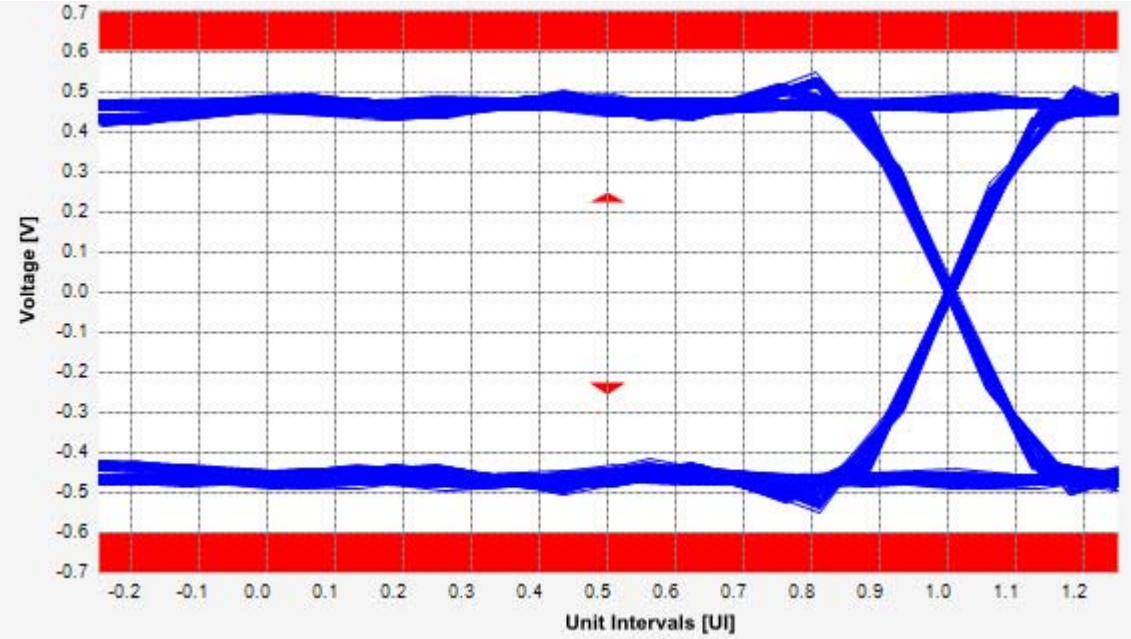


Figure 169 Reference Image for Peak Differential Output Voltage (Non-Transition) Test

20
Receiver (R_x) Tests, 5.0 GT/s, PCI-E 2.0

This section provides the Methods of Implementation (MOIs) for Receiver (Rx) 5.0 GT/s tests of PCI-E 2.0 using an Agilent 90000X series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

NOTE None of the included receiver tests validate the receiver's ability to correctly receive data (also known as receiver tolerance). Rather, they validate that the signal as seen by the receiver meets or exceeds various parameters (maximum voltage, jitter, eye width, etc.). These tests validate the transmitter and interconnect. Separate receiver tolerance testing is required to ensure the receiver is correctly receiving data.

Probing the Link for Rx Compliance

Receiver tests are done by probing the link as close as is feasibly possible to the pins of the receiver device. Alternatively, a dummy load can be used for the termination of the link. To probe the receiver link, you can:

- Use two differential probe heads with two 1169A probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of an oscilloscope that has 40 GS/s sample rate available on two channels.
- Use one differential probe head with the 1169A probe amplifier and the Ch2 input of an oscilloscope that has 40 GS/s sample rate available on that channel.

Table 96 Probing Options for Receiver Testing

	Probing Configurations			Captured Waveforms		System Specifications	
						90000X	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
DUT Connection	Single-Ended (2 x 1169A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	12 GHz	70 ps
	Differential (1 x 1169A w/ Differential Probe Head)	Y/N	1	True	No	12 GHz	70 ps

*Typical

Single-Ended Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1-Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1+Ch3)/2.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

Channel-to-channel de-skew is required using this technique because two channels are used.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

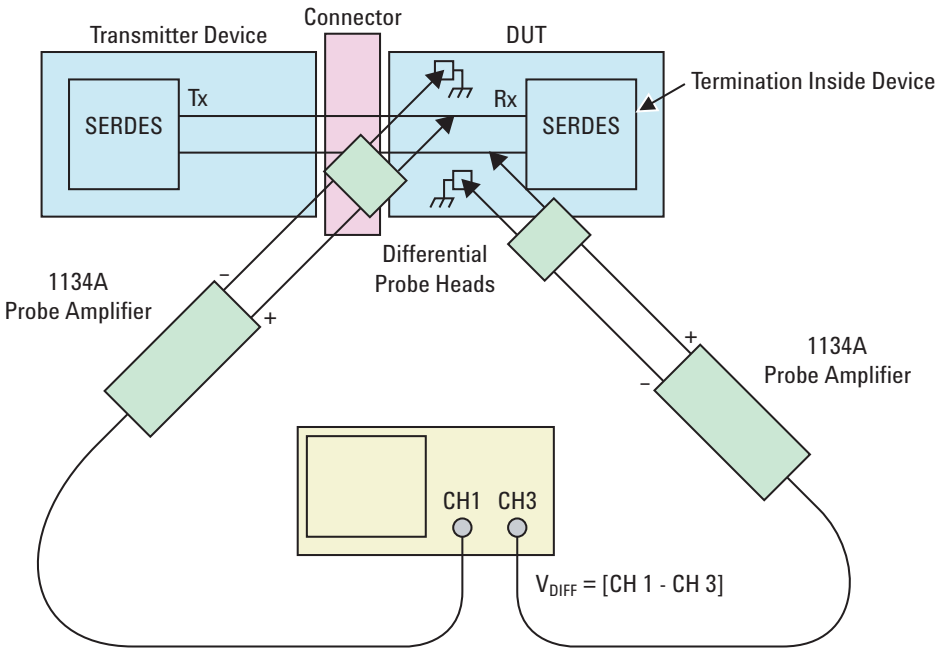


Figure 170 Single-Ended Probing

Differential Probing (Ch2)

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the receiver, as close as possible to the receiver, with the shortest ground connection possible.

This probing technique can be used for either a live link that is transmitting data, or a link terminated into a “dummy load.”

A single channel of the oscilloscope is used, so de-skew is not necessary.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

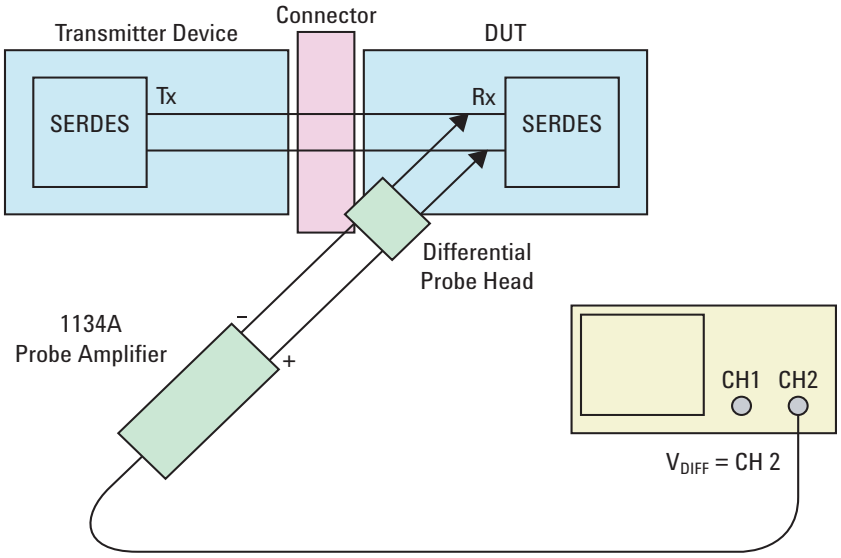


Figure 171 Differential Probing

Running Receiver Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "Receiver (Rx) Tests" group.

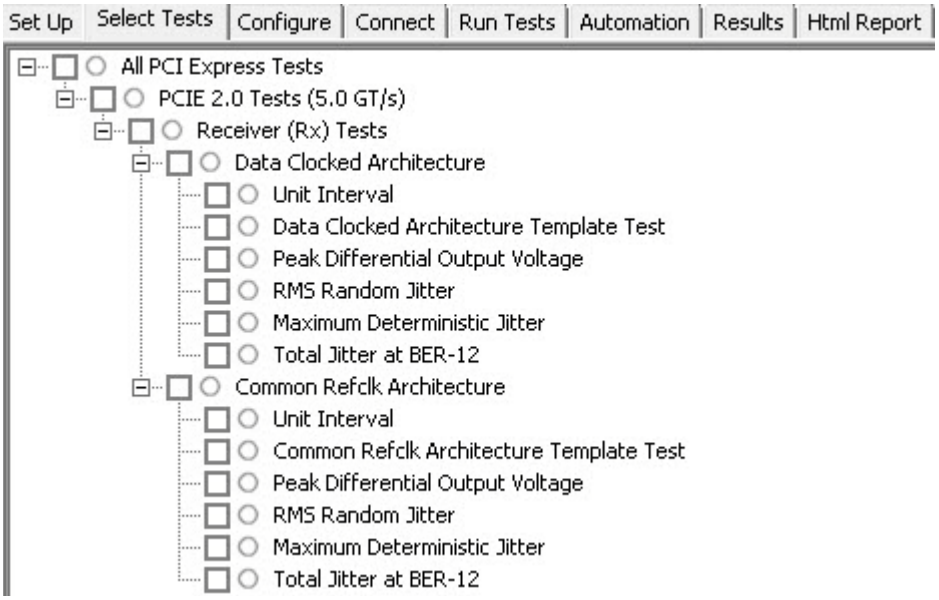


Figure 172 Selecting Receiver (Rx) Tests

Unit Interval Test

A recovered receiver unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$R_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The R_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another R_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case R_X UI is reported. There exists two different tests for unit interval test as follows:

- Data clocked unit interval test
- Common reference clocked unit interval test

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 97 Unit Interval Test Details

Symbol	Parameter	Min	Max	Comments
UI	Unit Interval	199.94 ps	200.06 ps	UI does not account for SSC caused variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Receiver Tests" on page 347 and select **Unit Interval**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.

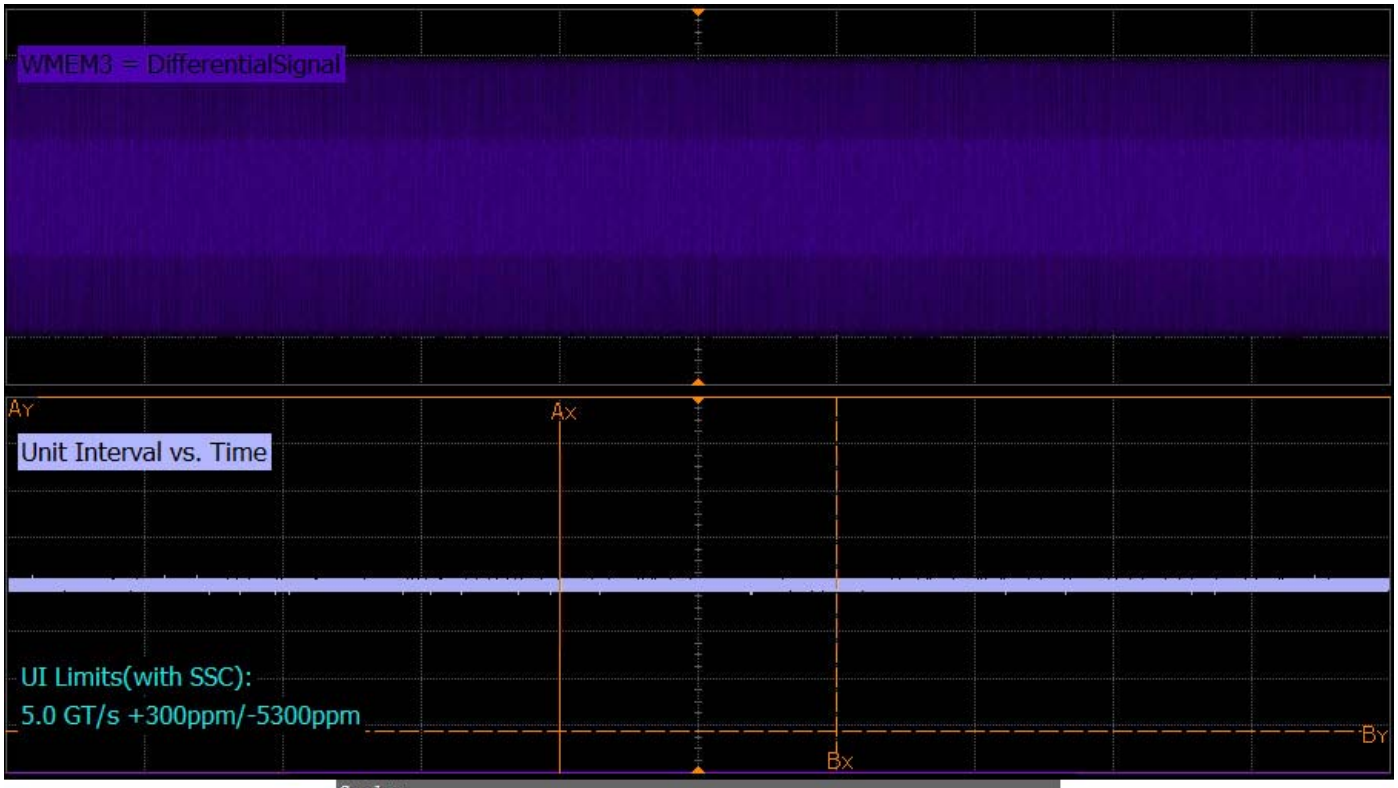
4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	32.00 µs/div	0.000s	20.00 fs/div	200.0 ps
Memory 3	32.00 µs/div	0.000s	162.5 mV/div	4.600 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-32.0000000040000 µs	200 pV
B	Function 3	32.0000000040000 µs	200 pV

Figure 173 Reference Image for Unit Interval Test (Data clocked architecture)

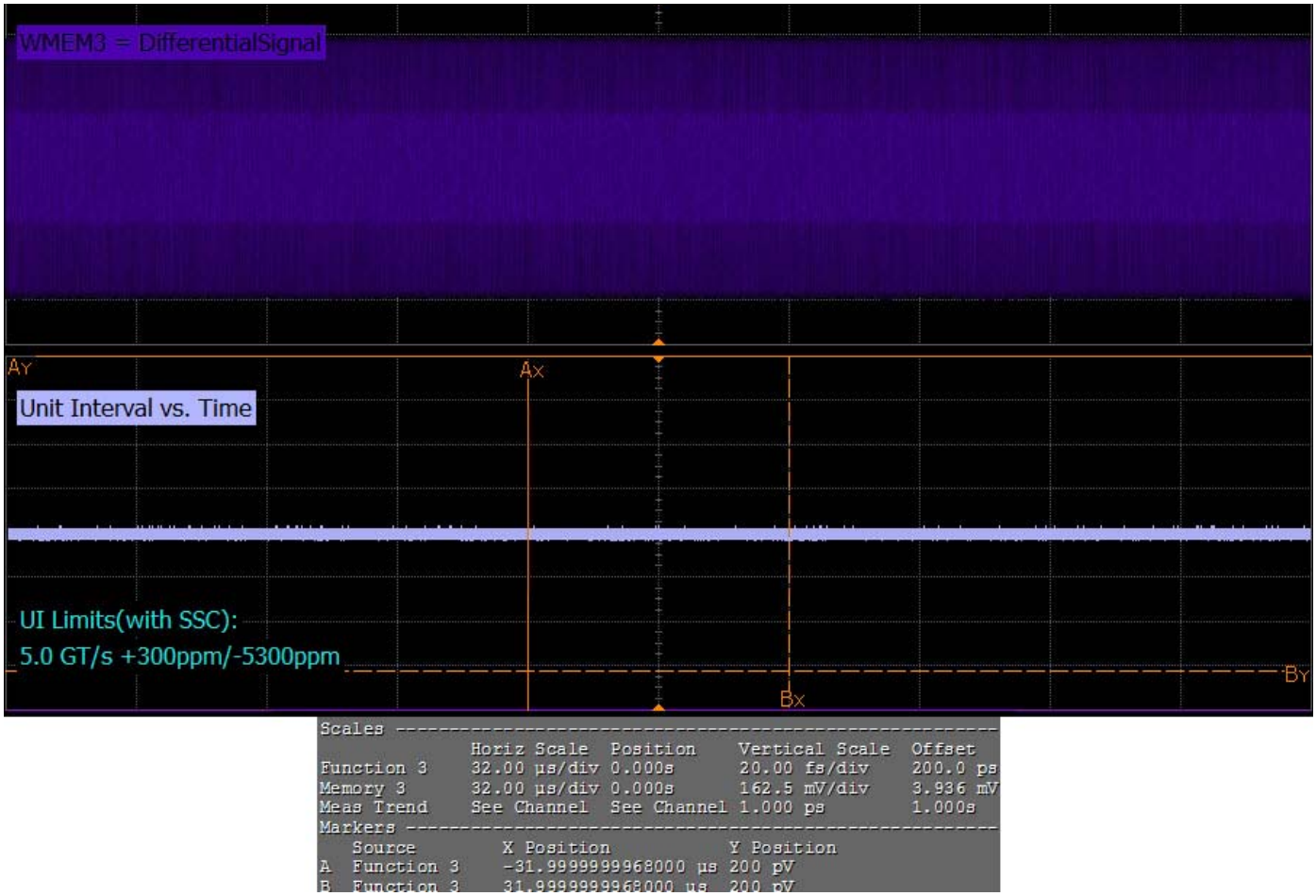


Figure 174 Reference Image for Unit Interval Test (Reference Clock architecture)

NOTE The MOI for the measurement of UI at the receiver is identical to measuring it at the transmitter, with the exception of the test point. Refer to "Unit Interval Test" on page 39.

Data Clocked Architecture Template Test/ Common Refclk Architecture Template Test

A receiver must reliably receives all data that meets the differential receiver input specifications as shown in PCI Express Base Specification, rev 2.0. This test does not validate the receiver's tolerance.

All links are assumed active while generating the eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level. There exists two different tests for template interval test with the same test procedure and exception of the template files as follows:

- Data clocked template test
- Common reference clocked template test

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 98 Template Test Details

Symbol	Parameter	Min	Max
$V_{RX-DIFF-PP-CC}$	Differential R_x peak-peak voltage for common Refclk Rx architecture	0.120V	1.2V
$V_{RX-DIFF-PP-DC}$	Differential R_x peak-peak voltage for data clocked Rx architecture	0.100V	1.2V

NOTE For more information on the receiver parameter details, refer to Section 4.3.7.2.2 of the base specification.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Receiver Tests" on page 347 and select **Data Clocked Architecture Template Test / Common Refclk Architecture Template Test**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the receiver compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the mean differential p-p R_x voltage swing as the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the base specification and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help..

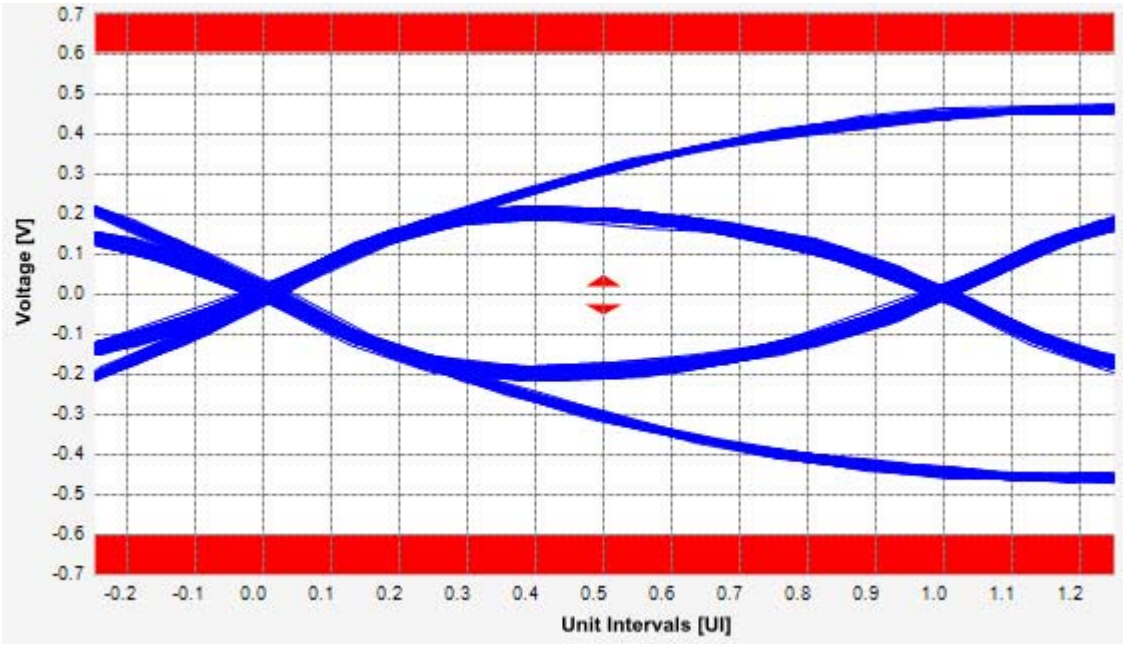


Figure 175 Reference Image for Data Clocked Architecture Template (transition) Test

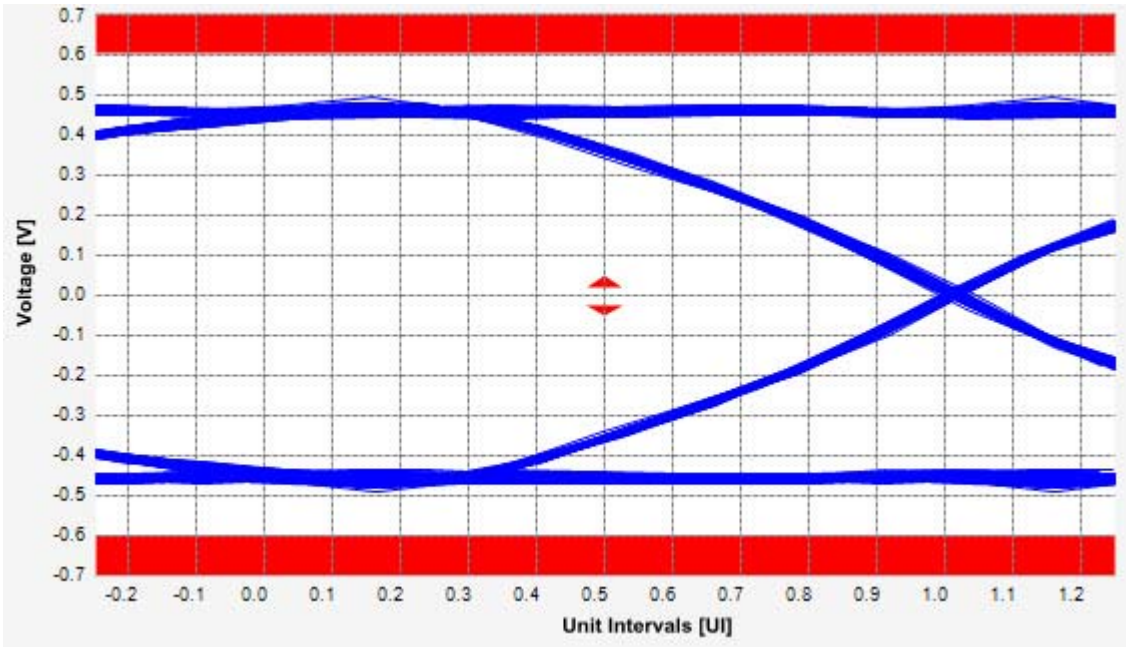


Figure 176 Reference Image for Data Clocked Architecture Template (non transition) Test

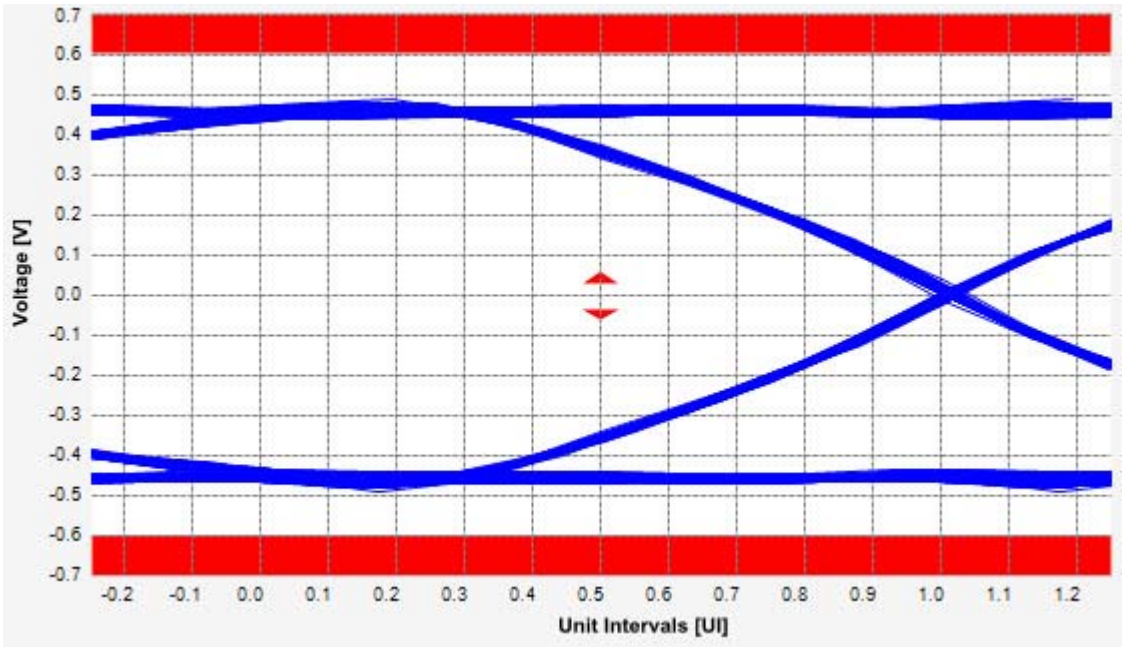


Figure 177 Reference Image for Reference Clock Architecture Template (transition) Test

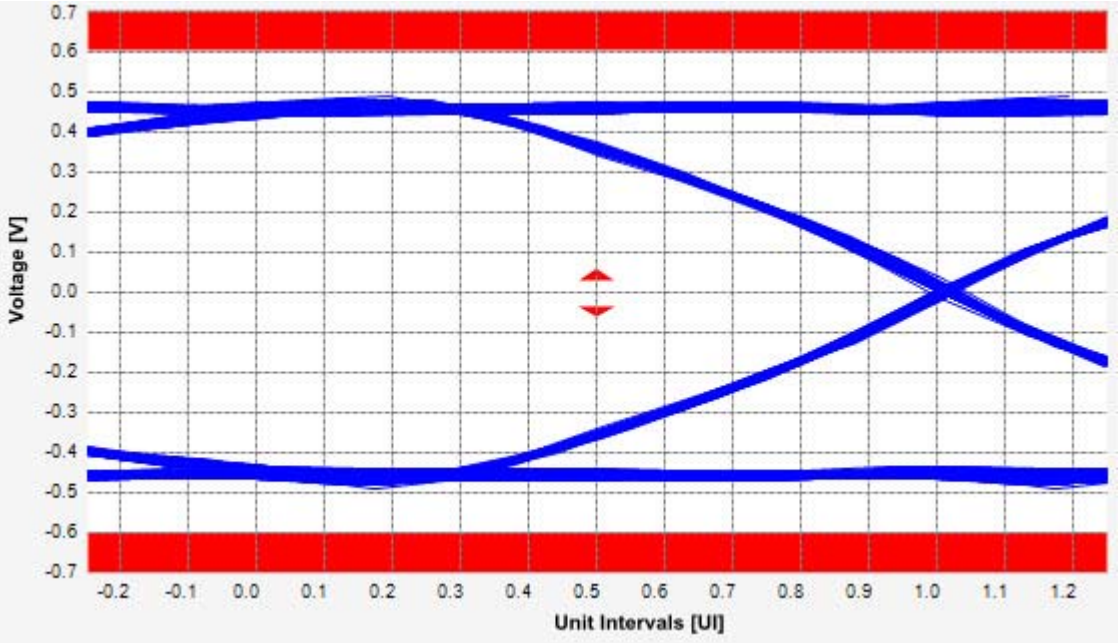


Figure 178 Reference Image for Reference Clock Architecture Template (non transition) Test

Peak Differential Output Voltage Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform.

$$V_{RX-DIFF-PP} = 2*Max(Max(V_{DIFF(i)}),M(axin)(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

There exists two different tests for peak differential output voltage test with the same test procedure and exception of the template files as follows:

- Data clocked architecture peak differential output voltage test
- Common reference clocked architecture peak differential output voltage test

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 99 Peak Differential Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{RX-DIFF-PP-CC}$	Differential R_x peak-peak Voltage for common refclk Rx architecture	0.120 V	1.2 V
$V_{RX-DIFF-PP-DC}$	Differential R_x peak-peak Voltage for data clocked Rx architecture	0.100 V	1.2 V

NOTE For more information on the peak differential output voltage test definition, refer to Section 4.3.7.2.2 of the base specification.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Receiver Tests" on page 347 and select **Peak Differential Output Voltage**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Extracts the non transition and transition eye diagram data from the SigTestWrapper.dll file.

2 Finds the peak differential output voltage (non transition) mean and peak differential output voltage (transition) mean from the center of UI.

3 Compares both the worst values and finds the worst case value and reports as peak differential output voltage (data clocked, reference clock).

4 Compares the measured peak differential output voltage (data clocked, reference clock) value to the compliance limits.

5 Reports the measured peak differential output voltage (transition) value as the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RMS Random Jitter

The **RMS Random Jitter** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The receiver margining leverages LF(low frequency) / HF(high frequency) jitter separation methodology employed for the transmitter.

There exists two different tests for this test with the same test procedure and exception of the template files as follows:

- Data clocked architecture RMS random jitter test
- Common reference clocked architecture RMS random jitter test

NOTE The RMS random jitter range for this test is not specified in the base specification (reference specs for all the transmitter and receiver tests). This test provides informative data only.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 100 RMS Random Jitter Test Details

Symbol	Parameter	Max	Comments
$T_{RX-TJ-CC}$	Max Rx inherent timing error	0.40 UI	Max Rx inherent total timing error for common Refclk Rx architecture. See below note.
$T_{RX-TJ-DC}$	Max Rx inherent timing error	0.34 UI	Max Rx inherent total timing error for data clocked Rx architecture. See below note.
$T_{RX-DJ-DD-CC}$	Max Rx inherent deterministic timing error	0.30 UI	Max Rx inherent deterministic timing error for common Refclk Rx architecture. See below note.
$T_{RX-DJ-DD-CC}$	Max Rx inherent deterministic timing error	0.24 UI	Max Rx inherent deterministic timing error for data clocked Rx architecture. See below note.

Test Definition Note from the Specification

The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Receiver Tests" on page 347 and select **RMS Random Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

Test Procedure

1 Gets RJ_rms test results from the SigTestWrapper.dll file.

2 Compares the measured RJ_rms value to the compliance test limits.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Maximum Deterministic Jitter Test

The **Maximum Deterministic Jitter** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The receiver margining leverages LF(low frequency) / HF(high frequency) jitter separation methodology employed for the transmitter.

There exists two different tests for this test with the same test procedure and exception of the template files as follows:

- Data clocked architecture maximum deterministic jitter test
- Common reference clocked architecture maximum deterministic jitter test

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4-12 is used as reference to check the compliance of the DUT.

Table 101 Maximum Deterministic Jitter Test Details

Symbol	Parameter	Max	Comments
$T_{RX\text{-}DJ\text{-}DD\text{-}CC}$	Max Rx inherent deterministic timing error	0.30 UI	Max Rx inherent deterministic timing error for common Refclk Rx architecture. See below note.
$T_{RX\text{-}DJ\text{-}DD\text{-}CC}$	Max Rx inherent deterministic timing error	0.24 UI	Max Rx inherent deterministic timing error for data clocked Rx architecture. See below note.

Test Definition Note from the Specification

The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Receiver Tests" on page 347 and select **Maximum Deterministic Jitter**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

Test Procedure

1 Gets DJ_dd test results from the SigTestWrapper.dll file.

2 Compares the measured DJ_dd value to the compliance test limits.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Jitter at BER-12 Test

The **Total Jitter at BER-12** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The receiver margining leverages LF(low frequency) / HF(high frequency) jitter separation methodology employed for the transmitter.

There exists two different tests for this test with the same test procedure and exception of the template files as follows:

- Data clocked architecture total jitter at BER- 12 test
- Common reference clocked architecture total jitter at BER- 12 test

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.4.4, Table 4- 12 is used as reference to check the compliance of the DUT.

Table 102 Total Jitter at BER -12 Test Details

Symbol	Parameter	Max	Comments
$T_{RX-TJ-CC}$	Max Rx inherent timing error	0.40 UI	Max Rx inherent total timing error for common Refclk Rx architecture. See below note.
$T_{RX-TJ-DC}$	Max Rx inherent timing error	0.34 UI	Max Rx inherent total timing error for data clocked Rx architecture. See below note.

Test Definition Note from the Specification

The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Receiver Tests" on page 347 and select **Total Jitter at BER-12**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

Test Procedure

1 Gets total jitter at BER-12 test results from the SigTestWrapper.dll file and divides it by unit interval.

2 Compares the measured total jitter at BER-12 value to the compliance test limits.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

21 Add-In Card (Tx) Tests, 5.0 GT/s, PCI-E 2.0

This section provides the Methods of Implementation (MOIs) for Add-In Card (Tx) 5.0 GT/s tests of PCI-E 2.0 using an Agilent 90000X series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Add-In Card Compliance

Connecting the Compliance Base Board for Add-in Card Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 connector slot.

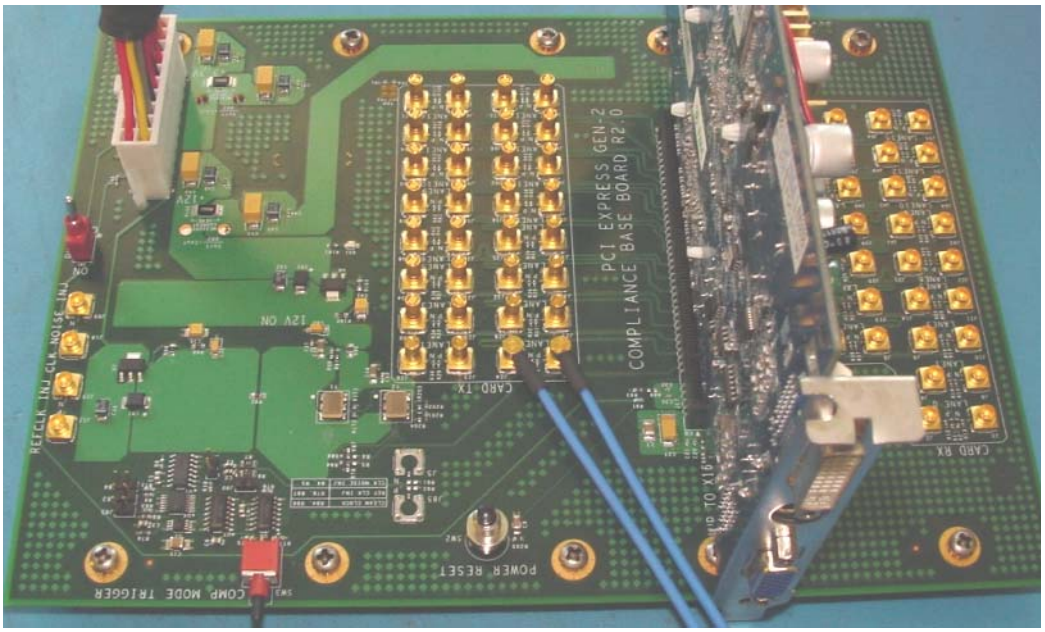


Figure 179 Compliance Base Board (CBB) Add-in Card Fixture

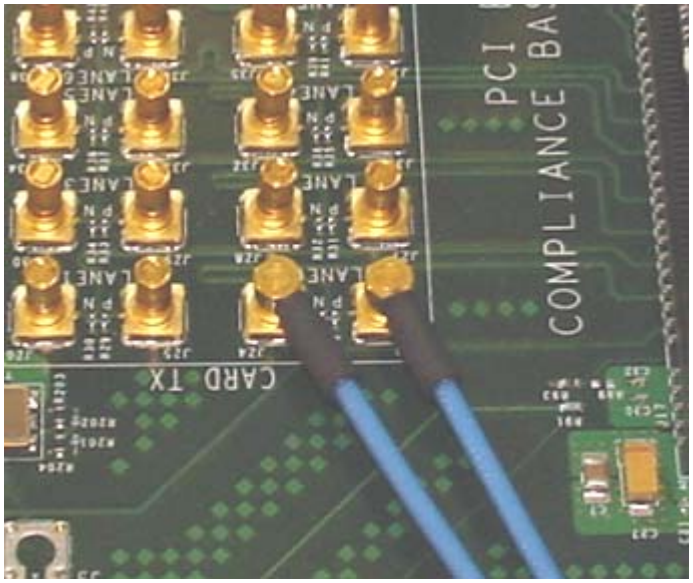


Figure 180 Compliance Base Board (CBB) 2.0 SMP Probing Option

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the D+ (where Lane 1 is under test in this example shown in Figure 180 above).

   b Digital Storage Oscilloscope channel 3 to the D- (where Lane 1 is under test in this example shown in Figure 180 above).

   When SMP probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 626).

   Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

   When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

4 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

5 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

Running Add-In Card Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "Add-In Card (Tx) Tests" group.

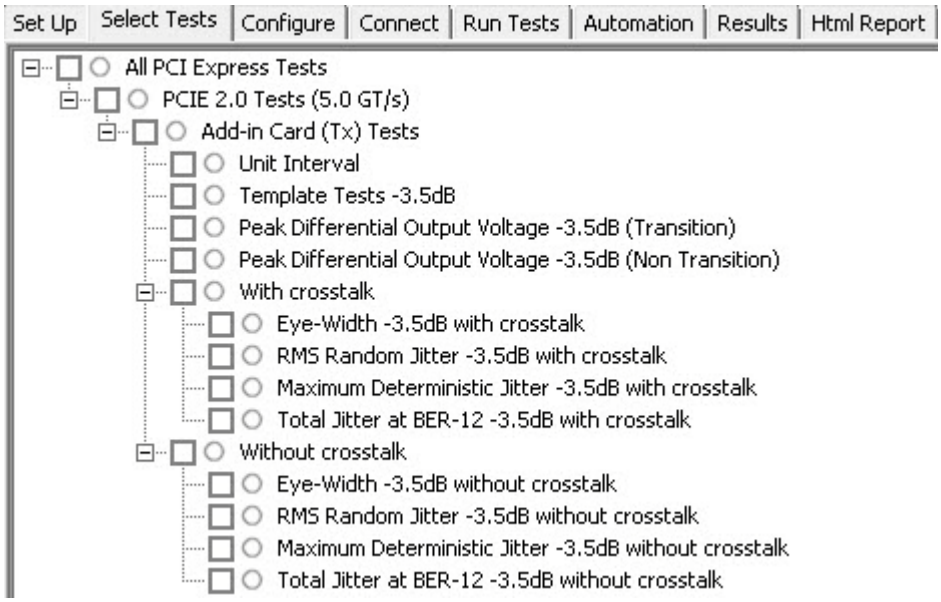


Figure 181 Selecting Add-In Card (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 103 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	199.94 ps	200.06 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Add-In Card Tests" on page 369 and select **Unit Interval**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

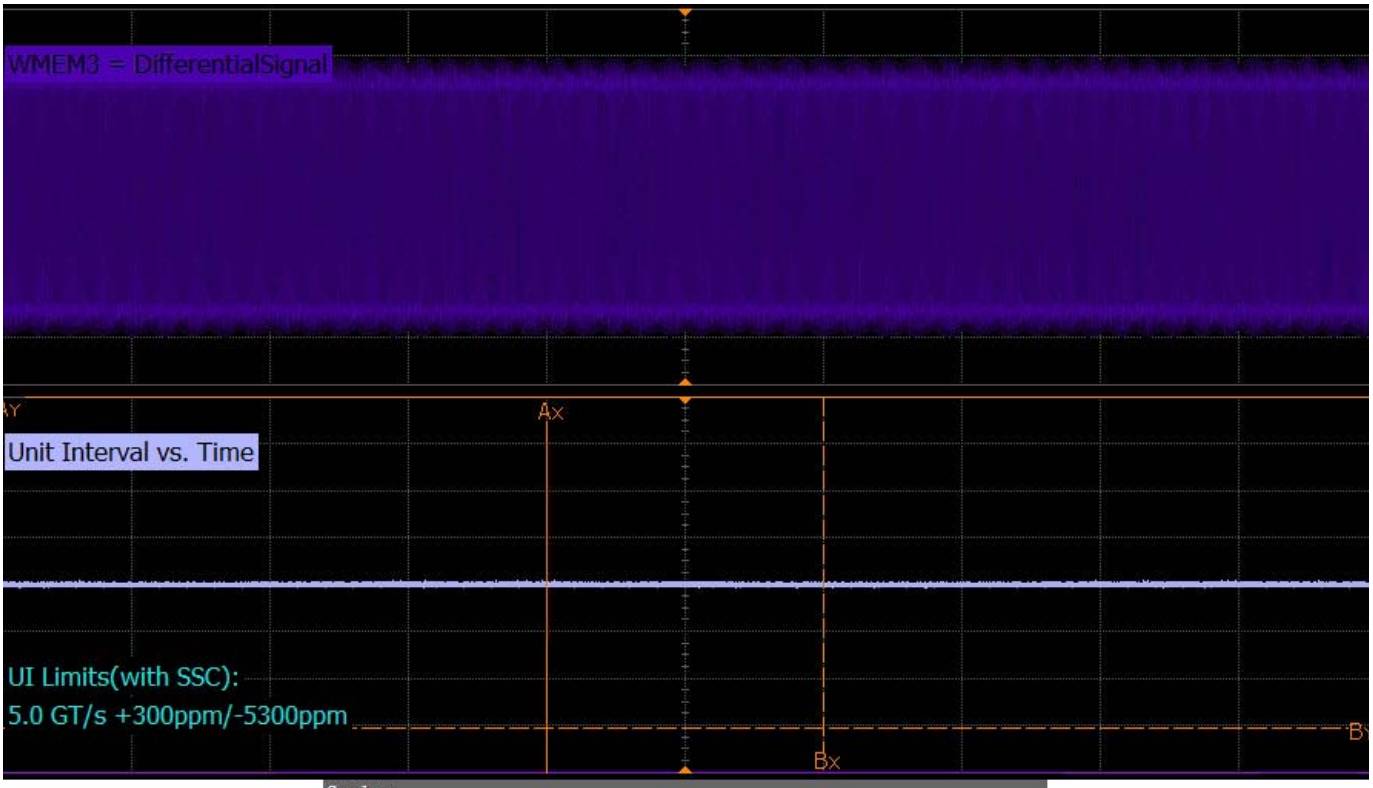
4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	32.00 µs/div	0.000s	20.00 fs/div	200.0 ps
Memory 3	32.00 µs/div	0.000s	186.3 mV/div	4.355 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-31.9999999936000 µs	200 pV
B	Function 3	31.9999999936000 µs	200 pV

Figure 182 Reference Image for Unit Interval Test

Template Tests

Add-in cards must meet the **Add-in Card Transmitter Path Compliance Eye-Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 2.0, Section 4.7.2, Table 4-8 and Table 4-10 as measured at the card edge-fingers. This test does not validate the receiver's tolerance, rather it validates that the signal at the receiver meets the specifications in Figure 4-7.

All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (Vtx_{A_d}).

There exists two different tests for template test with the same test procedure and exception of the template files used for the -3.5dB and 6.0 dB as follows:

- Template test -3.5dB
- Template test -6.0dB

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.2 is used as reference to check the compliance of the DUT.

Table 104 Template Test Details -3.5dB De-emphasis

Symbol	Min	Max
V_{TXA}	380 mV	1200 mV
V_{TXA_d}	380 mV	1200 mV
T_{TXA} (with crosstalk)	123 ps	
T_{TXA} (without crosstalk)	126ps	

Table 105 Template Test Details -6.0dB De-emphasis

Symbol	Min	Max
V_{TXA}	306 mV	1200 mV
V_{TXA_d}	260 mV	1200 mV
T_{TXA} (with crosstalk)	123 ps	
T_{TXA} (without crosstalk)	126ps	

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
- T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at BER10^{-12} must not exceed $T_{TXA.}$ If the add-in card board uses non-interleaved routing, then crosstalk will be present in the measured data. If the add-in card board uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.
- The values in Table 4-8 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

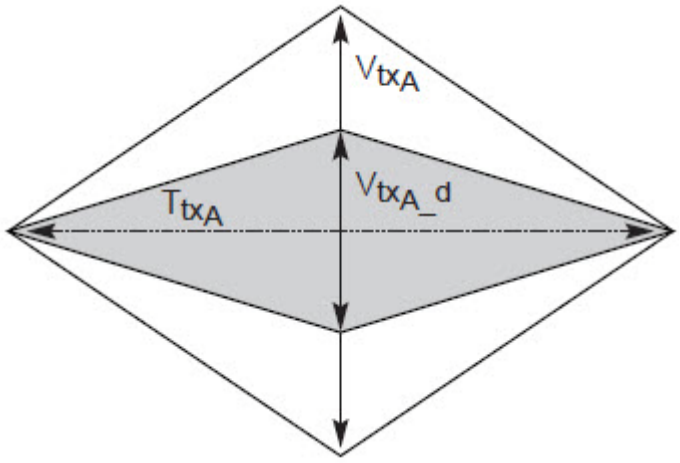


Figure 183 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Add-In Card Tests" on page 369 and select **Template Tests -3.5dB**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs compliance testing using the SigTestWrapper.dll file.
   a. Calls the add-in card compliance test function from the SigTestWrapper.dll file.
   b. Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.
3. Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.
4. Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 2.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

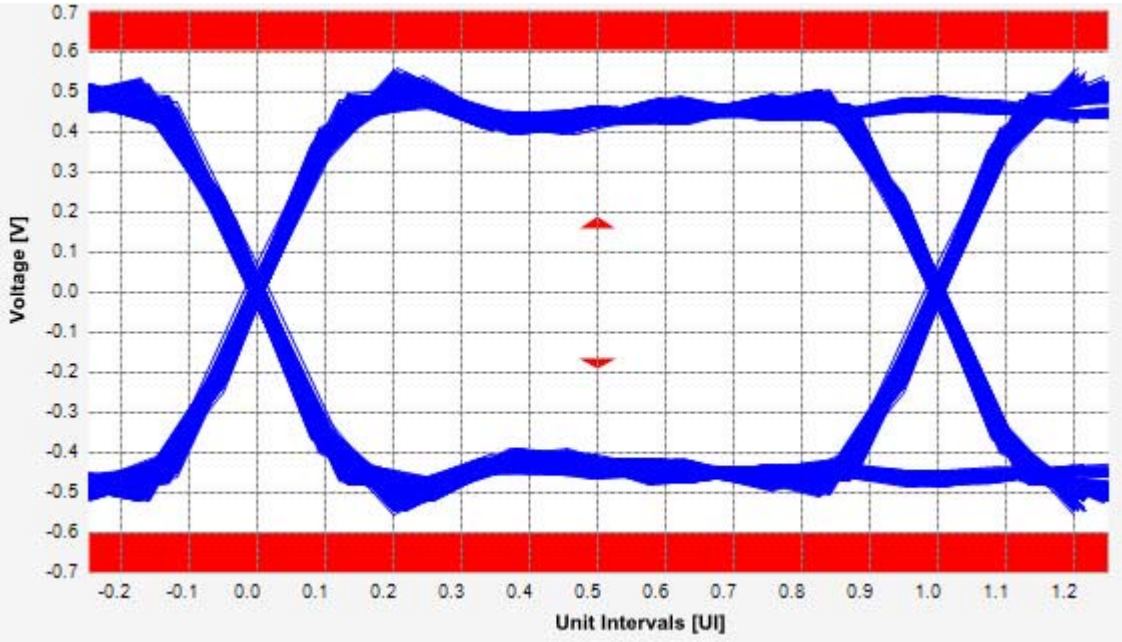


Figure 184 Reference Image for Template (Transition) Test

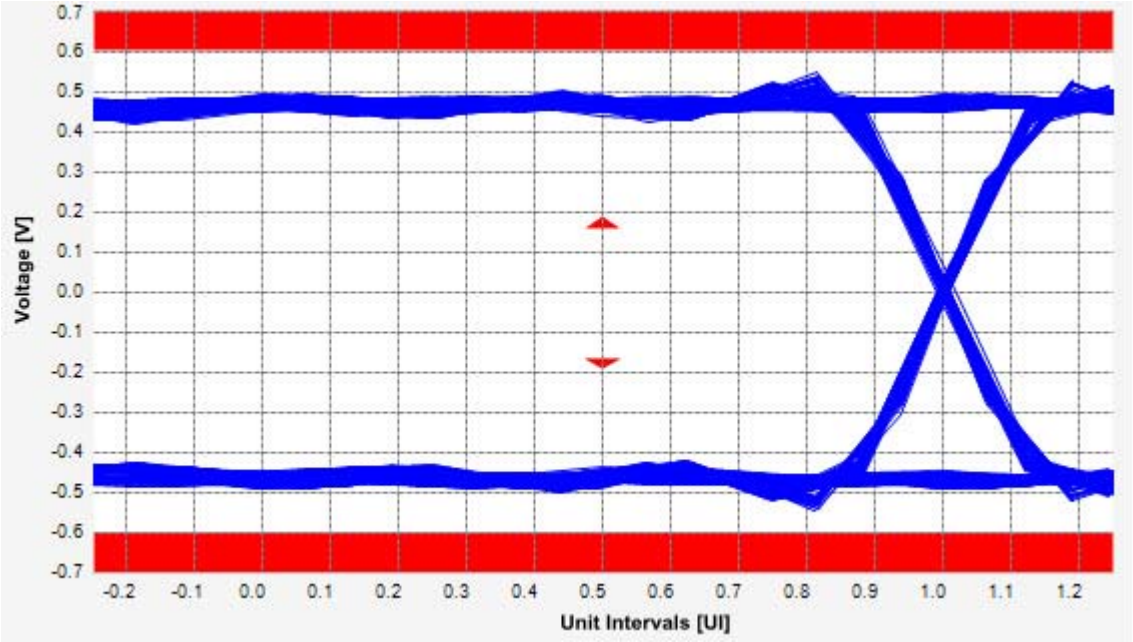


Figure 185 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

There exists two different tests for peak differential output voltage test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB as follows:

- Peak differential output voltage test -3.5dB (Non-transition)
- Peak differential output voltage test -6.0dB (Non-transition)

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.2, Table 4-8 and Table 4-10 is used as reference to check the compliance of the DUT.

Table 106 Peak Differential Output Voltage (Transition) -3.5dB De-emphasis Test Details

Symbol	Min	Max
V_{TXA}	380 mV	1200 mV
V_{TXA_d}	380 mV	1200 mV

Table 107 Peak Differential Output Voltage (Transition) -6.0dB De-emphasisTest Details

Symbol	Min	Max
V_{TXA}	306 mV	1200 mV
V_{TXA_d}	260 mV	1200 mV

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test.

- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
- The values in Table 4-8 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

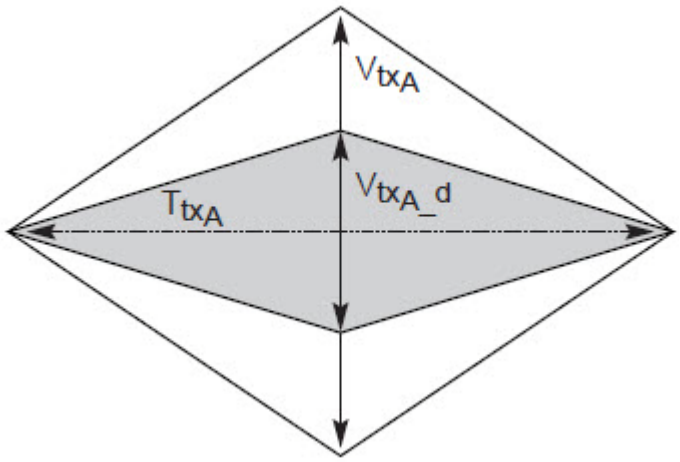


Figure 186 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 369 and select **Peak Differential Output Voltage -3.5dB (Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test (-3.5dB, -6.0dB) with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.

5 Reports the measurement results.fies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

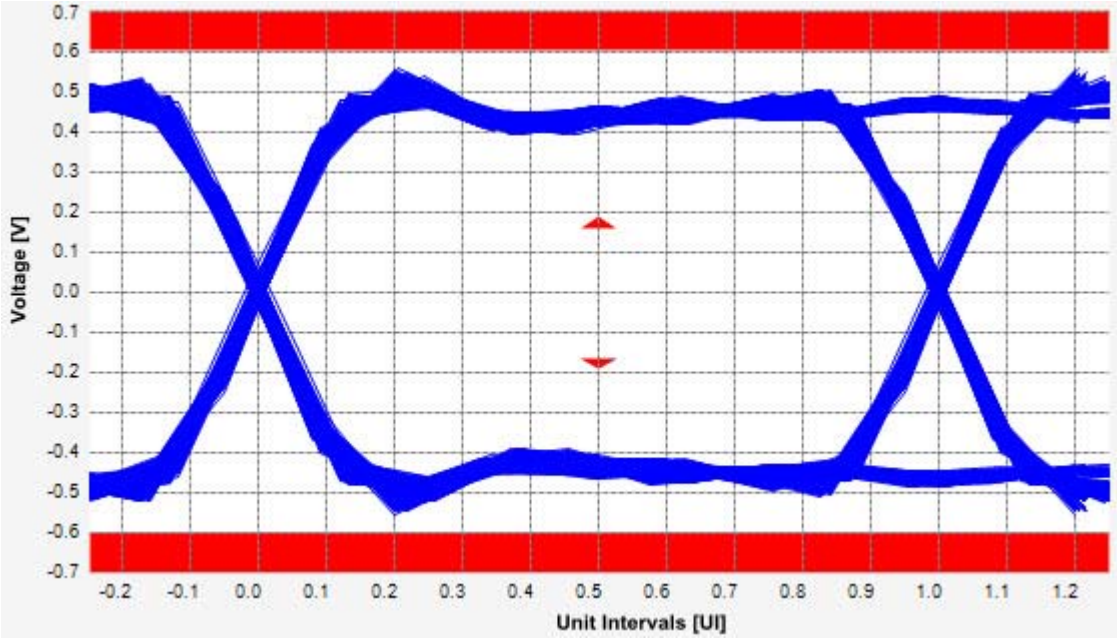


Figure 187 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

There exists two different tests for peak differential output voltage test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB as follows:

- Peak differential output voltage test -3.5dB (Non-transition)
- Peak differential output voltage test -6.0dB (Non-transition)

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.2, Table 4-8 and Table 4-10 is used as reference to check the compliance of the DUT.

Table 108 Peak Differential Output Voltage (Non-transition) -3.5dB De-emphasis Test Details

Symbol	Min	Max
V_{TXA}	380 mV	1200 mV
V_{TXA_d}	380 mV	1200 mV

Table 109 Peak Differential Output Voltage (Non-transition) -6.0dB De-emphasis Test

Symbol	Min	Max
V_{TXA}	306 mV	1200 mV
V_{TXA_d}	260 mV	1200 mV

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test.

- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
- The values in Table 4-8 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

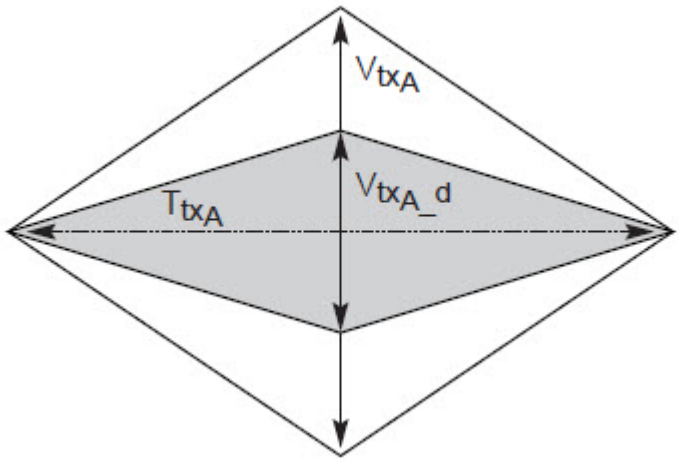


Figure 188 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 369 and select **Peak Differential Output Voltage -3.5dB (Non Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test (-3.5dB, -6.0dB) with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (non transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

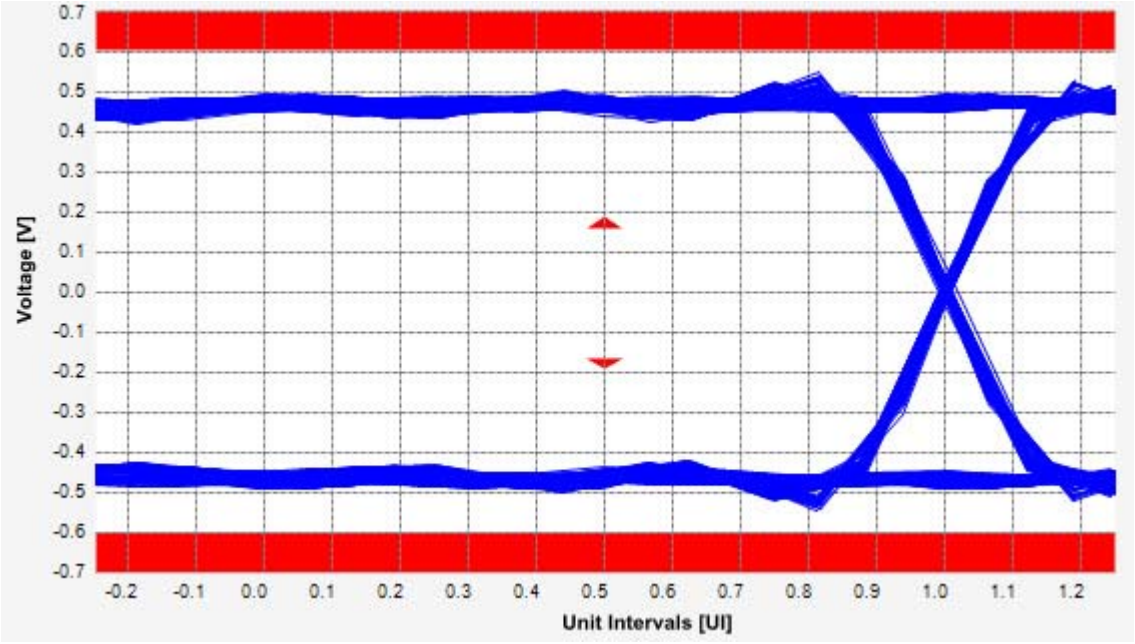


Figure 189 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER-12]$$

There exists four different tests for the eye-width test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB (for with and without crosstalk) as follows:

- Eye-width -3.5dB with crosstalk
- Eye-width -3.5dB without crosstalk
- Eye-width -6.0dB with crosstalk
- Eye-width -6.0dB without crosstalk

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.2 is used as reference to check the compliance of the DUT.

Table 110 Eye Width -3.5dB (with or without crosstalk) Test Details

Symbol	Min
$T_{TXA\ (with\ crosstalk)}$	123ps
$T_{TXA\ (without\ crosstalk)}$	126ps

Table 111 Eye Width -6.0dB (with or without crosstalk) Test Details

Symbol	Min
$T_{TXA\ (with\ crosstalk)}$	123ps
$T_{TXA\ (without\ crosstalk)}$	126ps

Test Definition Notes from the Specification

- An ideal reference clock without jitter is assumed for this specification. All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

- T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at BER10^{-12} must not exceed T_{TXA}. If the add-in card board uses non-interleaved routing, then crosstalk will be present in the measured data. If the add-in card board uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.
- The values in Table 4-8 are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

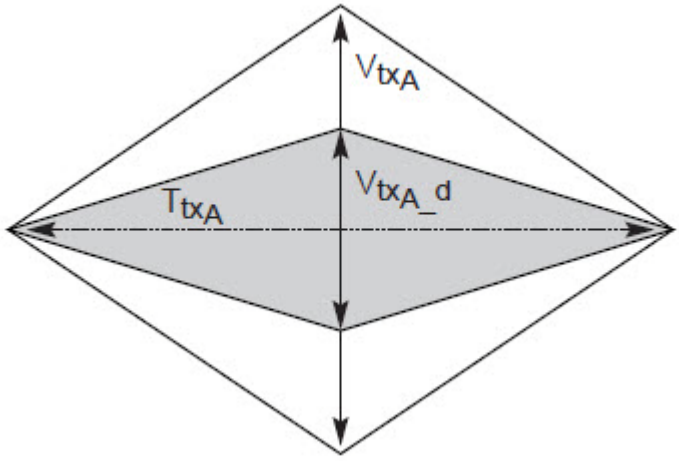


Figure 190 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 369 and select **Eye Width -3.5dB with crosstalk/Eye Width -3.5dB without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RMS Random Jitter Test

The **Random Jitter < 1.5MHz** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10kHz – 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists four different tests for the RMS random jitter test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB (for with and without crosstalk) as follows:

- RMS Random Jitter -3.5dB with crosstalk
- RMS Random Jitter -3.5dB without crosstalk
- RMS Random Jitter -6.0dB with crosstalk
- RMS Random Jitter -6.0dB without crosstalk

NOTE The RMS range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.2, Table 4-9 and Table 4-11 is used as reference to check the compliance of the DUT.

Table 112 RMS Random Jitter- 3.5dB/6.0dB (with or without crosstalk) Test Details

Parameter	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	57	77
Without crosstalk	54	74

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 369 and select **RMS Random Jitter -3.5dB with crosstalk/RMS Random Jitter -3.5dB without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Obtains the RMS Random Jitter test results from SigTestWrapper.dll file.

2 Compares the measured RMS Random Jitter values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.

3 Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Maximum Deterministic Jitter Test

The **Maximum Deterministic Jitter** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10kHz – 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists four different tests for the maximum deterministic jitter test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB (for with and without crosstalk) as follows:

- Maximum Deterministic Jitter -3.5dB with crosstalk
- Maximum Deterministic Jitter -3.5dB without crosstalk
- Maximum Deterministic Jitter -6.0dB with crosstalk
- Maximum Deterministic Jitter -6.0dB without crosstalk

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.2, Table 4-9 and Table 4-11 is used as reference to check the compliance of the DUT.

Table 113 Maximum Deterministic Jitter-3.5dB/6.0dB (with or without crosstalk) Test Details

Parameter	Max Dj (ps)
With crosstalk	57
Without crosstalk	54

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 369 and select **Maximum Deterministic Jitter -3.5dB with crosstalk/Maximum Deterministic Jitter -3.5dB without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1. Obtains the maximum deterministic jitter test results from the SigTestWrapper.dll file.
2. Compares the measured maximum deterministic jitter values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.
3. Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Jitter at BER-12 Test

The **Total Jitter at BER-12** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10kHz – 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists four different tests for the maximum deterministic jitter test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB (for with and without crosstalk) as follows:

- Total Jitter at BER-12 -3.5dB with crosstalk
- Total Jitter at BER-12 -3.5dB without crosstalk
- Total Jitter at BER-12 -6.0dB with crosstalk
- Total Jitter at BER-12 -6.0dB without crosstalk

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.2, Table 4-9 and Table 4-11 is used as reference to check the compliance of the DUT.

Table 114 Total Jitter at BER-12 -3.5dB/6.0dB (with or without crosstalk) Test Details

Parameter	Tj at BER 10^{-12}(ps)
With crosstalk	77
Without crosstalk	74

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 369 and select **Total Jitter at BER-12 -3.5dB with crosstalk/Total Jitter at BER-12 -3.5dB without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1. Obtains the total jitter at BER-12 test results from the SigTestWrapper.dll file.
2. Compares the measured total jitter at BER-12 values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.
3. Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

22 System Board (T_X) Tests, 5.0 GT/s, PCI-E 2.0

This section provides the Methods of Implementation (MOIs) for System Board (Tx) 5.0 GT/s tests of PCI-E 2.0 using an Agilent 90000X series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for System Board Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The are 2 types of PCI Express Signal Quality Load Board edge fingers combination available - x1 and x16 connectors, as well as x4 and x8 connectors.

The PCI Express Signal Quality Load Board will cause a PCI Express 2.0 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

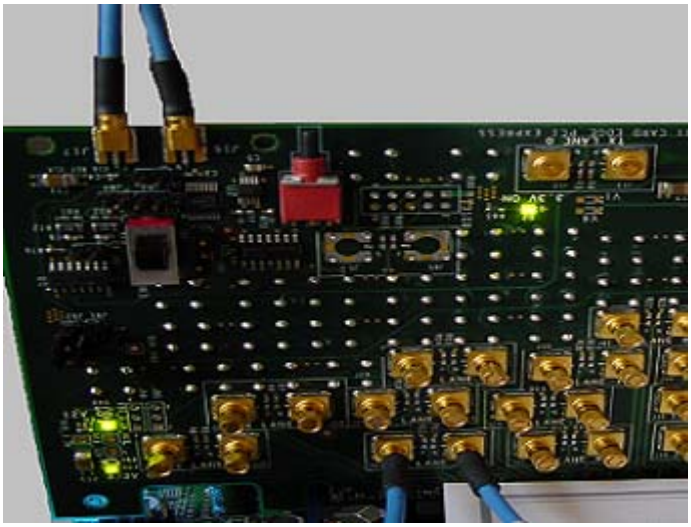


Figure 191 SMP Probing Option

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

a Digital Storage Oscilloscope channel 1 to Data and Channel 3 to Clock OR

b Digital Storage Oscilloscope channel 2 to Data and Channel 4 to Clock.

When SMP probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 626).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifiers and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

Running System Board Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "System Board (Tx) Tests" group.

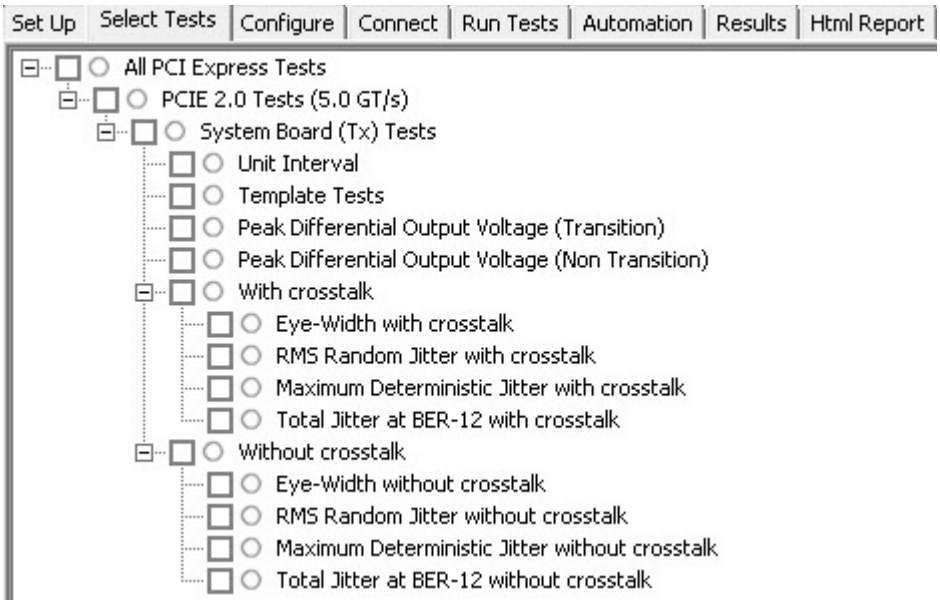


Figure 192 Selecting System Board (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.5, Table 4-9 is used as reference to check the compliance of the DUT.

Table 115 Unit Interval Test Details

Symbol	Parameter	Min	Max	Comments
UI	Unit Interval	199.94 ps	200.06 ps	For each reference clock source, the UI has tolerance of +/-300 ppm. Period does not account for SSC dictated variations.

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running System Board Tests" **on page 397** and select **Unit Interval.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

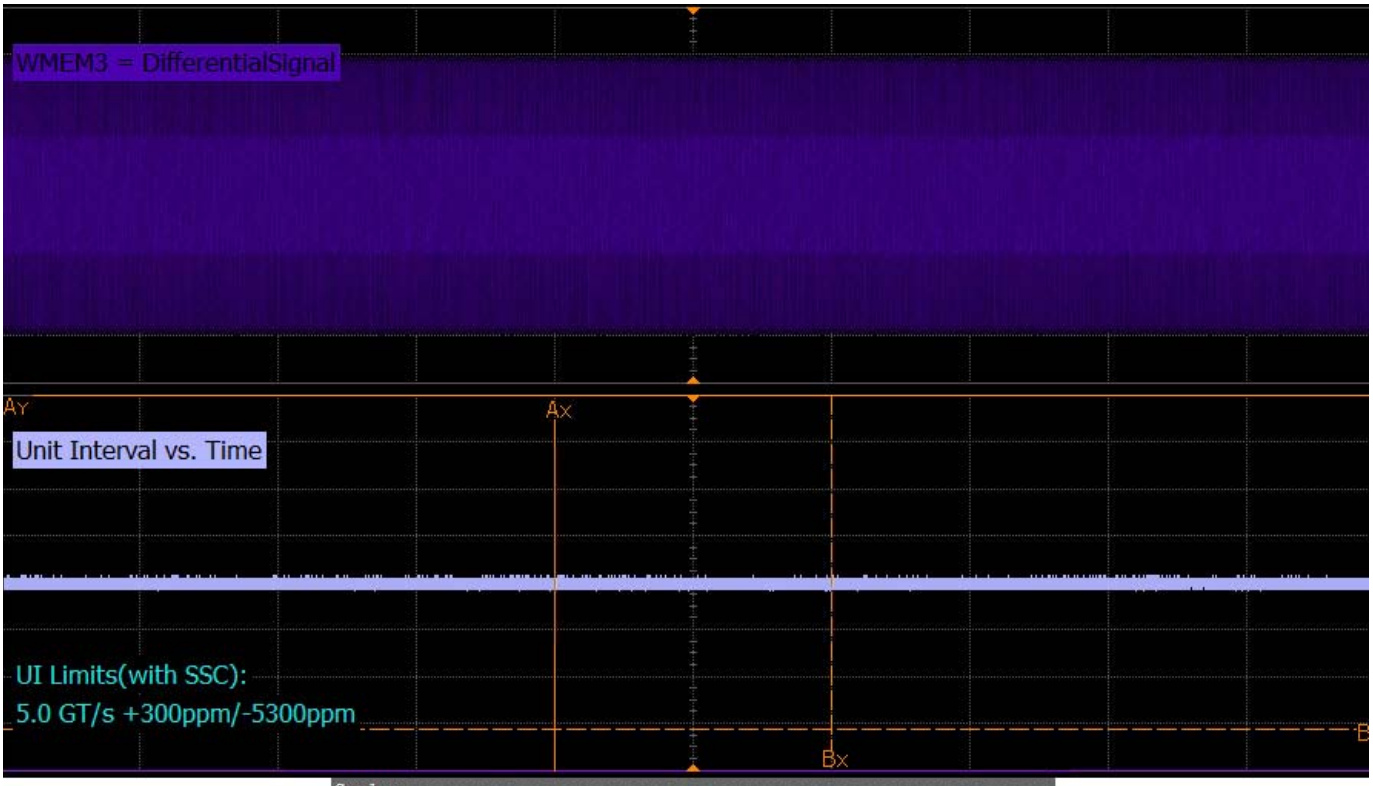
4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	32.00 µs/div	0.000s	20.00 fs/div	200.0 ps
Memory 3	32.00 µs/div	0.000s	162.5 mV/div	3.356 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-32.0000000080000 µs	200 pV
B	Function 3	32.0000000080000 µs	200 pV

Figure 193 Reference Image for Unit Interval Test

Template Tests

System boards must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 2.0, Section 4.7.6, Table 4-15 as measured after the connector with an ideal load.

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.6 is used as reference to check the compliance of the DUT.

Table 116 Template Test Details

Symbol	Min	Max
V_{TXS}	300 mV	1200 mV
V_{TXS_d}	300 mV	1200 mV
T_{TXS} (with crosstalk)	95 ps	
T_{TXS} (without crosstalk)	108 ps	

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test using the de-emphasis level that the system board wil use in normal operation.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
- T_{TXS} is the minimum eye width. The recommended sample size for the dual port measurement is at least 10^6 UI. The minimum eye opening at BER10^{-12} is calculated based on the measurement data and must not exceed T_{TXS}. If the system board uses non-interleaved routing, then crosstalk will be present in the measured data. If the add-in card board uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.
- The values in Table 4-15 are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

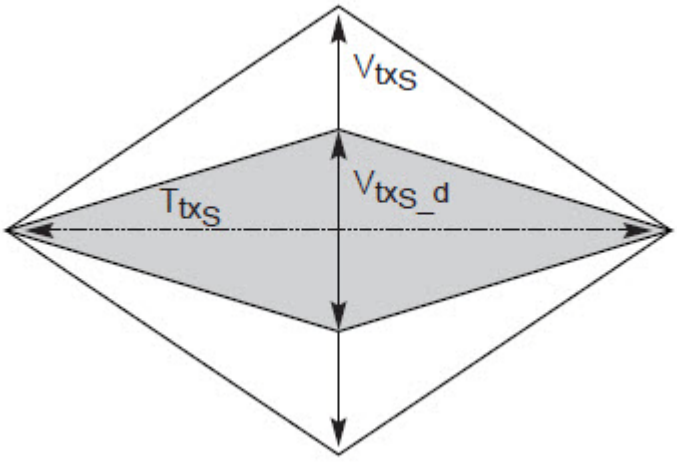


Figure 194 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running System Board Tests" on page 397 and select **Template Tests**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 2.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

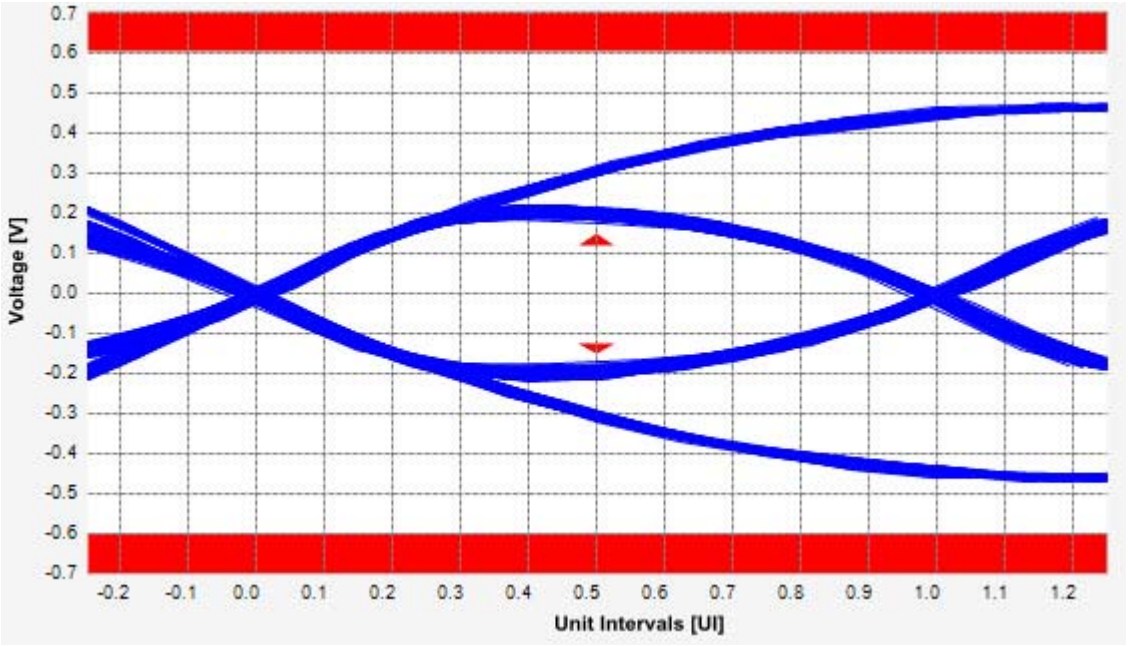


Figure 195 Reference Image for Template (Transition) Test

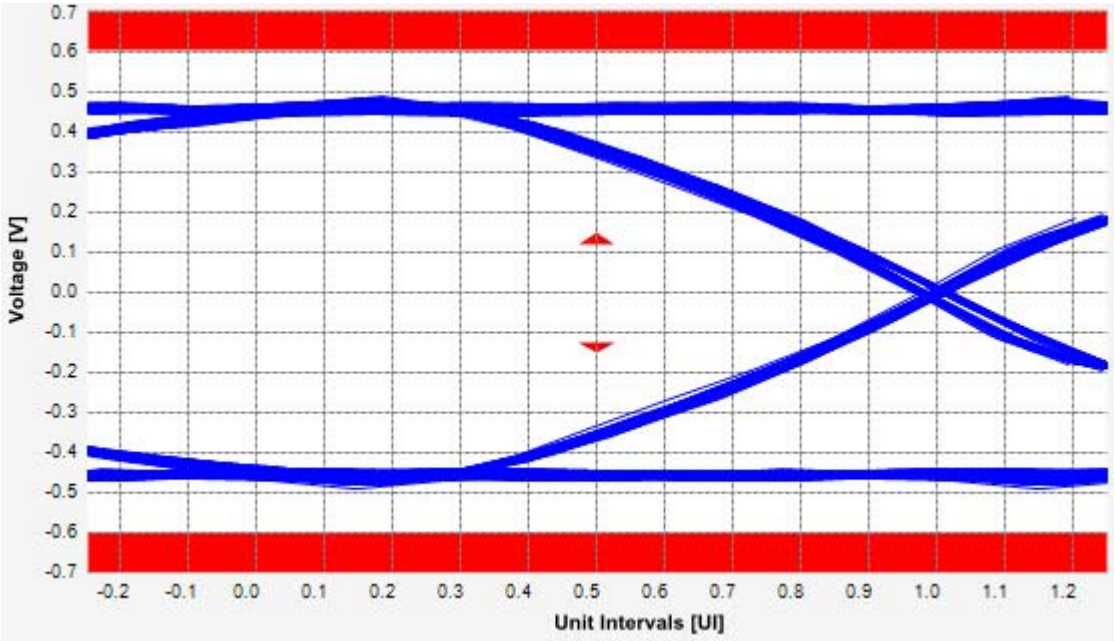


Figure 196 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-15 is used as reference to check the compliance of the DUT.

Table 117 Peak Differential Output Voltage (Transition) Test Details

Symbol	Min	Max
V_{TXS}	300 mV	1200 mV
V_{TXS_d}	300 mV	1200 mV

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test using the de-emphasis level that the system board wil use in normal operation.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
- The values in Table 4-15 are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

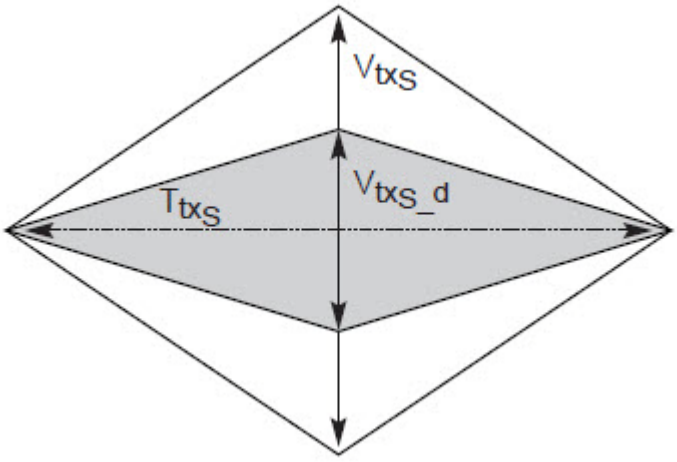


Figure 197 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 397 and select **Peak Differential Output Voltage (Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

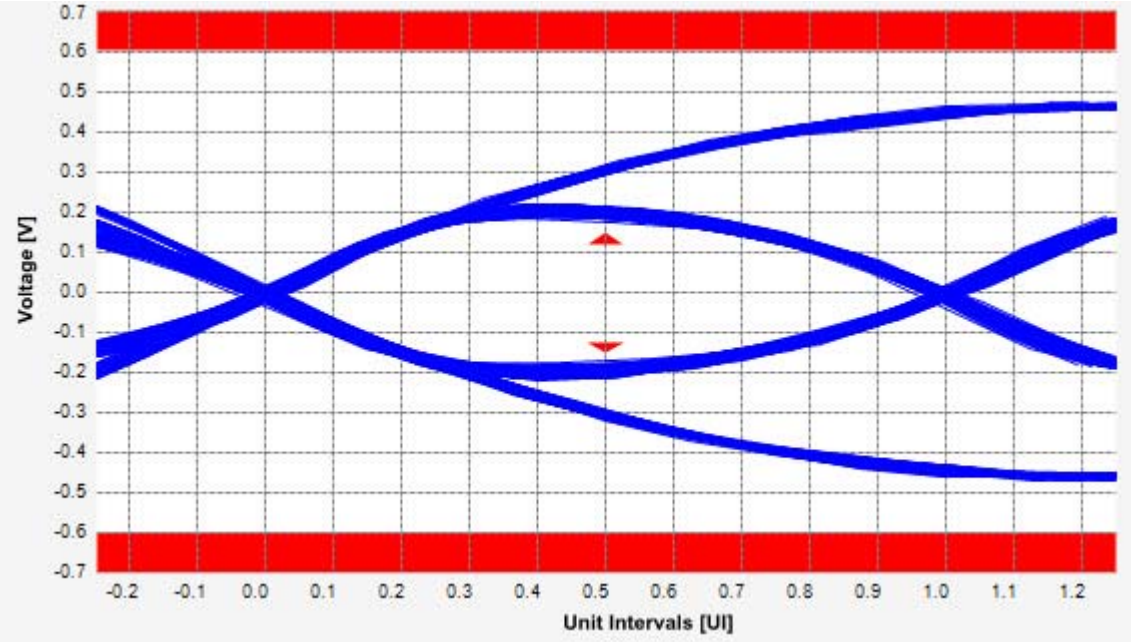


Figure 198 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-15 is used as reference to check the compliance of the DUT.

Table 118 Peak Differential Output Voltage (Non-transition) Test Details

Symbol	Min	Max
V_{TXA}	300 mV	1200 mV
V_{TXA_d}	300 mV	1200 mV

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test using the de-emphasis level that the system board wil use in normal operation.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
- The values in Table 4-15 are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

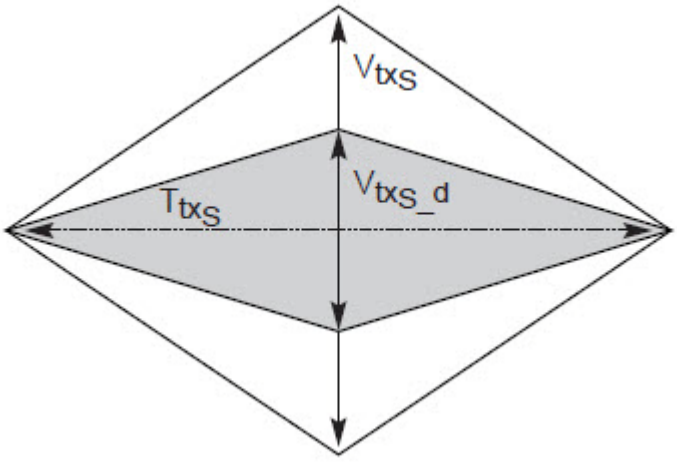


Figure 199 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 397 and select **Peak Differential Output Voltage (Non Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (non-transition) value to the compliance test limits.

5 Reports the measured peak differential output voltage (non-transition) value as the measurement result and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

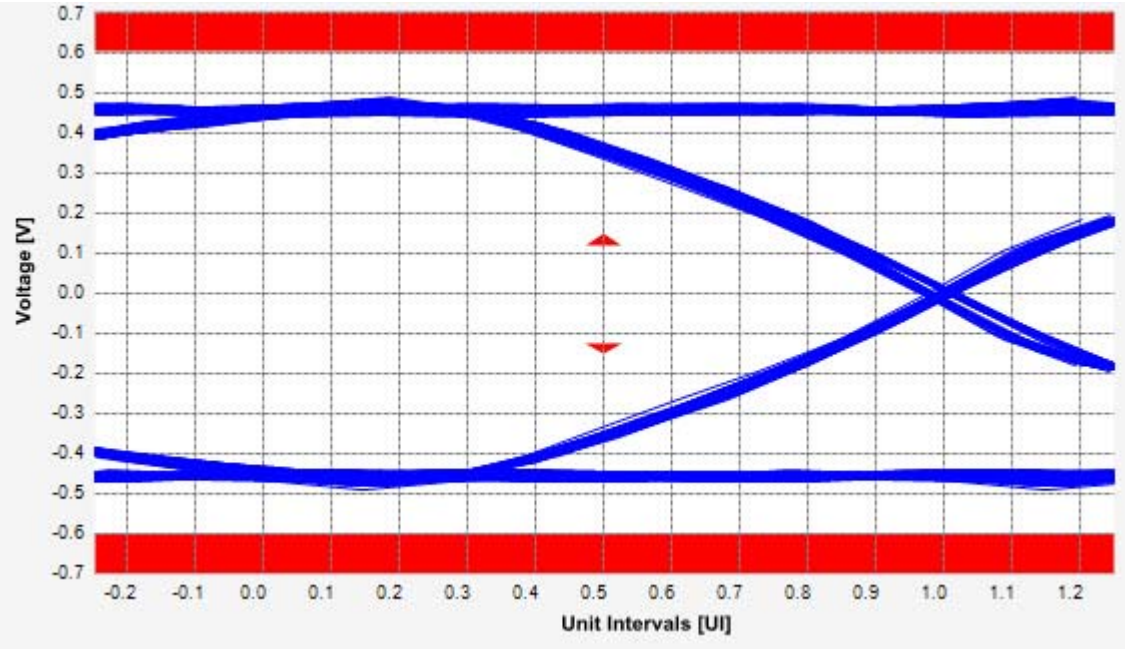


Figure 200 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER-12]$$

There exists two different tests for the eye-width test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB (for with and without crosstalk) as follows:

- Eye-width with crosstalk
- Eye-width without crosstalk

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.6 is used as reference to check the compliance of the DUT.

Table 119 Eye Width (with or without crosstalk) Test Details

Symbol	Min
$T_{TXS\ (with\ crosstalk)A}$	95ps
$T_{TXS\ (without\ crosstalk)}$	108ps

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (PCI Express Base Specification, Revision 2.0, Section 4.2.8) is being transmitted during the test using the de-emphasis level that the system board wil use in normal operation.
- T_{TXS} is the minimum eye width. The recommended sample size for the dual port measurement is at least 10^6 UI. The minimum eye opening at BER10^{-12} is calculated based on the measurement data and must not exceed T_{TXS}. If the system board uses non-interleaved routing, then crosstalk will be present in the measured data. If the add-in card board uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.
- The values in Table 4-15 are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge finger. Exact conditions required for verifying compliance while generating this eye diagram are given in the PHY Electrical Test Considerations for PCI Express Architecture document.

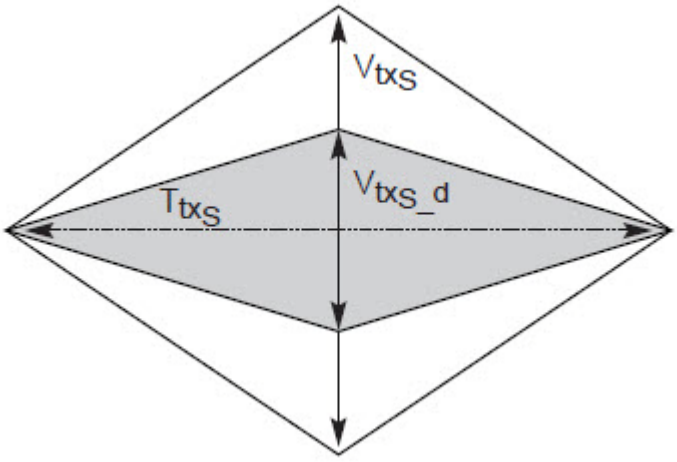


Figure 201 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 397 and select **Eye-Width with crosstalk/Eye-Width without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is

captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RMS Random Jitter Test

The **Random Jitter < 1.5MHz** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10kHz – 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists two different tests for the RMS random jitter test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB (for with and without crosstalk) as follows:

- RMS Random Jitter with crosstalk
- RMS Random Jitter without crosstalk

NOTE The RMS range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-16 is used as reference to check the compliance of the DUT.

Table 120 RMS Random Jitter (with or without crosstalk) Test Details

Parameter	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	57	105
Without crosstalk	44	92

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 397 and select **RMS Random Jitter with crosstalk/RMS Random Jitter without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Obtains the RMS Random Jitter test results from SigTestWrapper.dll file.

2 Compares the measured RMS Random Jitter values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.

3 Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Maximum Deterministic Jitter Test

The **Maximum Deterministic Jitter** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10kHz – 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists two different tests for the maximum deterministic jitter test with the same test procedure and exception of the compliance test limits used for the -3.5dB and 6.0 dB (for with and without crosstalk) as follows:

- Maximum Deterministic Jitter with crosstalk
- Maximum Deterministic Jitter without crosstalk

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-16 is used as reference to check the compliance of the DUT.

Table 121 Maximum Deterministic Jitter (with or without crosstalk) Test Details

Parameter	Max Dj (ps)
With crosstalk	57
Without crosstalk	54

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 397 and select **Maximum Deterministic Jitter with crosstalk/Maximum Deterministic Jitter without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Obtains the maximum deterministic jitter test results from the SigTestWrapper.dll file.

2 Compares the measured maximum deterministic jitter values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.

3 Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Jitter at BER-12 Test

The **Total Jitter at BER-12** test is a timing measurement in PCI Express 2.0 that requires separation of the high frequency jitter on the transmitter signal.

The transmitter is tested with a low jitter reference clock (clean clock). However, the reference clock may still have some low frequency wander. Besides that, the transmitter itself may have low frequency wander from VDD (supply voltage), temperature and other affects. In order to avoid this increasing observed transmitter jitter, jitter on the recovered clock is separated into different bands and measured.

- High frequency jitter (above 1.5 MHz) that is not tracked by the receiver and therefore reduces the transmitter eye width.
- Low frequency jitter (10kHz – 1.5MHz) that is mostly tracked by the receiver and used as part of the receiver testing.
- Jitter below 10 kHz that is considered wander or drift and are tracked by the receiver.

There exists two different tests for the maximum deterministic jitter test with the same test procedure and exception of the compliance test limits used with and without crosstalk as follows:

- Total Jitter at BER-12 with crosstalk
- Total Jitter at BER-12 without crosstalk

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-16 is used as reference to check the compliance of the DUT.

Table 122 Total Jitter at BER-12 (with or without crosstalk) Test Details

Parameter	Tj at BER 10^{-12}(ps)
With crosstalk	105
Without crosstalk	92

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 397 and select **Total Jitter at BER-12 with crosstalk/Total Jitter at BER-12 without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE2.0

Data Rate: 5.0GT/s

1 Obtains the total jitter at BER-12 test results from the SigTestWrapper.dll file.

2 Compares the measured total jitter at BER-12 values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.

3 Reports the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

23 Reference Clock Tests, 5.0 GT/s, PCI-E 2.0

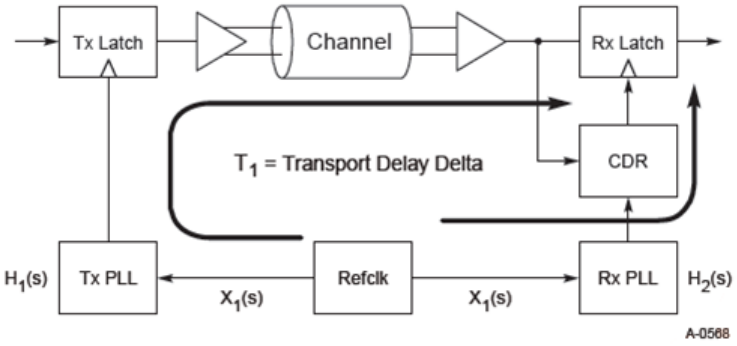
This section provides the Methods of Implementation (MOIs) for Reference Clock tests using a 90000X Series Infiniium oscilloscope, 1134A or 1169A probes, and the PCI Express Automated Test Application.

Reference Clock Architectures

For PCI-E 2.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



$$X_{CC}(s) = X_1(s) * H_{CC}(s)$$

$$H_{CC}(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} e^{-sT_1} - \frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \right]$$

Jitter contribution from H_1 Jitter contribution from H_2

Table 123 Difference Function Parameters Applied to the Refclk Measurement

Symbol	Parameter	Min	Max	Units	Comments
T_1	Data/clock transport delay delta		12	ns	See Note 1.
ω_1	PLL #1 natural frequency	4.31*2π or 1.82*2π		Mrad/s	See Notes 1, 2, and 3.
ζ_1	PLL #1 damping factor	0.54 or 1.16	1.75 (0.5 dB)		See Notes 1 and 2.
ω_2	PLL #2 natural frequency		8.61*2π	Mrad/s	See Note 1.
ζ_2	PLL #2 damping factor	0.54 or 1.16	1.75 (0.5 dB)		See Notes 1, 2, and 4.

NOTES:

1 T_1 defines the cumulative transport delay delta of the data and Refclk paths as shown in the above diagram and includes both off-chip and on-chip delay terms. The maximum internal transport delay for Tx and Rx is 2.0 ns.

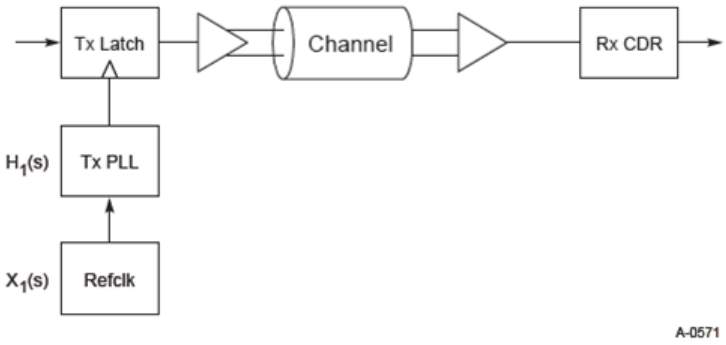
2 For the common Refclk Rx architecture, two possible combinations of minimum PLL BW and corresponding peaking are specified. If the min PLL BW is ≥5 MHz, then a max peaking of 1.0 dB (corresponding to ζ = 1.16) is required. If the min PLL BW is ≥8 MHz, then 3 dB of peaking (corresponding to ζ = 0.54) is allowed.

3 The natural frequency limits for PLL #1 correspond to –3 dB cut-off frequencies of 8.0 MHz (4.31e6*2π) and 5.0 MHz (1.82e6*2π).

4 The natural frequency limit for PLL #2 corresponds to a –3 dB cut-off frequency of 16 MHz.

Data Clock Architecture

This section describes the data driving architecture.



$$X_{DC}(s) = X_1(s) * H_1(s)$$

$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} \right]$$

Table 124 PLL Parameters for the Data Clocked Rx Architecture

Symbol	Parameter	Min	Max	Units	Comments
ω_1	Tx PLL natural frequency		8.61*2π	Mrad/s	See Note 1.
ζ_1	Tx PLL damping factor	0.54 (3.0 dB)	1.75 (0.5 dB)		See Notes 1 and 2.

NOTES:

1 The ω_1 and ζ_1 correspond to 16 MHz with 3.0 dB of peaking. Note that for the data driving architecture, we cannot take advantage of the differencing function for two PLLs and must instead apply the full 0-16 MHz/3.0 dB peaking PLL transfer function. Similarly, the lack of an Rx PLL obviates the need for defining a transport delay parameter.

2 A minimum peaking is also specified in order to place an upper limit on the amount of energy in the rolloff of the PLL. Since ζ_1 defines both the peaking and rolloff, a minimum and maximum for ζ_1 uniquely defines the amount of BW in the rolloff region.

Probing the Link for Reference Clock Compliance

Reference Clock tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the reference clock link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1134A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1134A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Card Electromechanical Specification) will be transmitted.

Table 125 Probing Options for Reference Clock Testing

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1134A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1134A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended SMA Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 – Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

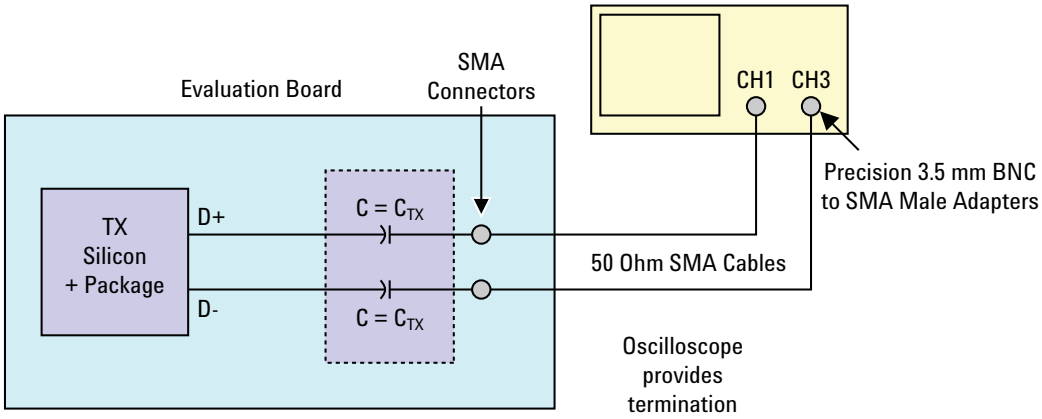


Figure 202 Single-Ended SMA Probing using Channel 1 and Channel 3

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 – Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the reference clock, as close as possible to the reference clock. Place single-ended grounds as close to the signal line's reference ground as possible. Channel-to-Channel deskew is required using this probing technique because two channels are used.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

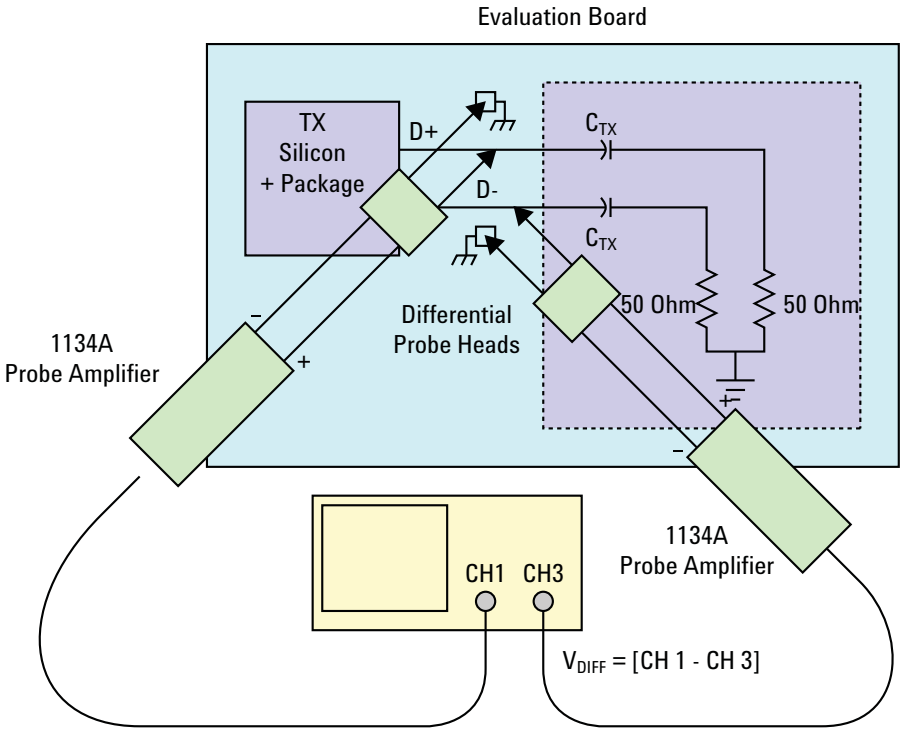


Figure 203 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the reference clock, as close as possible to the reference clock.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1134A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

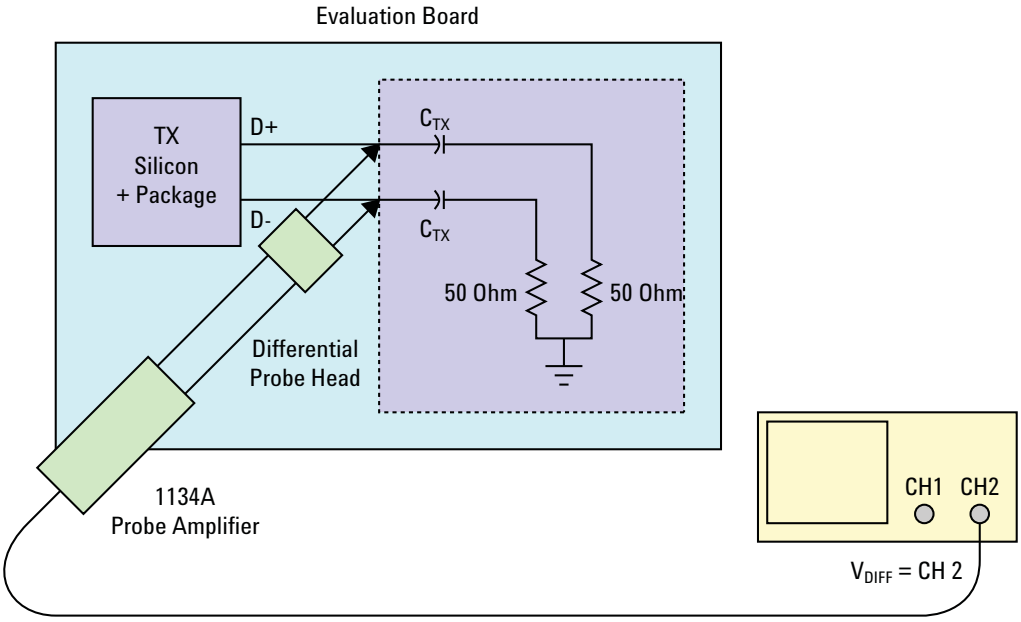


Figure 204 Differential Probing

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in Figure 4-25 of the Card Electromechanical Specification.

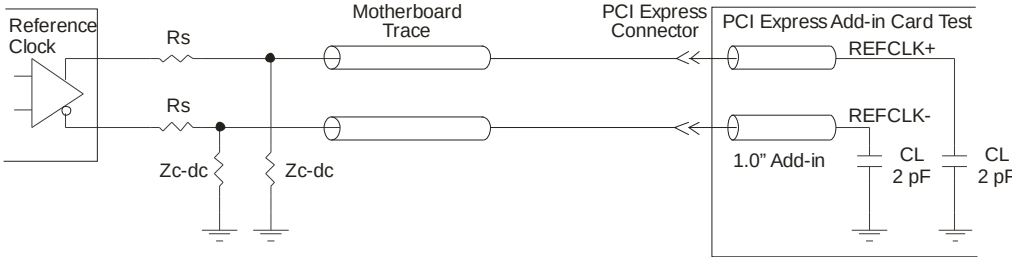


Figure 205 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to "Reference Clock Tests" in the "PCIE 2.0 Tests" group.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

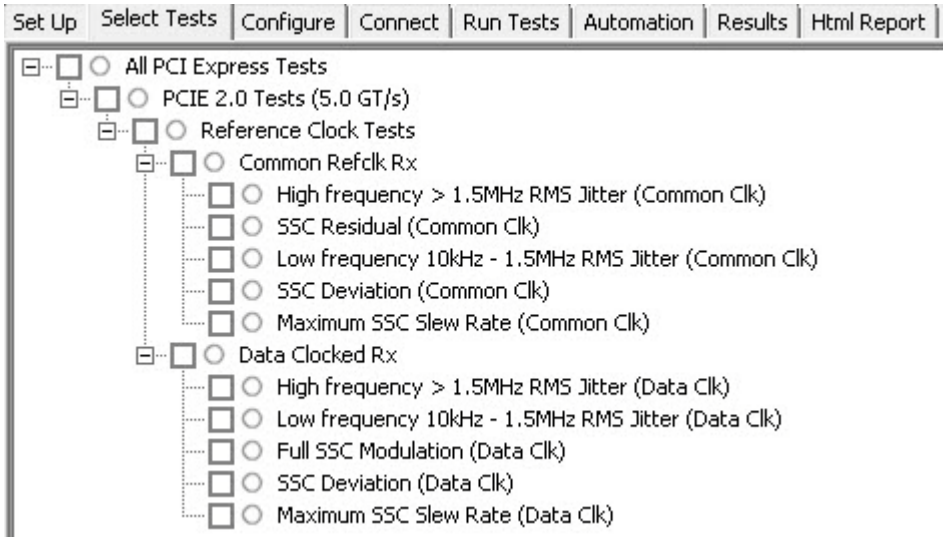


Figure 206 Selecting Reference Clock Tests when SSC is Selected

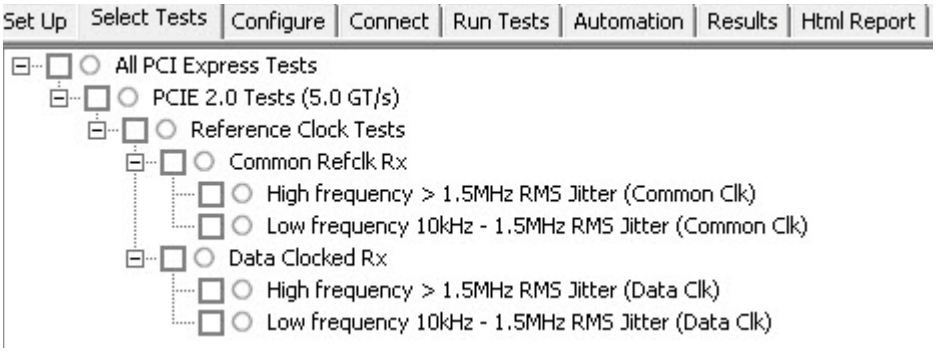


Figure 207 Selecting Reference Clock Tests when Clean Clock is Selected

High Frequency >1.5 MHz RMS Jitter (Common Clk) Test

This test verifies that the reference clock $T_{REFCLK-HF-RMS}$ is within the conformance limits specified in Table 4-31 of the PCIE Base Specification, rev. 3.0, version 0.71.

Test Reference

PCI Express Base Specification, Rev 3.0, Version 0.71, Section 4.3.12, Table 4-31 is used as reference to check the compliance of the DUT.

Table 126 High Frequency >1.5 MHz RMS Jitter (Common Clk) Test Details

Symbol	Description	Max
$T_{REFCLK-HF-RMS}$	>1.5MHz to Nyquist RMS jitter after applying Equation 4-3	3.1ps RMS

Test Definition Notes from the Specification

$T_{REFCLK-HF-RMS}$ is measured at the far end of the test circuit illustrated in Figure 4-88 after the filter function defined in Table 4-29 for common Refclk Rx for > 1.5 MHz jitter components has been applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 430 and select **High Frequency >1.5 MHz RMS Jitter (Common Clk)**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
3. Fits and displays all sample data on screen.
4. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example,

at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

6 Stitches each acquired acquisition to make a continuous TIE data.

7 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies a high pass filter to remove components which are <=1.5MHz.

   c Applies the PLL filter using parameters for common clocked architecture.

   d Converts back the frequency domain TIE data to time domains.

   e Computes the filtered peak-peak jitters and RMS jitter.

8 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

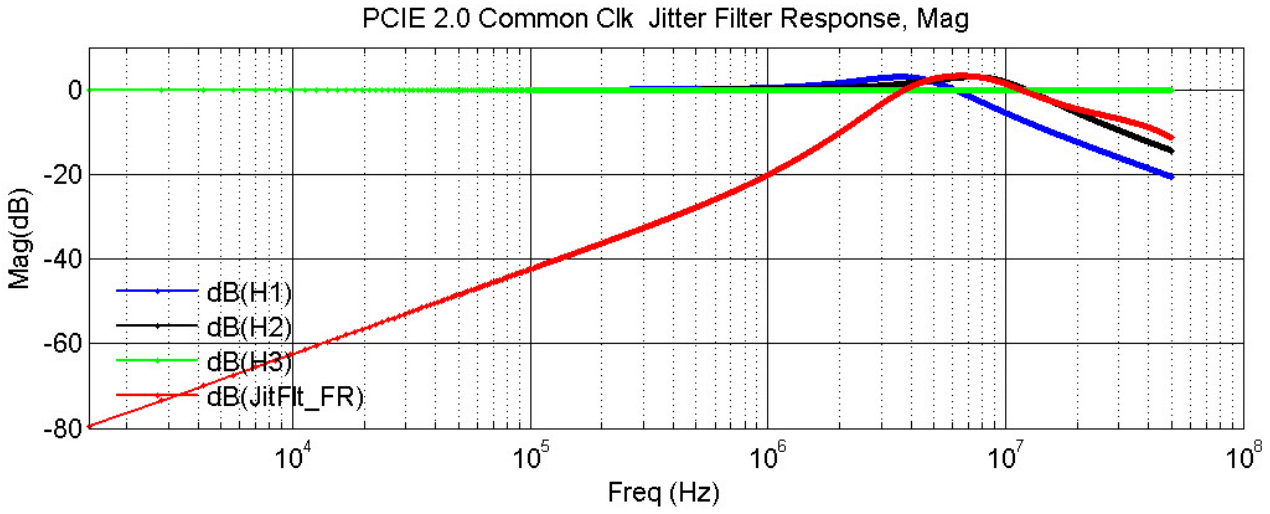


Figure 208 Common Clock Jitter Filter Response

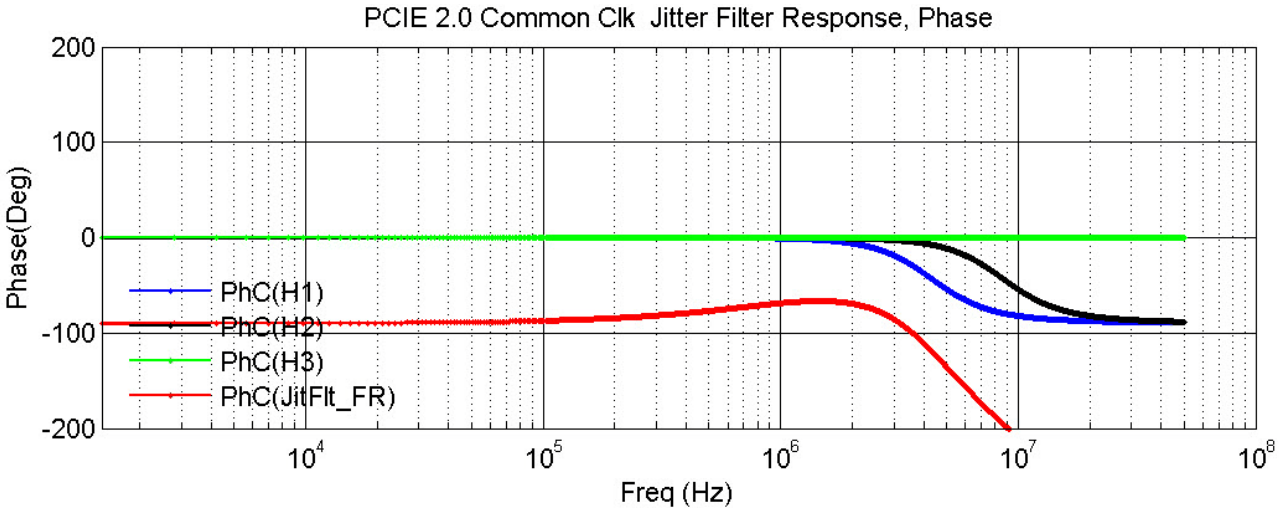


Figure 209 Common Clock Jitter Filter Response

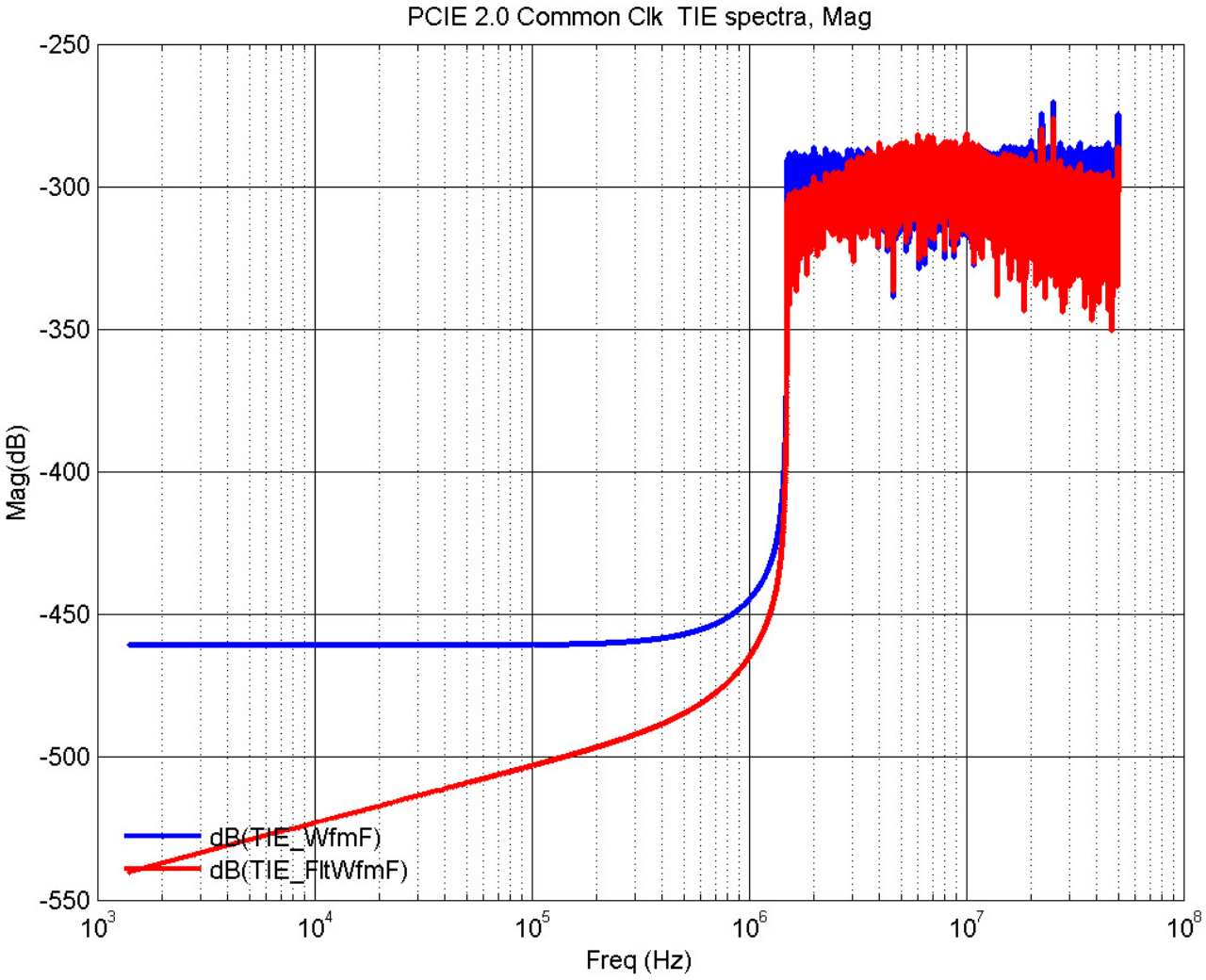


Figure 210 Common Clock TIE Spectra

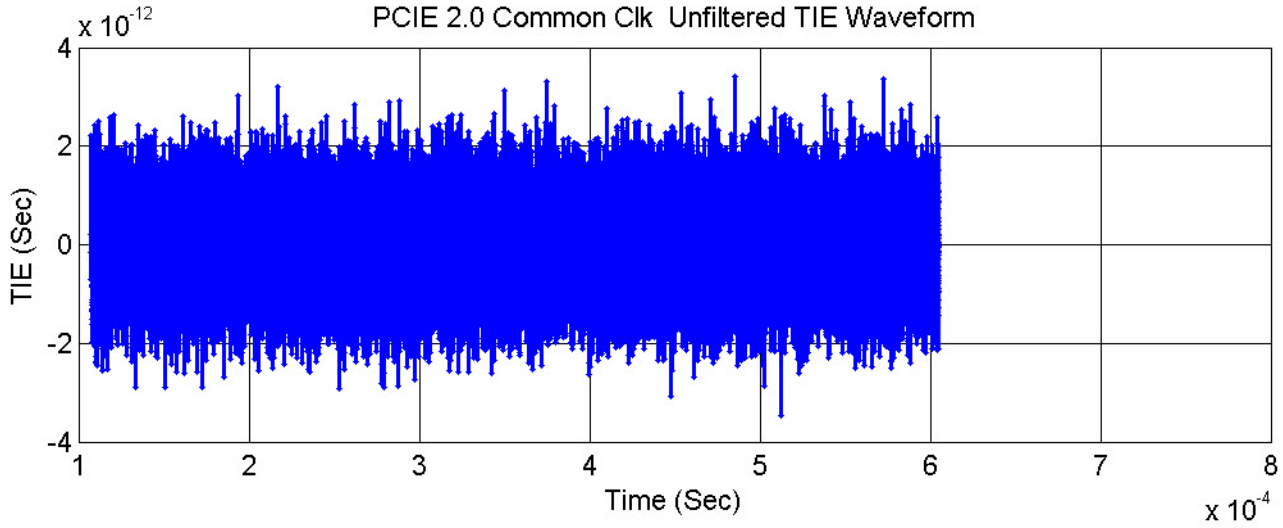


Figure 211 Common Clock Unfiltered TIE waveform

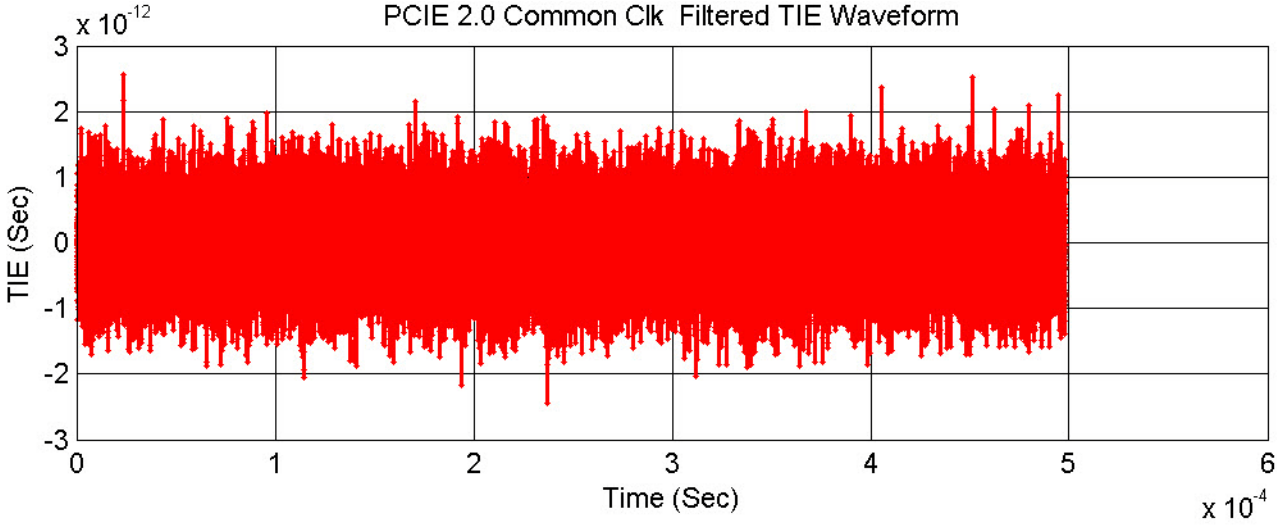


Figure 212 Common Clock Filtered TIE Waveform

SSC Residual (Common Clk) Test

This test verifies that the measured SSC residual is within the conformance limits specified in Table 4-31 of the PCIE Base Specification, rev. 3.0, version 0.71.

Test Reference

PCI Express Base Specification, Rev 3.0, version 0.71, section 4.3.12, Table 4-31 is used as reference to check the compliance of the DUT.

Table 127 SSC Residual (Common Clk) Test Details

Symbol	Description	Max
$T_{REFCLK-SSC-RES}$	SSC Residual	75ps RMS

Test Definition Notes from the Specification

$T_{REFCLK-HF-RMS}$ is measured at the far end of the test circuit illustrated in Figure 4-88 after the filter function defined in Table 4-29 for common Refclk Rx for > 1.5 MHz jitter components has been applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 430 and select **SSC Residual (Common Clk)**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
3. Fits and displays all sample data on screen.
4. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example,

at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

6 Stitches each acquired acquisition to make a continuous TIE data.

7 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies a high pass filter to remove components which are <=1.5MHz.

   c Applies the PLL filter using parameters for common clocked architecture.

   d Converts back the frequency domain TIE data to time domains.

   e Computes the filtered peak-peak jitters and RMS jitter.

8 Reports filtered peak-peak jitter as SSC residual and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Common Clk) Test

This test verifies that the reference clock $T_{REFCLK-HF-RMS}$ is within the conformance limits specified in, Table 4-31 of the PCIE Base Specification, rev. 3.0, version 0.71.

Test Reference

PCI Express Base Specification, Rev 3.0, version 0.71, Section 4.3.12, Table 4-31 is used as reference to check the compliance of the DUT.

Table 128 Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Common Clk) Test Details

Symbol	Description	Max
$T_{REFCLK-LF-RMS}$	10KHz - 1.5 MHz RMS jitter	3.0ps RMS

Test Definition Notes from the Specification

$T_{REFCLK-SSC-RES}$ and $T_{REFCLK-LF-RMS}$ are measured after the filter function defined in Table 4-29 for Common Refclk Rx for > 1.5MHz jitter components has been applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 430 and select **Low Frequency 10 kHz - 1.5 MHz RMS Jitter (Common Clk).**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
3. Fits and displays all sample data on screen.
4. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200

points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

6 Stitches each acquired acquisition to make a continuous TIE data.

7 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

- **a** Converts time domain TIE data to frequency domain.
- **b** Applies a band pass filter to remove components which are <10KHz and >1.5MHz.
- **c** Applies the PLL filter using parameters for common clocked architecture.
- **d** Removes SSC components (fundamental and harmonics).
- **e** Converts back the frequency domain TIE data to time domains.
- **f** Computes the filtered peak-peak jitters and RMS jitter.

8 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

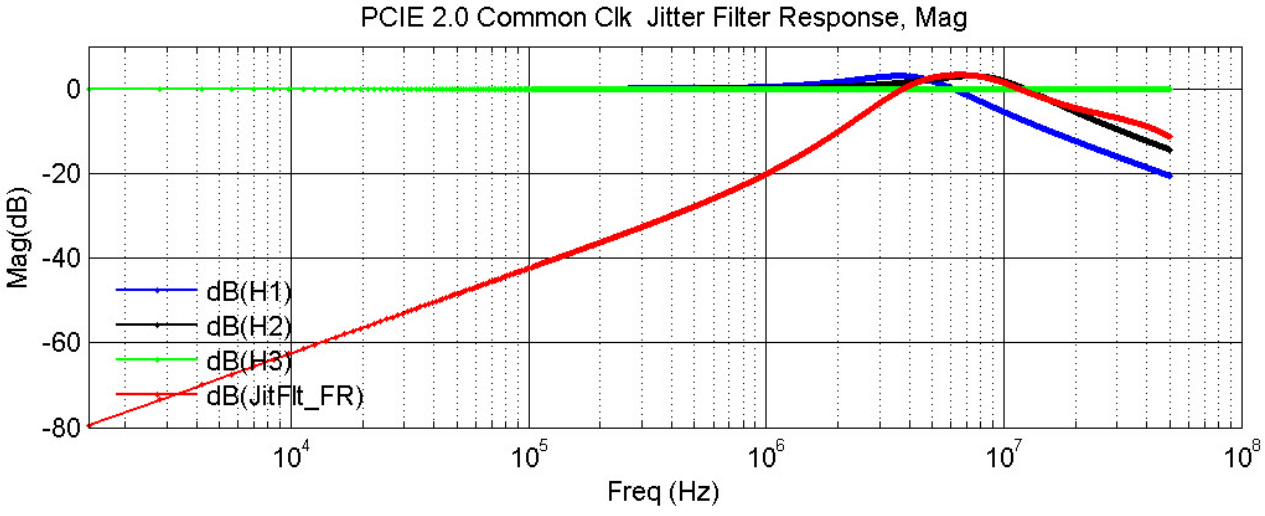


Figure 213 Common Clock Jitter Response

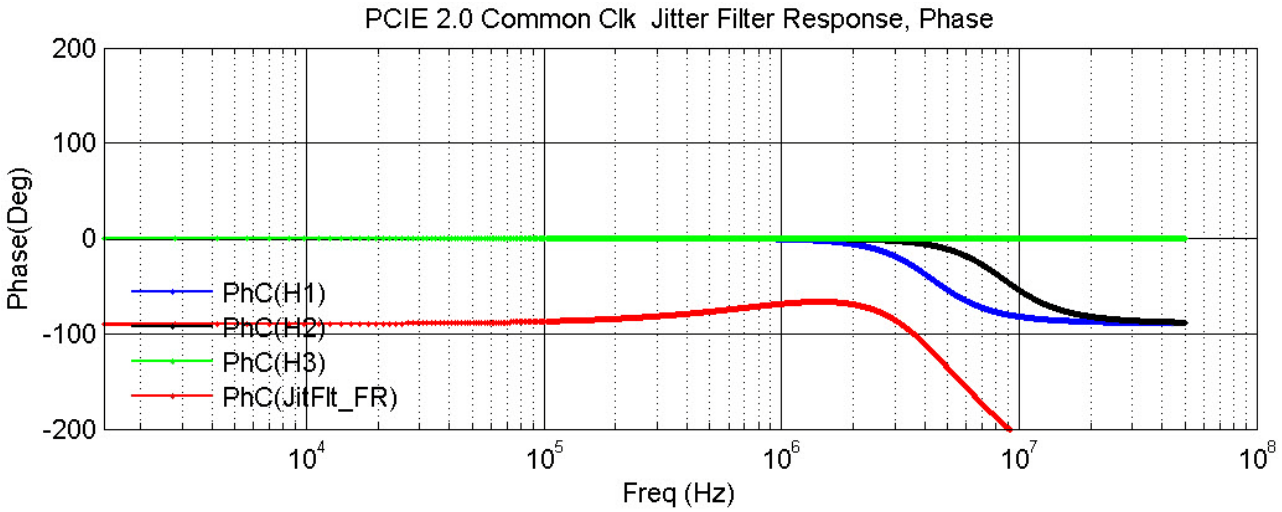


Figure 214 Common Clock Jitter Filter Response

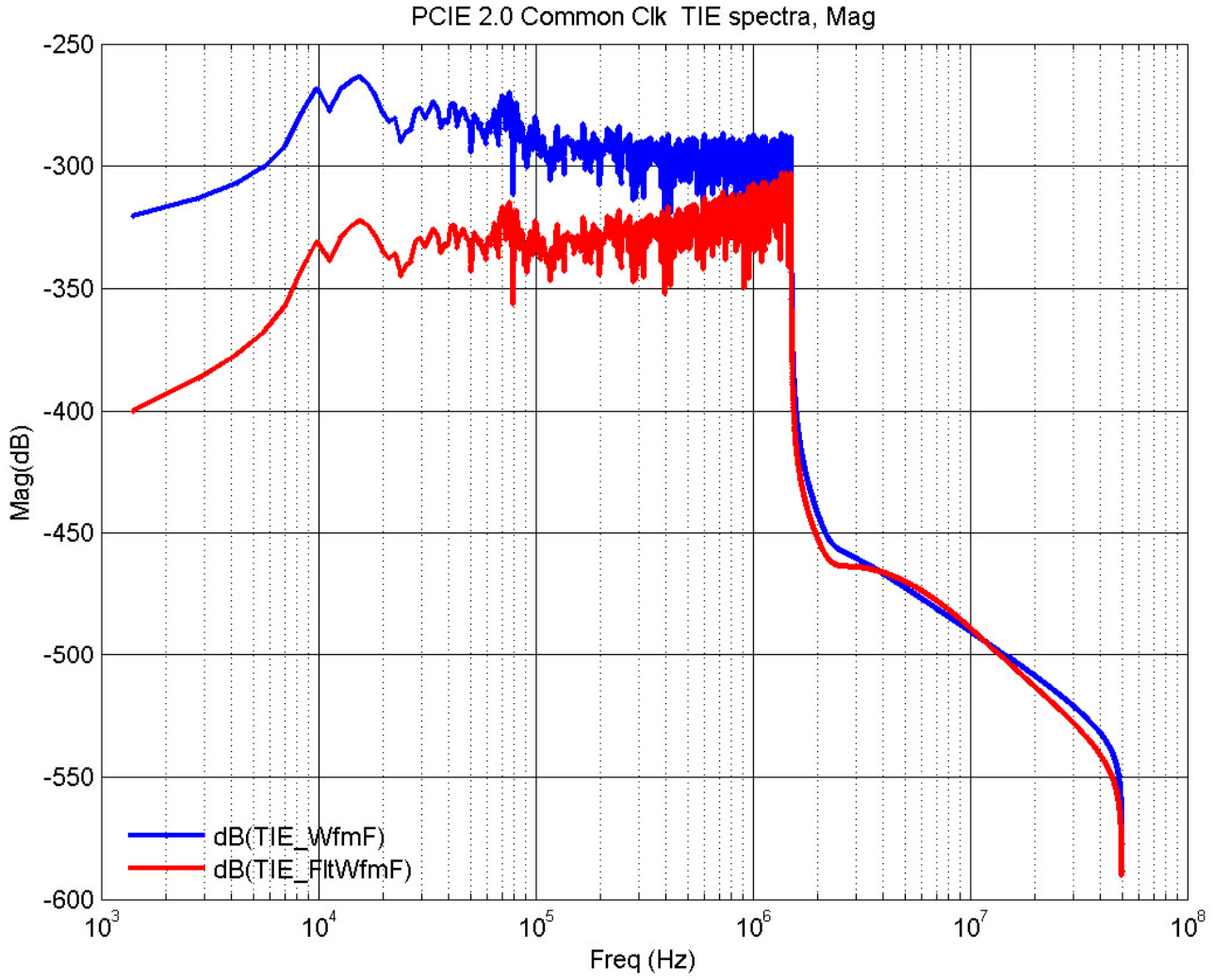


Figure 215 Common Clock TIE Spectra

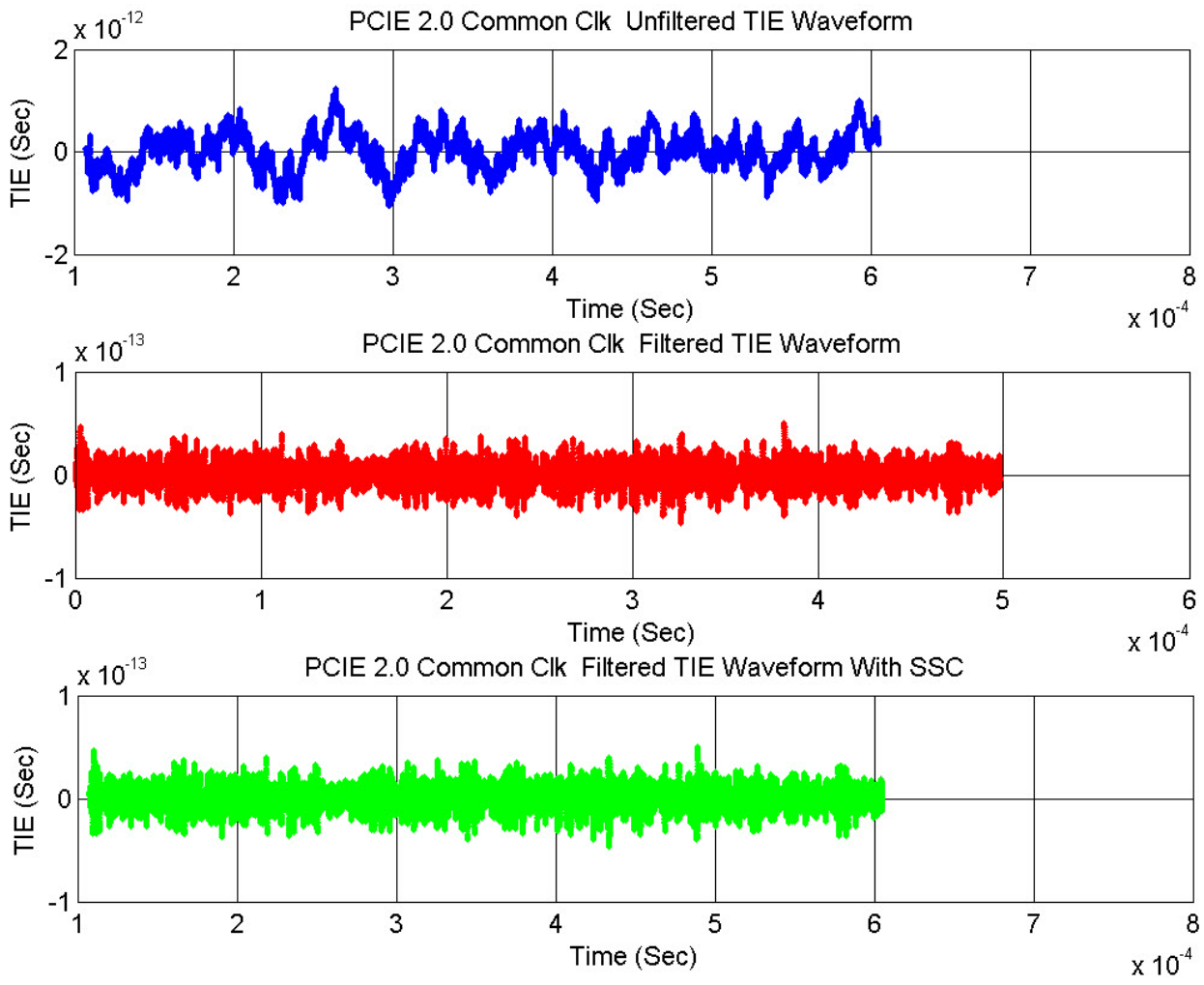


Figure 216 Common Clock TIE Waveform

SSC Deviation (Common Clk) Test

This test verifies that the reference clock SSC deviation is within the conformance limits specified in Table 4-31 of the PCIE Base Specification, rev. 3.0, version 0.71.

Test Reference

PCI Express Base Specification, Rev 3.0, version 0.71, Section 4.3.12, Table 4-31 is used as reference to check the compliance of the DUT.

Table 129 SSC Deviation (Common Clk) Test Details

Symbol	Description	Max
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	+0.0/-0.5%

Test Definition Notes from the Specification

$T_{REFCLK-SSC-RES}$ and $T_{REFCLK-LF-RMS}$ are measured after the filter function defined in Table 4-29 for Common Refclk Rx for > 1.5MHz jitter components has been applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 430 and select **SSC Deviation (Common Clk).**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.

4 Uses markers to indicate upper and lower limit (trend data of periodic measurements).

5 Measures Period_max, Period_min and Period_average.

6 Reports the measurement results.

7 Calculates SSC deviation% = (MaxPeriod - MinPeriod)/MinPeriod * 100%

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Maximum SSC Slew Rate (Common Clk) Test

This test verifies that the reference clock SSC slew rate is within the conformance limits specified in Table 4-31 of the PCIE Base Specification, rev. 3.0, version 0.71.

Test Reference

PCI Express Base Specification, Rev 3.0, version 0.71, Section 4.3.12, Table 4-31 is used as reference to check the compliance of the DUT.

Table 130 Maximum SSC Slew Rate (Common Clk) Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}PERIOD\text{-}SLEW}$	Maximum SSC df/dt	0.75 ps/UI

Test Definition Notes from the Specification

Defined for a worst case SSC modulation profile such as Lexmark.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 430 and select **Maximum SSC Slew Rate (Common Clk).**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

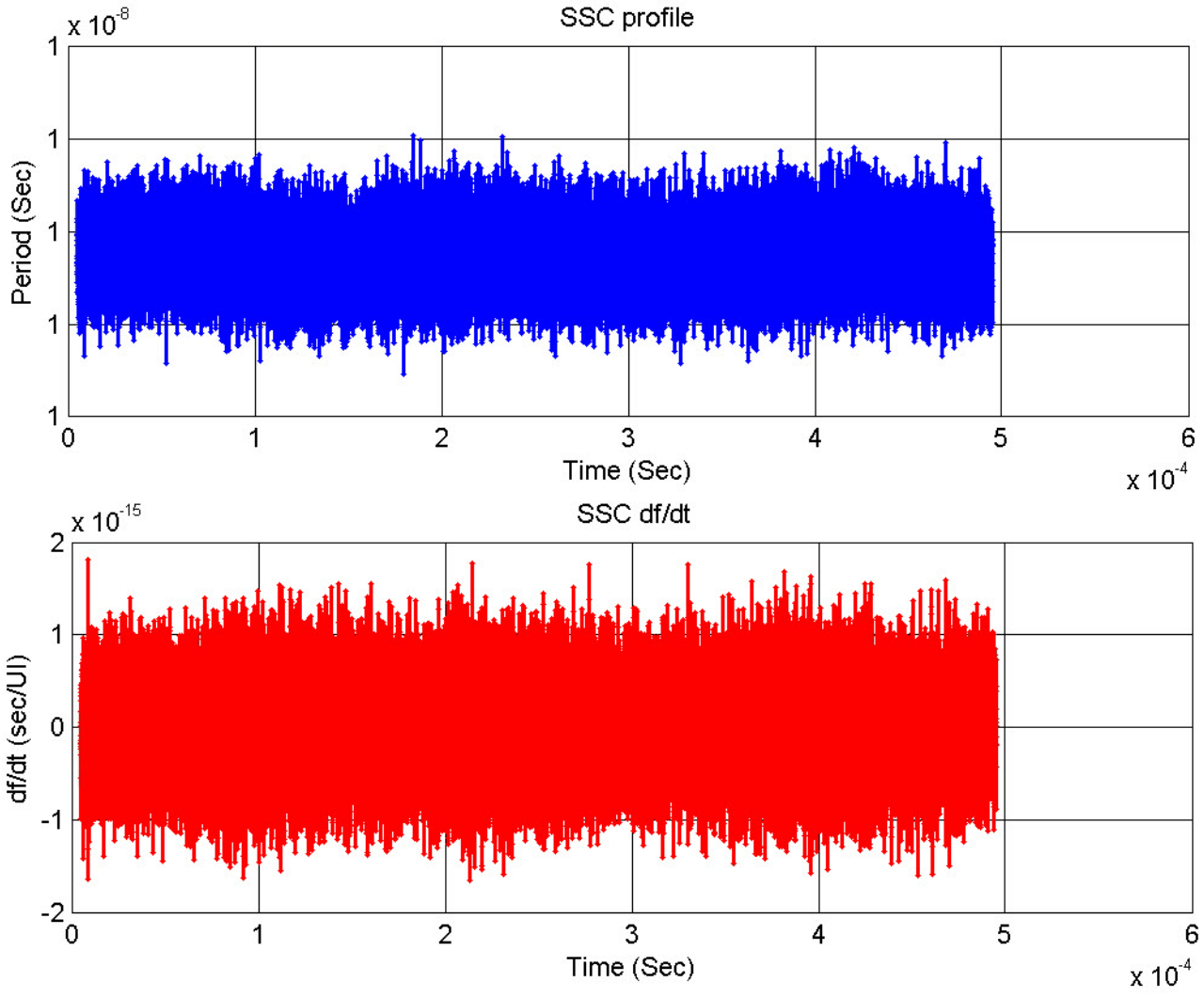
3 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.

4 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function generates a differential plot (x_n - x_{n-1}). The maximum slew rate corresponds to the peak of the differential plot.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.


SSC profile
x 10^-8
Period (Sec)
Time (Sec)
x 10^-4
SSC df/dt
x 10^-15
df/dt (sec/UI)
Time (Sec)
x 10^-4

High Frequency >1.5 MHz RMS Jitter (Data Clk) Test

This test verifies that the reference clock $T_{REFCLK-HF-RMS}$ is within the conformance limits specified in Table 4-33 of the PCIE Base Specification, rev. 3.0, version 0.71.

Test Reference

PCI Express Base Specification, Rev 3.0, version 0.71, Section 4.3.12, Table 4-33 is used as reference to check the compliance of the DUT.

Table 131 High Frequency >1.5 MHz RMS Jitter (Data Clk) Test Details

Symbol	Description	Max
$T_{REFCLK-HF-RMS}$	1.5 - Nyquist MHz RMS jitter after applying Equation 4-5	4.0 ps RMS

Test Definition Notes from the Specification

$T_{REFCLK-HF-RMS}$ is measured at the far end of the test circuit illustrated in Figure 4-88 after the filter function defined in Table 4-29 for common Refclk Rx for > 1.5 MHz jitter components has been applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 430 and select **High Frequency >1.5 MHz RMS Jitter (Data Clk).**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
3. Fits and displays all sample data on screen.
4. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example,

at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

6 Stitches each acquired acquisition to make a continuous TIE data.

7 Analyzes the stitched TIE data using a MATLAB (PCIEMatlabFunction) function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies a high pass filter to remove components which are <=1.5MHz.

   c Applies the PLL filter using parameters for data clocked architecture.

   d Converts back the frequency domain TIE data to time domains.

   e Computes the peak-peak jitters and RMS jitter.

8 Reports the peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

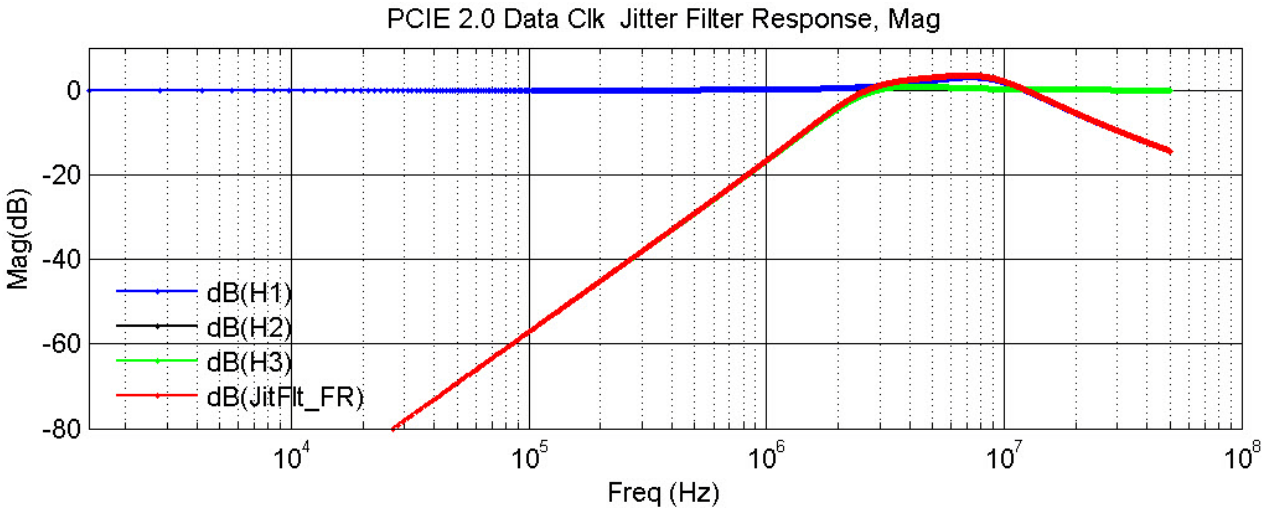


Figure 217 Data Clock Jitter Filter Response

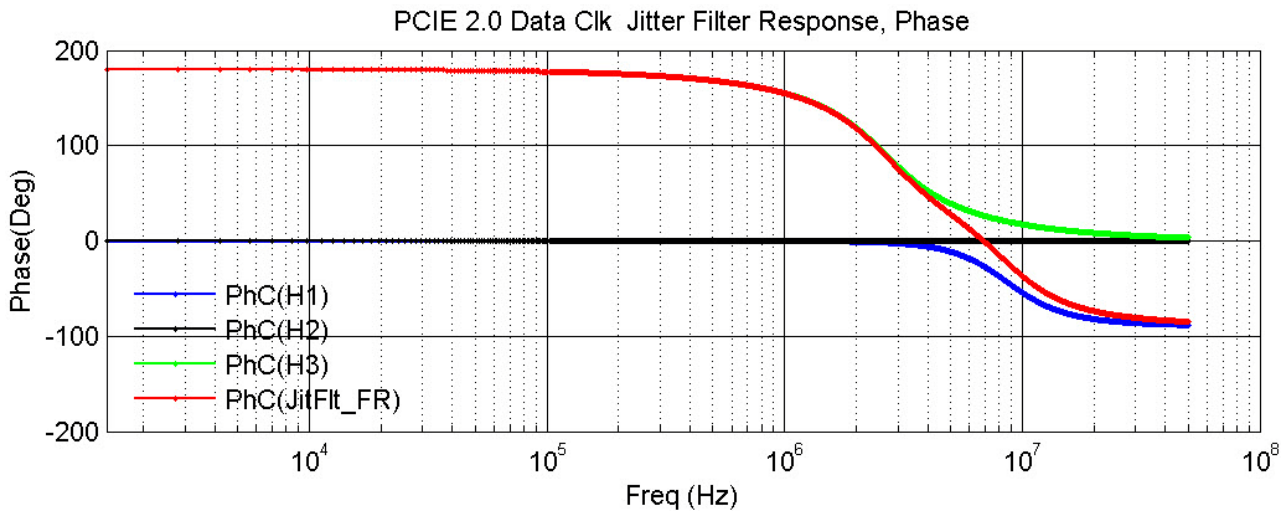


Figure 218 Data Clock Jitter Filter Response

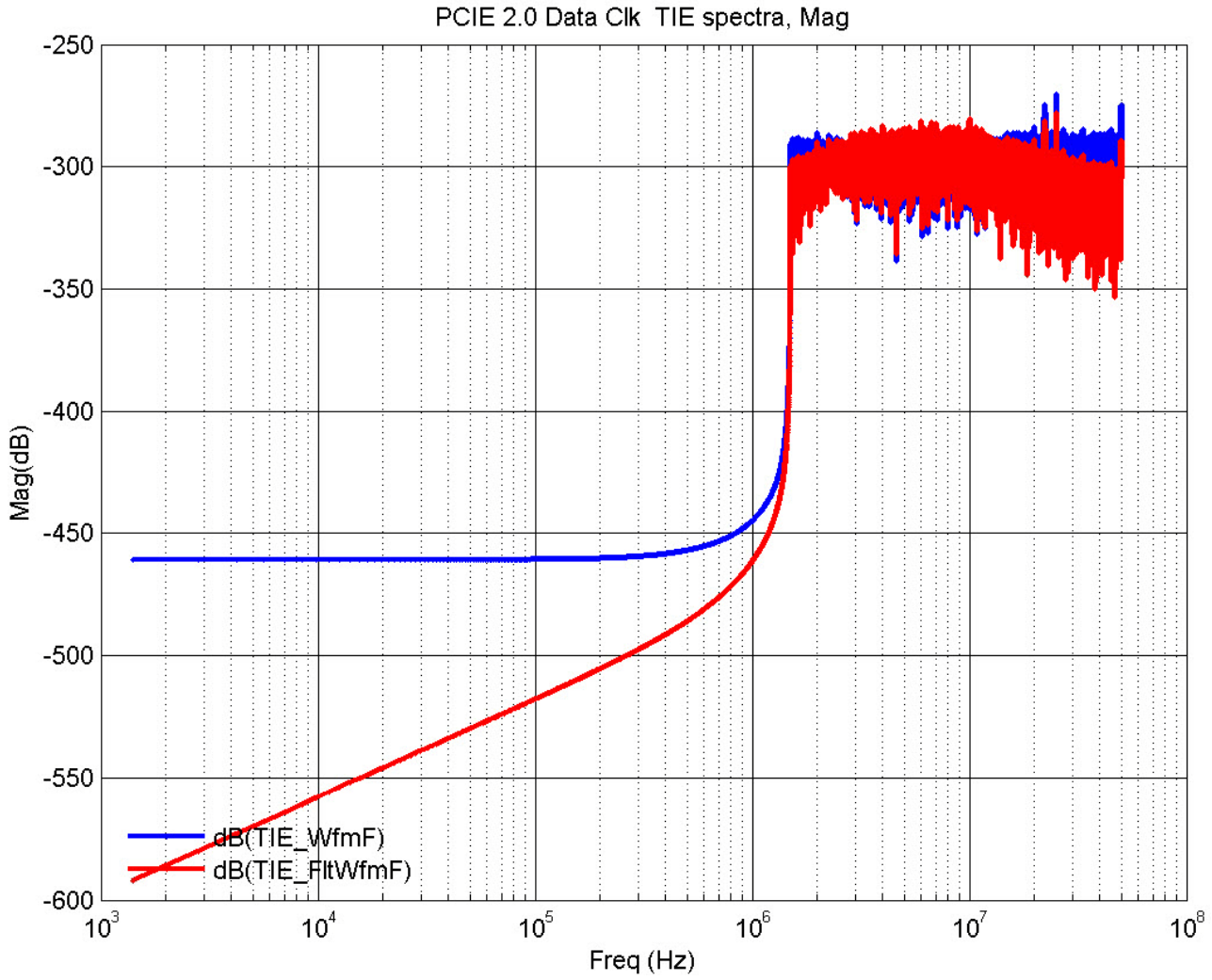

PCIE 2.0 Data Clk TIE spectra, Mag
-250
-300
-350
-400
-450
-500
-550
-600
Mag(dB)
dB(TIE_WfmF)
dB(TIE_FltWfmF)
10^3
10^4
10^5
10^6
10^7
10^8
Freq (Hz)

Figure 219 Data Clock TIE Spectra

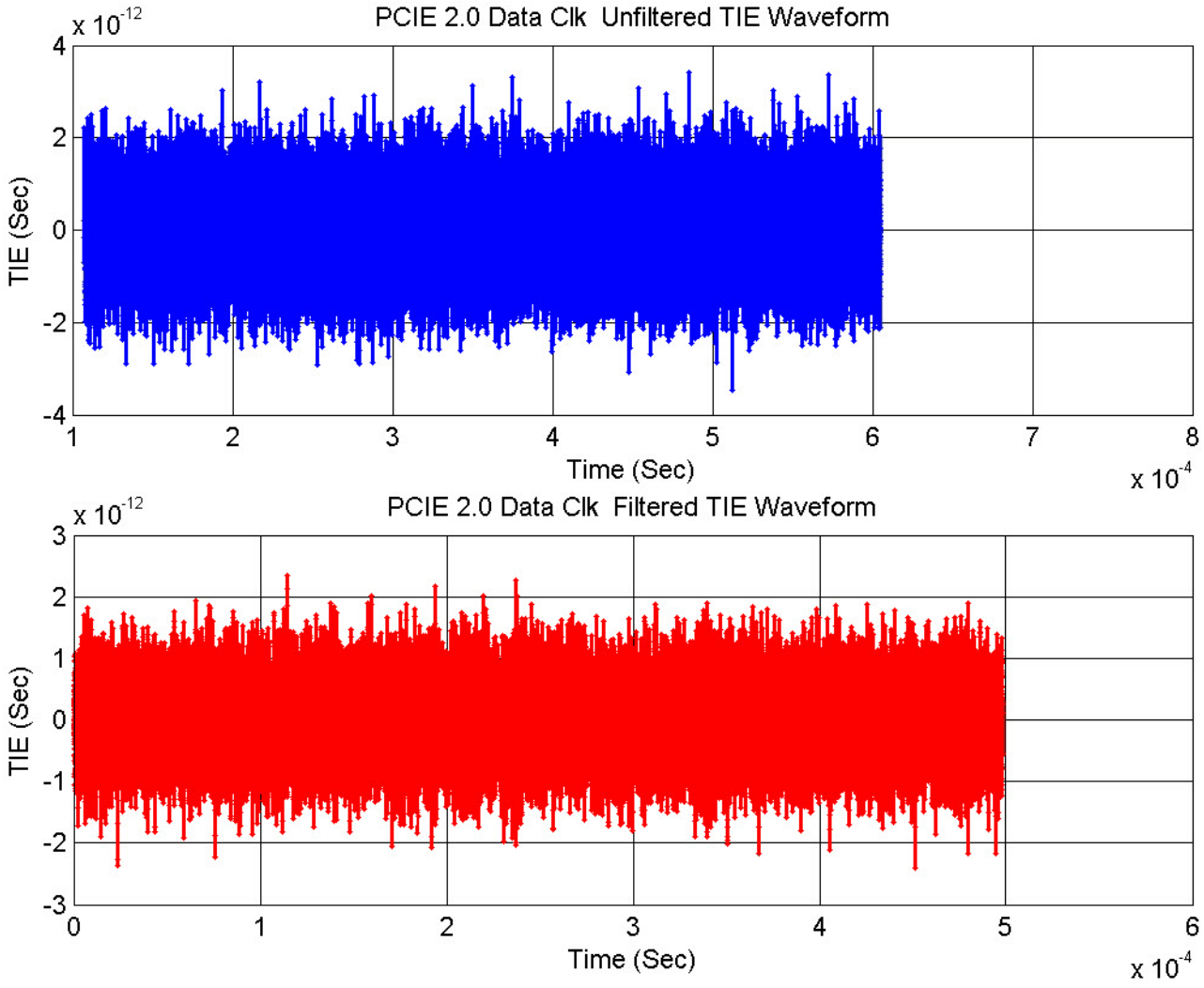


Figure 220 Common Clock Unfiltered/Filtered TIE Waveform

Full SSC Modulation (Data Clk) Test

This test verifies that the reference clock full SSC modulation is within the conformance limits specified in Table 4-33 of the PCIE Base Specification, rev. 3.0, version 0.71.

Test Reference

PCI Express Base Specification, Rev 3.0, version 0.71, Section 4.3.12, Table 4-33 is used as reference to check the compliance of the DUT.

Table 132 Full SSC Modulation (Data Clk) Test Details

Symbol	Description	Max
$T_{REFCLK-SSC-FULL}$	Full SSC modulation corresponding to +0 -0.5%	20 ns

Test Definition Notes from the Specification

- $T_{REFCLK-HF-RMS}$ is measured at the far end of the test circuit illustrated in Figure 4-88 after the filter function defined in Table 4-29 for common Refclk Rx for > 1.5 MHz jitter components has been applied.
- $T_{REFCLK-SSC-RES}$ and $T_{REFCLK-LF-RMS}$ are measured after the filter function defined in Table 4-29 for Common Refclk Rx for > 1.5MHz jitter components has been applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 430 and select **Full SSC Modulation (Data Clk).**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.

3 Fits and displays all sample data on screen.

4 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.

5 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

6 Stitches each acquired acquisition to make a continuous TIE data.

7 Analyzes the stitched TIE data using a MATLAB (PCIEMatlabFunction) function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies a band pass filter to remove components which are <=10KHz and components which are >=1.5MHz.

   c Applies the PLL filter using parameters for data clocked architecture.

   d Converts back the frequency domain TIE data to time domains.

   e Computes the peak-peak jitters. This value corresponds to the full SSC modulation since the SSC components were not removed.

8 Reports the peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Data Clk) Test

This test verifies that the RMS reference clock phase jitter at a bit error rate of $10E^{-6}$ is within the conformance limits specified in Table 4-33 of the PCIE Base Specification, rev. 3.0, version 0.71.

Test Reference

PCI Express Base Specification, Rev 3.0, version 0.71, Section 4.3.12, Table 4-33 is used as reference to check the compliance of the DUT.

Table 133 Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Data Clk) Test Details

Symbol	Description	Max
$T_{REFCLK-LF-RMS}$	10kHz - 1.5 MHz RMS jitter	7.5 ps RMS

Test Definition Notes from the Specification

$T_{REFCLK-SSC-RES}$ and $T_{REFCLK-LF-RMS}$ are measured after the filter function defined in Table 4-29 for Common Refclk Rx for > 1.5MHz jitter components has been applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 430 and select **Low Frequency 10 kHz to 1.5 MHz RMS Jitter (Data Clk).**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
3. Fits and displays all sample data on screen.
4. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200

points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

6 Stitches each acquired acquisition to make a continuous TIE data.

7 Analyzes the stitched TIE data using a MATLAB (PCIEMatlabFunction) function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies a band pass filter to remove components which are <=10KHz and components which are >=1.5MHz.

   c Applies the PLL filter using parameters for data clocked architecture.

   d Removes SSC components (fundamental and harmonics).

   e Converts back the frequency domain TIE data to time domains.

   f Computes the peak-peak jitters and RMS jitter.

8 Reports the peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

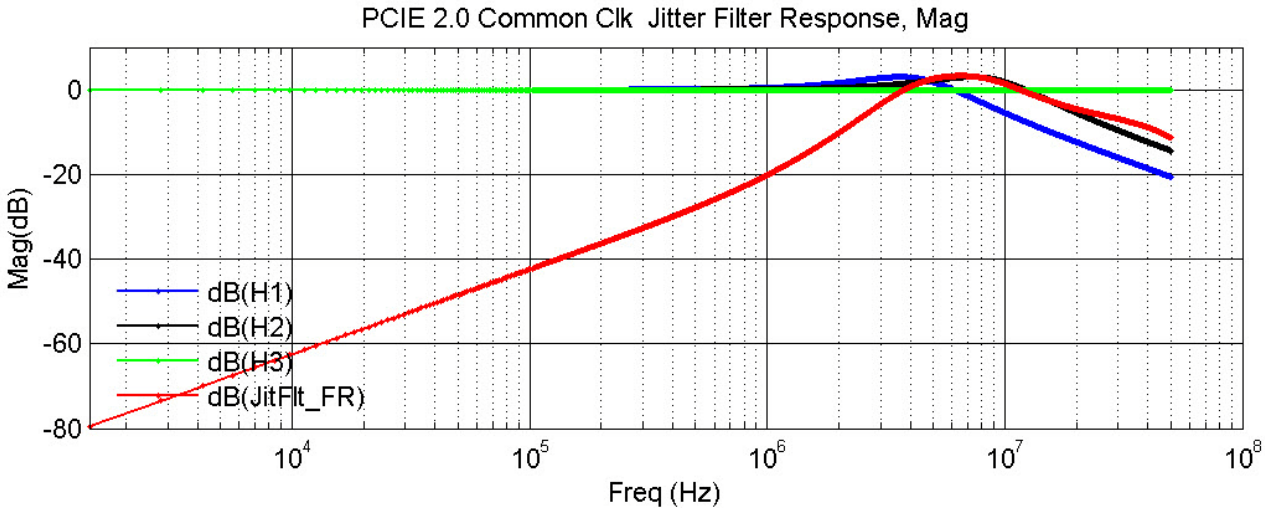


Figure 221 Data Clock Jitter Filter Response

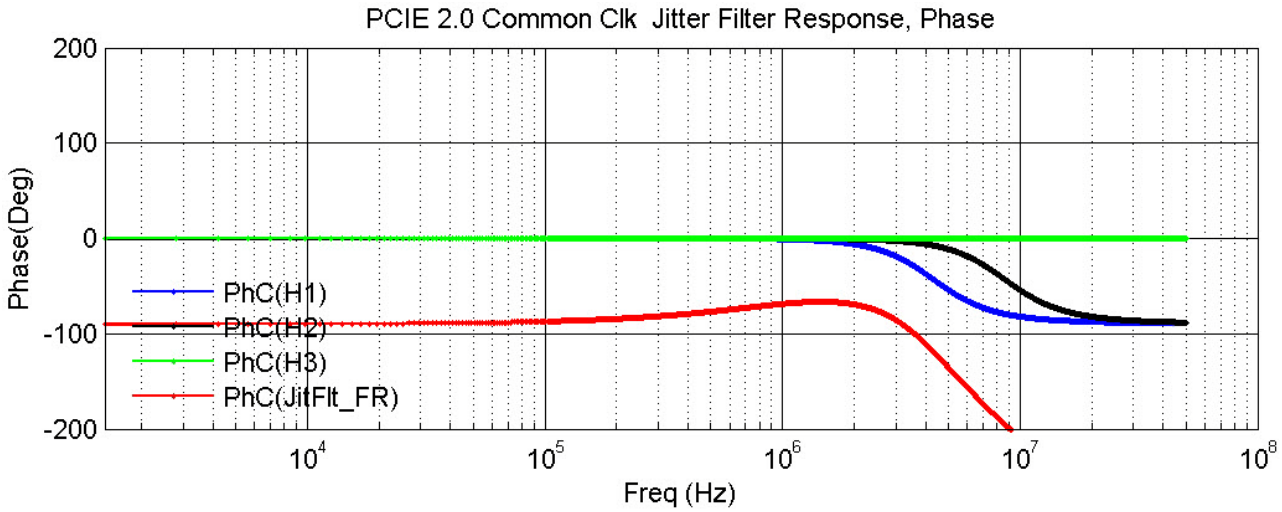


Figure 222 Data Clock Jitter Filter Response

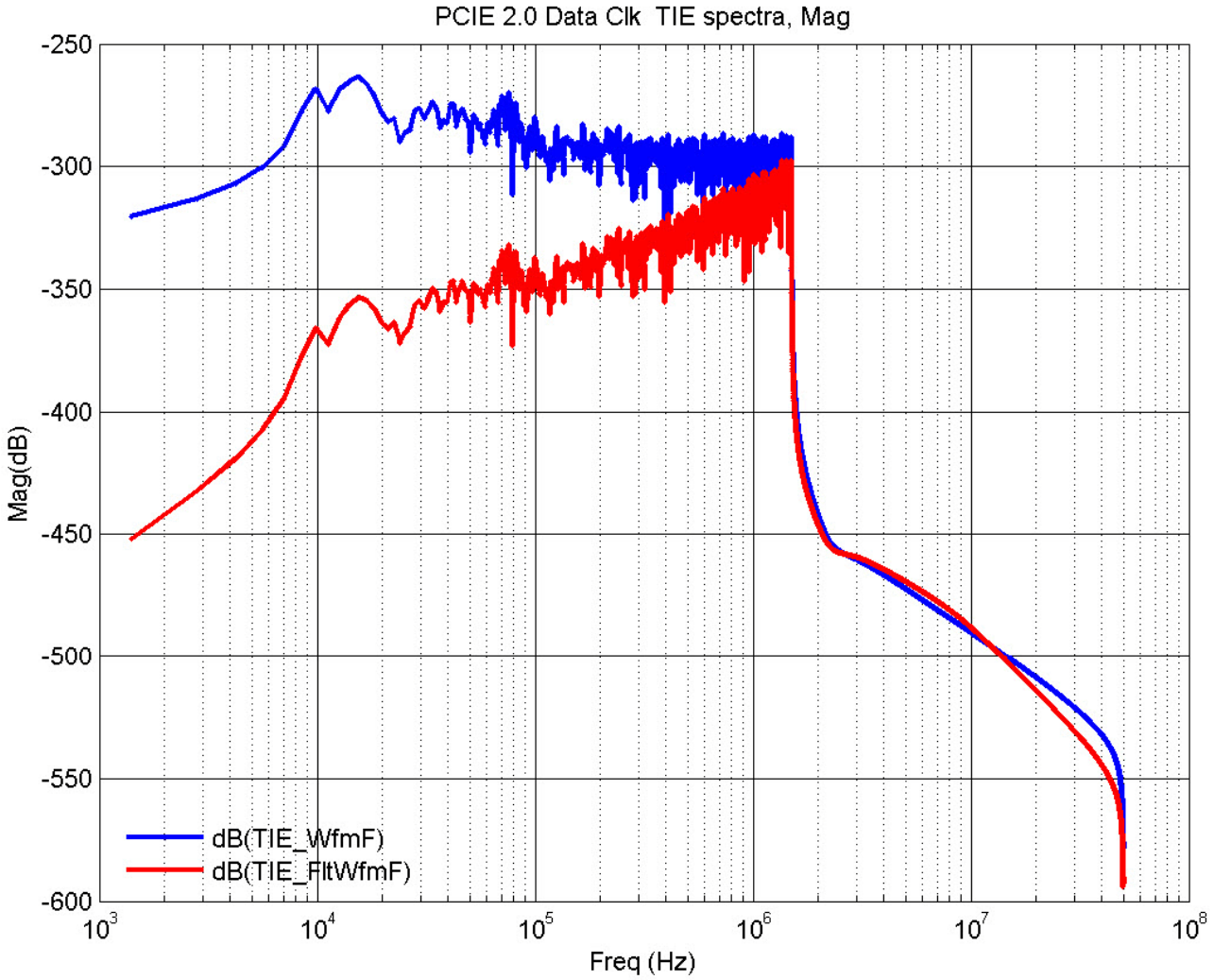


Figure 223 Data Clock TIE Spectra

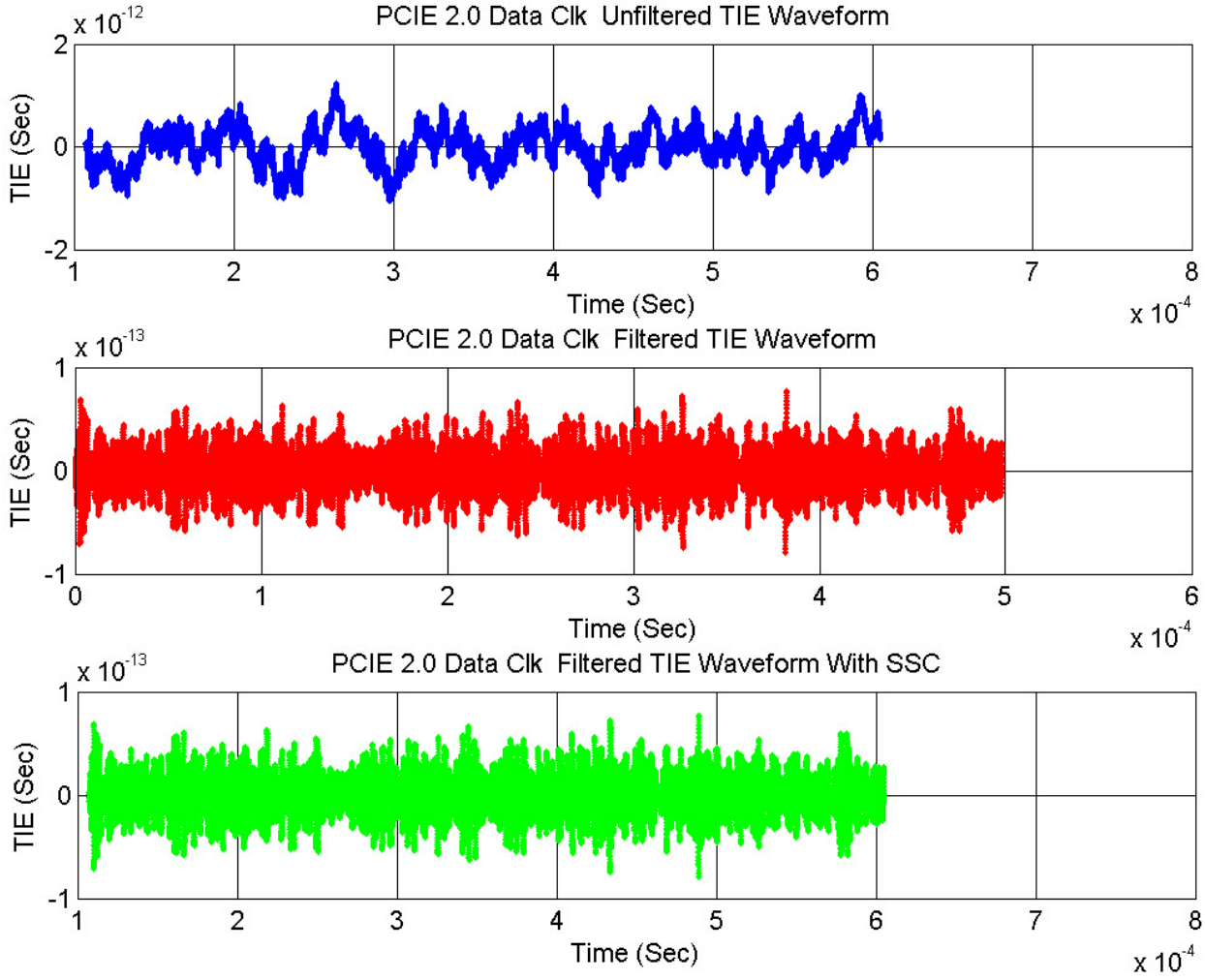


Figure 224 Data Clock TIE Waveform

SSC Deviation (Data Clk) Test

This test verifies that the reference clock SSC deviation is within the conformance limits specified in Table 4-33 of the PCIE Base Specification, rev. 3.0, version 0.71.

Test Reference

PCI Express Base Specification, Rev 3.0, version 0.71, Section 4.3.12, Table 4-33 is used as reference to check the compliance of the DUT.

Table 134 SSC Deviation (Data Clk) Test Details

Symbol	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	+0.0/-0.5%

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 430 and select **SSC Deviation (Data Clk).**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
3. Fits and displays all sample data on screen.
4. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.
6. Uses markers to indicate upper and lower limit on FUNC3 (Trend data of period measurements).
7. Measures Period_max, Period_min and Period_average.
8. Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Maximum SSC Slew Rate (Data Clk) Test

This test verifies that the reference clock SSC deviation is within the conformance limits specified in Table 4-33 of the PCIE Base Specification, rev. 3.0, version 0.71.

Test Reference

PCI Express Base Specification, Rev 3.0, version 0.71, Section 4.3.12, Table 4-33 is used as reference to check the compliance of the DUT.

Table 135 Maximum SSC Slew Rate (Data Clk) Test Details

Symbol	Description	Max
$T_{SSC-MAX-PERIOD-SLEW}$	Max SSC df/dt	0.75 ps/UI

Test Definition Notes from the Specification

Defined for a worst case SSC modulation profile such as Lexmark.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 430 and select **Maximum SSC Slew Rate (Data Clk).**

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
3. Fits and displays all sample data on screen.
4. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
5. Analyzes measurements trend using the jitter **Meas Trend** function.

6 Uses markers to indicate upper and lower limit on FUNC3 (Trend data of period measurements).

7 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:

   a Generates a differential plot (x_n - x_{n-1}).

   b The maximum slew rate corresponds to the peak of the differential plot.

8 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

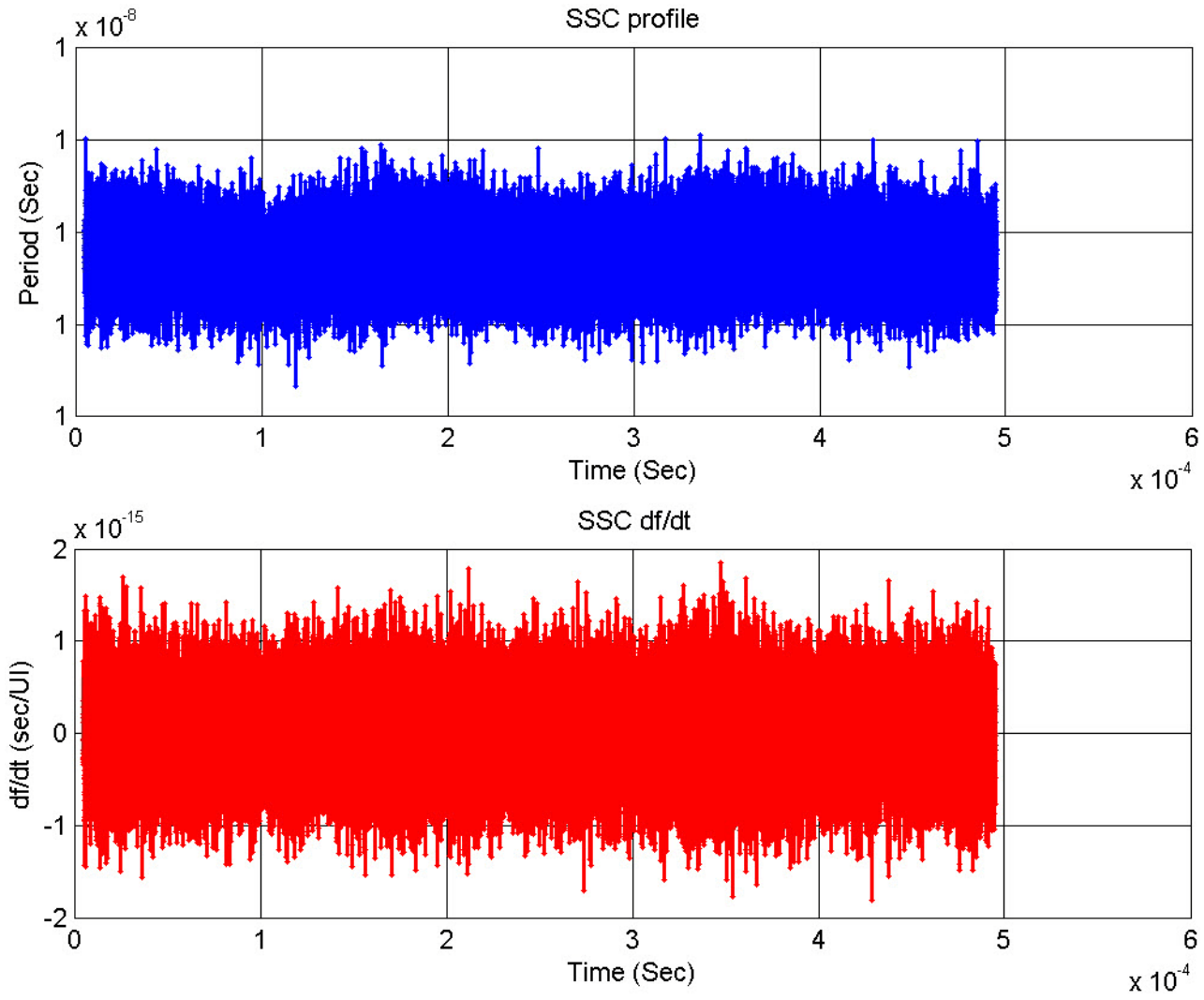


Figure 225 Maximum SSC Slew Rate

Part VI
PCI Express Version 3.0

Agilent Technologies

Part VI

24
Transmitter (Tx) Tests, PCI-E 3.0

This section provides the Methods of Implementation (MOIs) for Transmitter (Tx) tests of PCI-E 3.0 using an Agilent 90000X series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Tx Compliance

Transmitter tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the transmitter link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the Ch1 and Ch3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use two differential probe heads with two 1169A probe amplifiers (with the negative lead grounded for single-ended measurements) and the Ch1 and Ch3 inputs of an oscilloscope that has 40 GS/s sample rate available on two channels.
- Use one differential probe head with the 1169A probe amplifier and the Ch2 input of an oscilloscope that has 40 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Base Specification) will be transmitted.

Table 136 Probing Options for Transmitter Testing

	Probing Configurations			Captured Waveforms		System Specifications	
						90000X	
	Probing Method	Break Serial Link	Channels Used	Differential Mode	Common Mode	System Band Width	Rise* Time (20-80)
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	12 GHz	70 ps
	Single-Ended (2 x 1169A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	12 GHz	70 ps
	Differential (1 x 1169A w/ Differential Probe Head)	Y/N	1	True	No	12 GHz	70 ps

*Typical

Single-Ended SMA Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1 – Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1 + Ch3)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel de-skew is required using this technique because two channels are used.

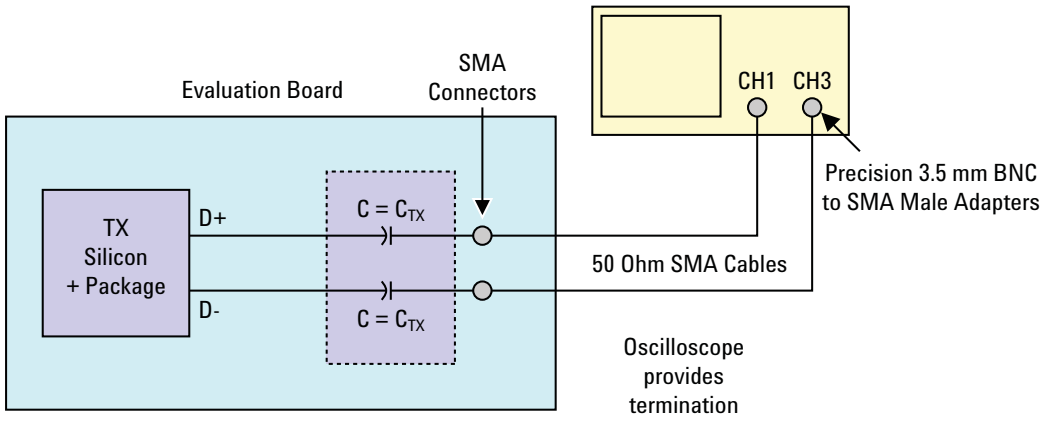


Figure 226 Single-Ended SMA Probing

Single-Ended Probing (Ch1) and (Ch3)

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Ch1 – Ch3. The Common mode measurements are also available in this configuration from the common mode waveform (Ch1 + Ch3)/2.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel de-skew is required using this technique because two channels are used.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

Place single-ended grounds as close to the signal line’s reference ground as possible.

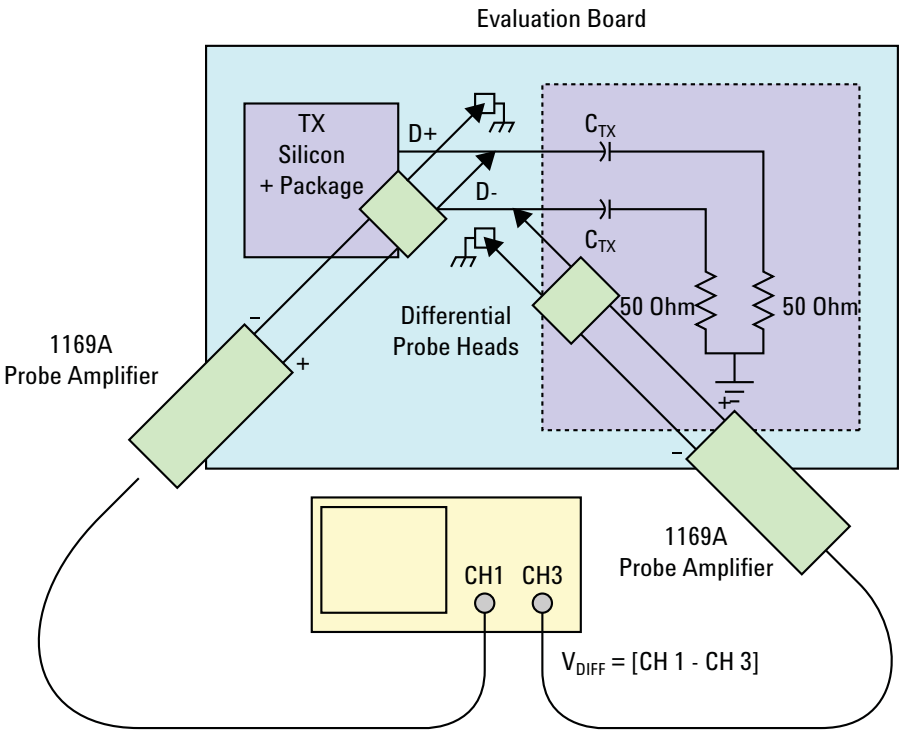


Figure 227 Single-Ended Probing

Differential Probing (Ch2)

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the transmitter, as close as possible to the transmitter.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

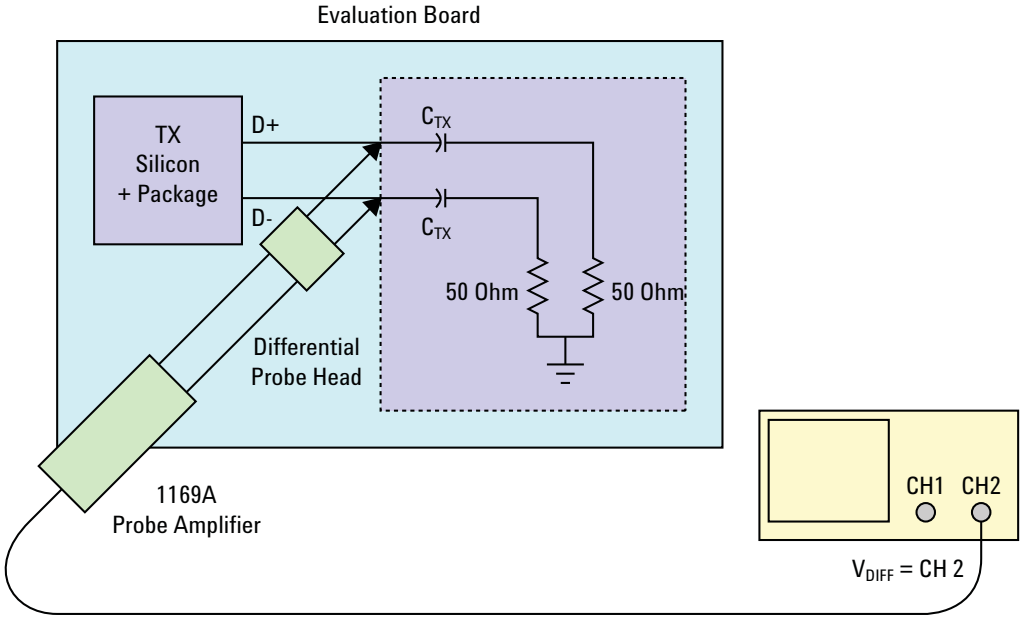


Figure 228 Differential Probing

Tx Compliance Test Load

The compliance test load for driver compliance is shown in Figure 4-25 (Base Specification).

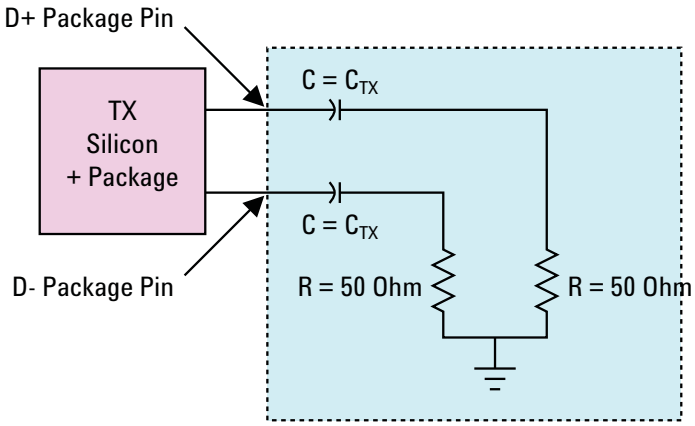


Figure 229 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to “Transmitter (Tx) Tests” in the “PCIE 3.0 Tests” group.

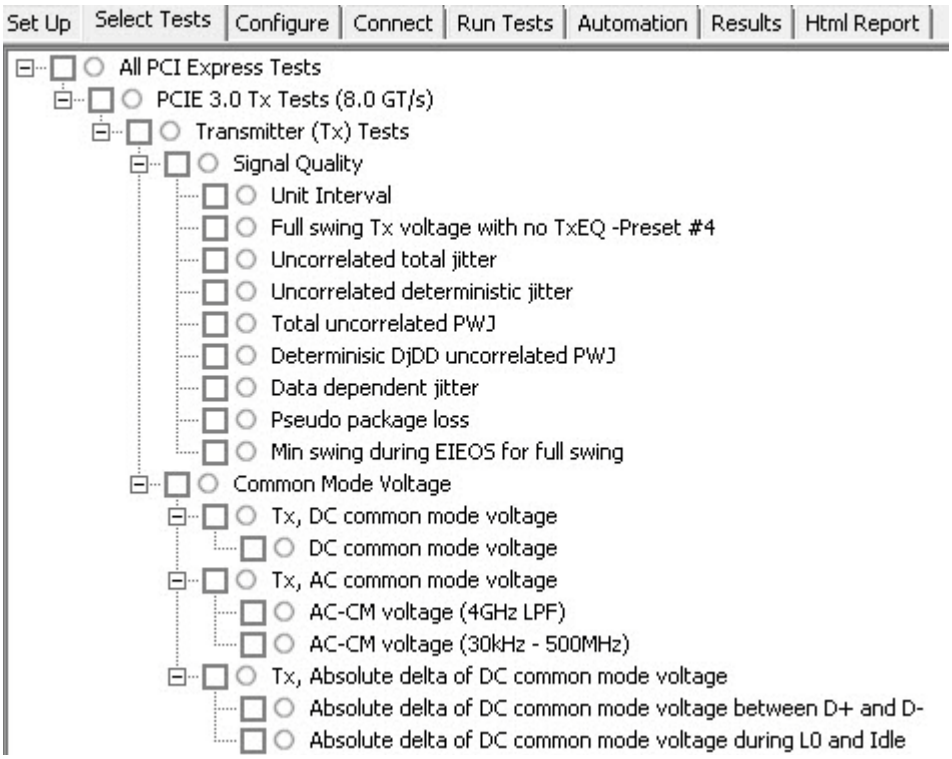


Figure 230 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13, Table 4-18 is used as reference to check the compliance of the DUT.

Table 137 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	124.9625 ps	125.0375 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Unit Interval**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.

4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 3.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

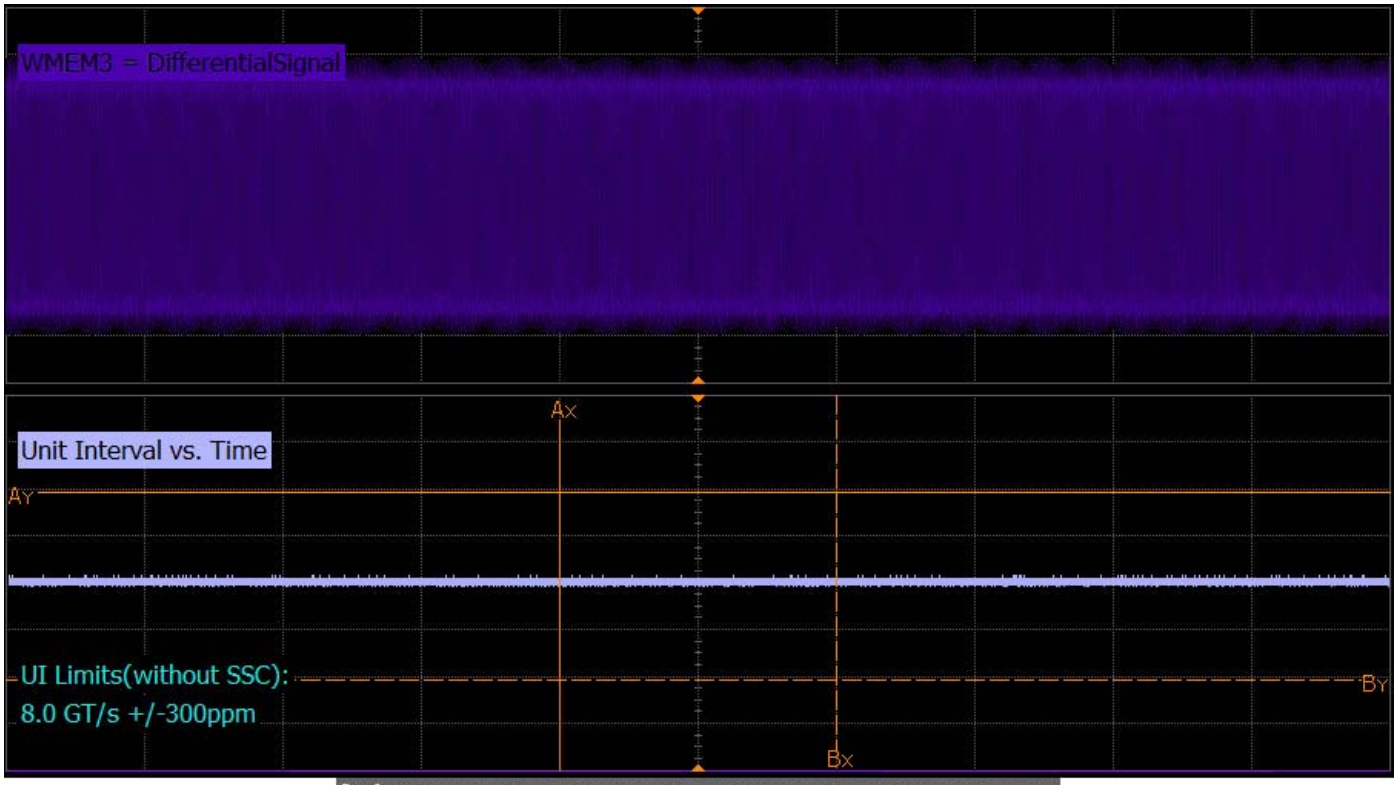


Figure 231 Reference Image for Unit Interval Test

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in Table 4-19 of the PCIE Base Specification, rev. 3.0.

The range for a transmitter's output voltage swing, (specified by V_d) with no equalization is defined by $V_{TH\text{-}FS\text{-}NO\text{-}EQ}$, and is obtained by setting c-1 and c+1 to zero and measuring the PP voltage on the 64-ones/64-zeros segment of the compliance pattern. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to last few UI of each half cycle (UI 57-62 of 64-ones/64-zeros). High frequency noise is mitigated by averaging over multiple reading until the PP noise over the area of interest is less than 2% of the magnitude of $V_{TH\text{-}FS\text{-}NO\text{-}EQ}$.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-19 is used as reference to check the compliance of the DUT.

Table 138 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}FS\text{-}NO\text{-}EQ}$	Full swing Tx voltage with no TxEQ	1300 mVPP	800 mVPP

Test Definition Notes from the Specification

Voltage measurements for $V_{TX\text{-}FS\text{-}NO\text{-}EQ}$ and $V_{TX\text{-}RS\text{-}NO\text{-}EQ}$ are made using the 64-zeros/64-ones pattern in the compliance pattern.

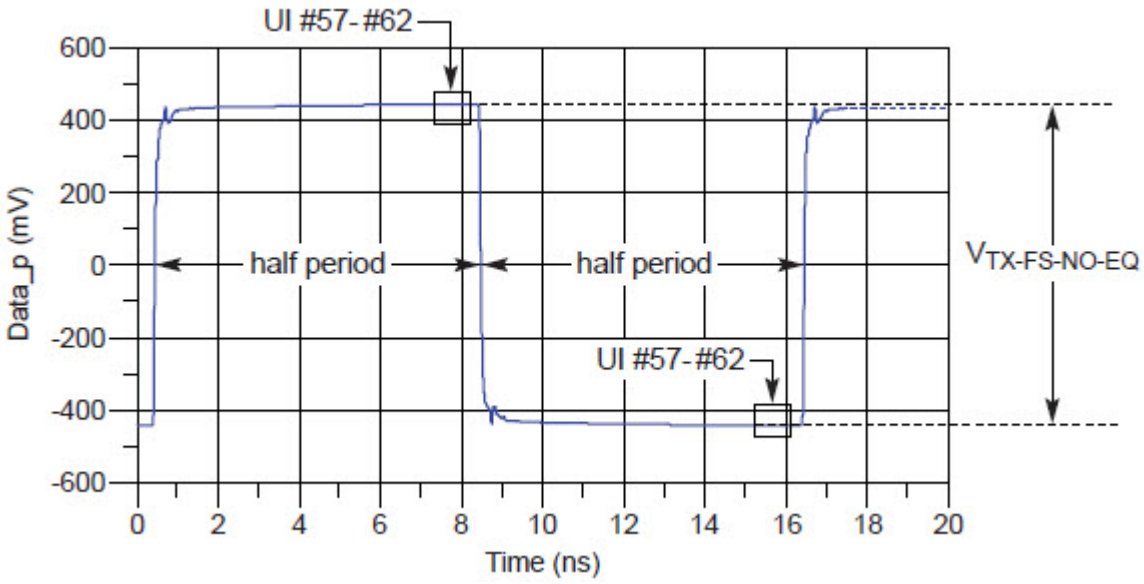


Figure 232 $V_{TX\text{-}FS\text{-}NO\text{-}EQ}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Full Swing Tx Voltage with no TxEQ -Preset #4**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Sets up grid display settings on the scope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses MATLAB function to generate the clock recovery for 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:

   a Searches the pattern for 64-ones/64-zeros segment of the compliance pattern.

   b Generates an impulse signal for each segment of signal that meet the pattern.

4 Sets up for the real time eye and fold the signal using MATLAB generated function as the clock recovery.

5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeros segment of the compliance pattern using histogram.

6 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

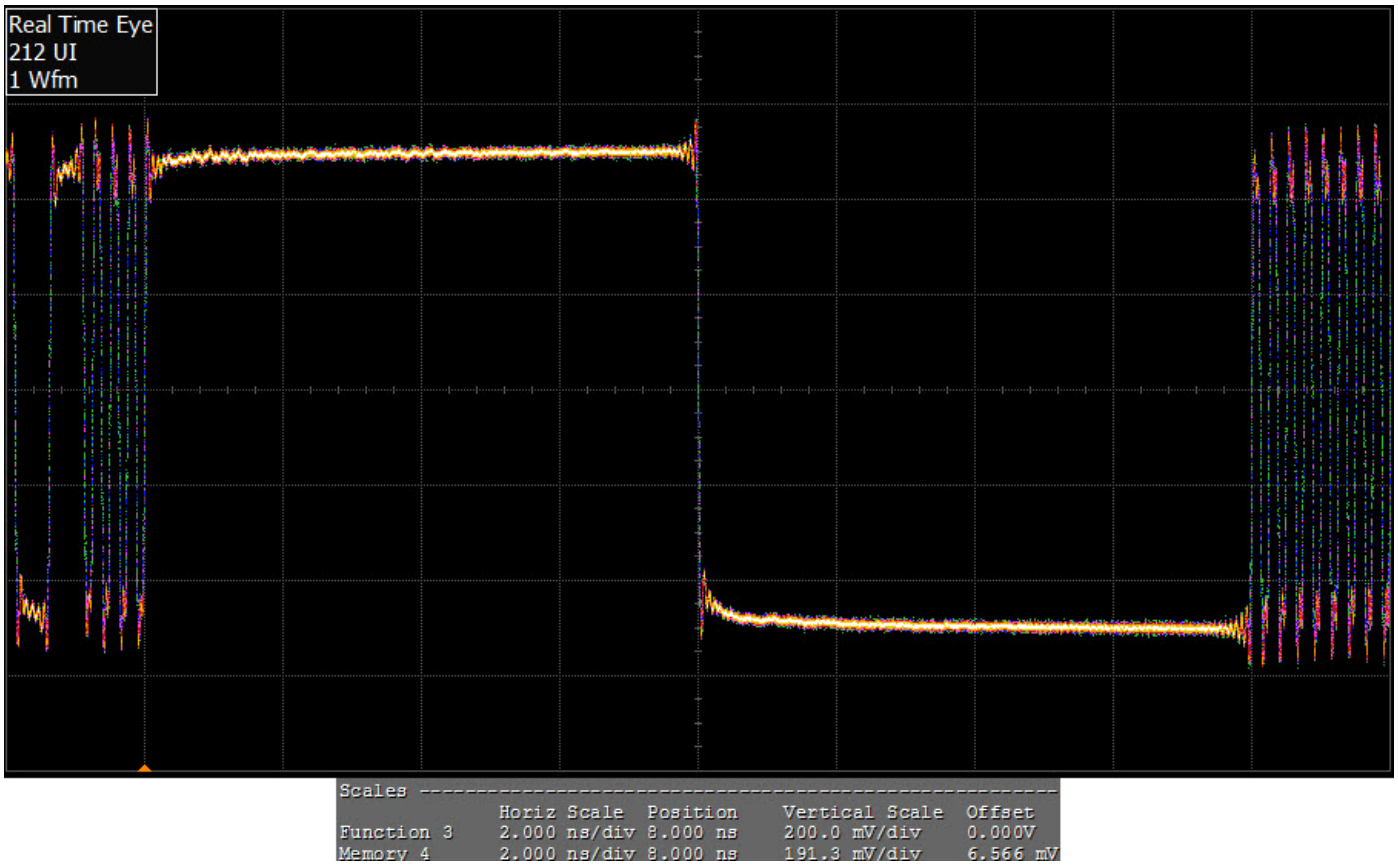


Figure 233 Reference Image for Full Swing T_x Voltage Test

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced swing signaling is within the conformance limits specified in Table 4-19 of the PCIE Base Specification, rev. 3.0, version.

The range for a transmitter's output voltage swing, (specified by V_d) with no equalization is defined by $V_{TH\text{-}RS\text{-}NO\text{-}EQ}$, and is obtained by setting c-1 and c+1 to zero and measuring the PP voltage on the 64-ones/64-zeros segment of the compliance pattern. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to last few UI of each half cycle (UI 57-62 of 64-ones/64-zeros). High frequency noise is mitigated by averaging over multiple reading until the PP noise over the area of interest is less than 2% of the magnitude of $V_{TH\text{-}RS\text{-}NO\text{-}EQ}$.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-19 is used as reference to check the compliance of the DUT.

Table 139 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min
$V_{TX-FS-NO-EQ}$	Full swing Tx voltage with no TxEQ	1300 mVPP

Test Definition Notes from the Specification

Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeros/64-ones pattern in the compliance pattern.

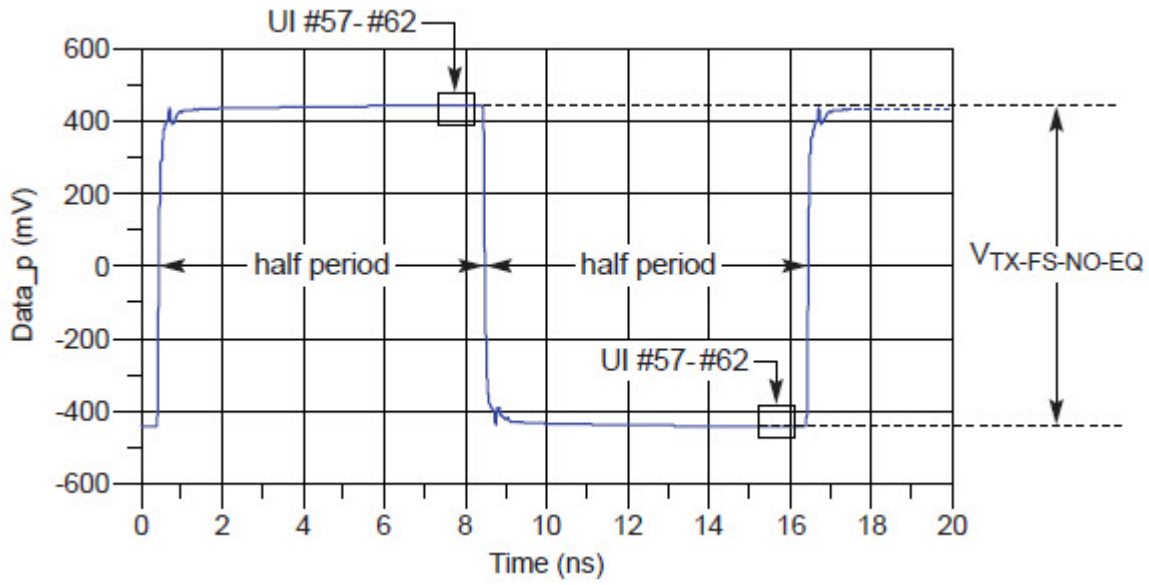


Figure 234 $V_{TX-FS-NO-EQ}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Reduced Swing Tx Voltage with no TxEQ -Preset #4**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Sets up grid display settings on the scope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses MATLAB function to generate the clock recovery for 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:

   a Searches the pattern for 64-ones/64-zeros segment of the compliance pattern.

   b Generates an impulse signal for each segment of signal that meet the pattern.

4 Sets up for the real time eye and fold the signal using MATLAB generated function as the clock recovery.

5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeros segment of the compliance pattern using histogram.

6 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

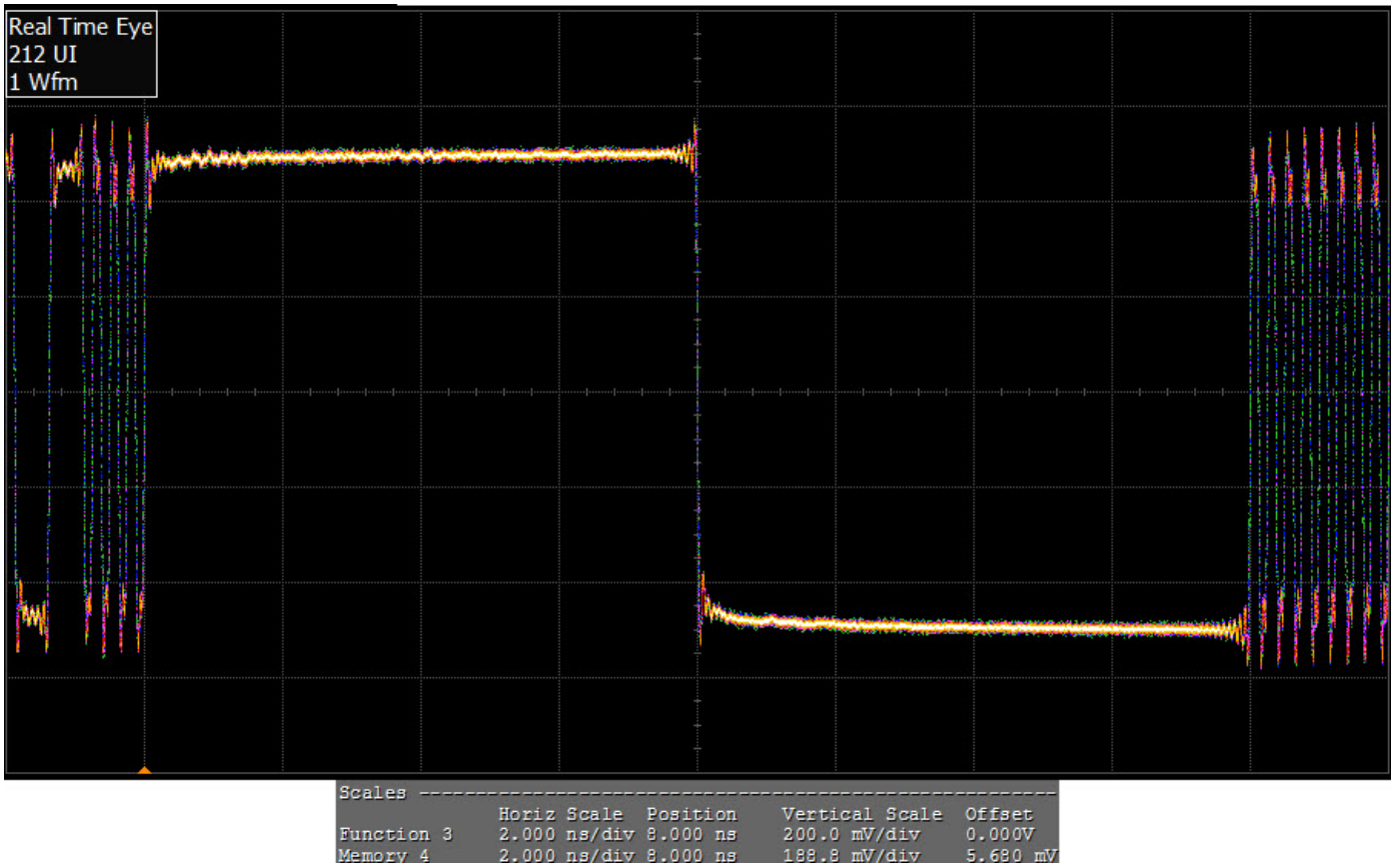


Figure 235 Reference Image for Reduced Swing T_x Voltage Test

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX\text{-}EIEOS\text{-}FS}$ is within the allowed range.

$V_{TX\text{-}EIEOS\text{-}FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of eight consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX\text{-}EIEOS\text{-}FS}$ for full swing signaling and by $V_{TX\text{-}EIEOS\text{-}RS}$ for reduced swing signaling. $V_{TX\text{-}EIEOS\text{-}RS}$ is smaller than

$V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a c+1 coefficient value of -0.33 and a c-1 coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 4-19. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with a c+1 coefficient value of -0.167 and a c-1 coefficient of 0.00, corresponding to preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-19 is used as reference to check the compliance of the DUT.

Table 140 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250 mVPP

Test Definition Notes from the Specification

Voltage limits comprehend both full swing and reduced swing modes. The Tx must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the Tx can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mVPP at the Rx pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel. The transmitter must advertise a value for LF during TS1 at 8.0 GT/s that ensures these parameters are met.

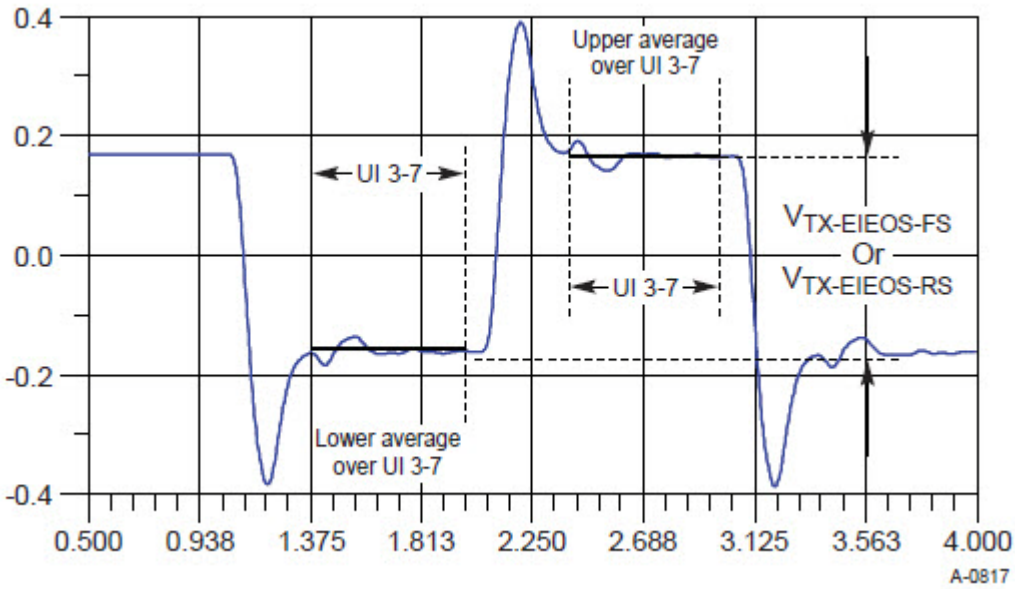


Figure 236 Measurement $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Min Swing During EIEOS for Full Swing**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTestWrapper.dll file.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTestWrapper.dll file.

   d Gets compliance test results from SigTestWrapper.dll file.

   e Finds and updates the worst case test result values.

   f Gets the average EIEOS high voltage.

   g Gets the average EIEOS low voltage.

   h Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX\text{-}EIEOS\text{-}RS}$ is within the allowed range.

$V_{TX\text{-}EIEOS\text{-}FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of eight consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be

taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a c+1 coefficient value of -0.33 and a c-1 coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 4-19. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with a c+1 coefficient value of -0.167 and a c-1 coefficient of 0.00, corresponding to preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-19 is used as reference to check the compliance of the DUT.

Table 141 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	232 mVPP

Test Definition Notes from the Specification

Voltage limits comprehend both full swing and reduced swing modes. The Tx must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the Tx can drive. The $V_{TX-EIEOS-FS}$

and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mVPP at the Rx pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel. The transmitter must advertise a value for LF during TS1 at 8.0 GT/s that ensures these parameters are met.

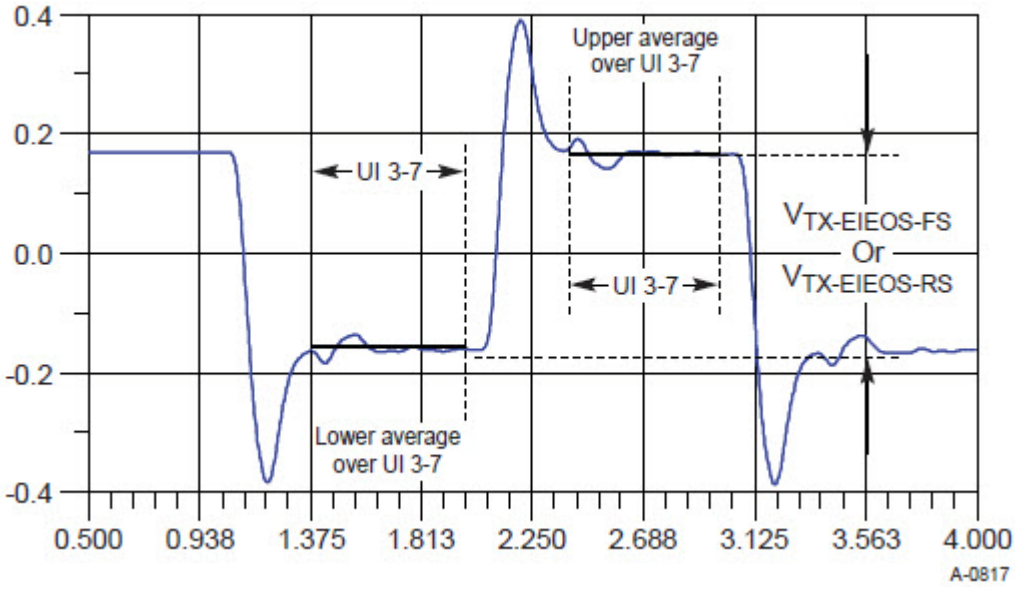


Figure 237 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Min Swing During EIEOS for Reduced Swing**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTestWrapper.dll file.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTestWrapper.dll file.

   d Gets compliance test results from SigTestWrapper.dll file.

   e Finds and updates the worst case test result values.

   f Gets the average EIEOS high voltage.

   g Gets the average EIEOS low voltage.

   h Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter $T_{TX\text{-}UTJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-19 is used as reference to check the compliance of the DUT.

Table 142 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	31.25 ps PP at 10^{-12}

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Uncorrelated total jitter**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTestWrapper.dll file.
   a. Gets input test waveform data from scope.
   b. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
   c. Performs the transmitter compliance test function using the SigTestWrapper.dll file.
   d. Gets compliance test results from SigTestWrapper.dll file.
   e. Reports the RJ RMS jitter value.
   f. Reports the peak total jitter value.
3. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-19 is used as reference to check the compliance of the DUT.

Table 143 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	12 ps PP

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Uncorrelated deterministic jitter**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTestWrapper.dll file.
   a. Gets input test waveform data from scope.
   b. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
   c. Performs the transmitter compliance test function using the SigTestWrapper.dll file.
   d. Gets compliance test results from SigTestWrapper.dll file.
   e. Reports the peak uncorrelated deterministic jitter value.
3. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX\text{-}UPW\text{-}TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-19 is used as reference to check the compliance of the DUT.

Table 144 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX\text{-}UPW\text{-}TJ}$	Total uncorrelated PWJ	24 ps PP at 10^{-12}

Test Definition Notes from the Specification

PWJ parameters are measured after DDJ separation.

Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Total Uncorrelated PWJ**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTestWrapper.dll file.
   a. Gets input test waveform data from scope.
   b. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
   c. Performs the transmitter compliance test function using the SigTestWrapper.dll file.
   d. Gets compliance test results from SigTestWrapper.dll file.
   e. Reports the random jitter value.
   f. Reports the uncorrelated total pulse width jitter value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX\text{-}UPW\text{-}DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-19 is used as reference to check the compliance of the DUT.

Table 145 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX\text{-}UPW\text{-}DJDD}$	Deterministic DjDD uncorrelated PWJ	10 ps PP

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Deterministic DjDD uncorrelated PWJ**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTestWrapper.dll file.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTestWrapper.dll file.

   d Gets compliance test results from SigTestWrapper.dll file.

   e Reports the peak deterministic DjDD uncorrelated PWJ value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter

This test verifies that the maximum data dependent jitter, $T_{TX\text{-}DDJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-19 is used as reference to check the compliance of the DUT.

Table 146 Data Dependent Jitter Test Details

Symbol	Parameter	Max
$T_{TX\text{-}DDJ}$	Data dependent jitter	18 ps PP

Test Definition Notes from the Specification

- Measured with optimized preset value after de-embedding to Tx pin.
- The 18 ps number takes into account measurement error.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Data dependent jitter**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTestWrapper.dll file.
   a. Gets input test waveform data from scope.
   b. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
   c. Performs the transmitter compliance test function using the SigTestWrapper.dll file.
   d. Gets compliance test results from SigTestWrapper.dll file.
   e. Reports the data dependent value.
3. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss

This test verifies that the maximum pseudo package loss, ps21TX is within the allowed range.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V111) against a 1010 pattern (V101). Tx package loss measurement is made with c-1 and c+1 both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V101 and V111. Multiple measurements shall be made and averaged to obtain stable values for V101 and V111. Due to the HF content of V101, ps21 TX measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V101 and V111 is made towards the end of each interval to minimize ISI and low frequency effects. V101 is defined as the peak-peak voltage between minima and maxima of the clock pattern. V111 is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-19 is used as reference to check the compliance of the DUT.

Table 147 Pseudo Package Loss Test Details

Symbol	Parameter	Min
$ps21_{TX}$	Pseudo package loss	–3.0 dB

Test Definition Notes from the Specification

- PP ratio of 64-ones/64-zeroes pattern versus 0101 pattern. No Tx equalization.
- The –3.0 dB number takes into account the measurement error. For some Tx package/driver combinations, $ps21_{TX}$ may be greater than 0 dB.

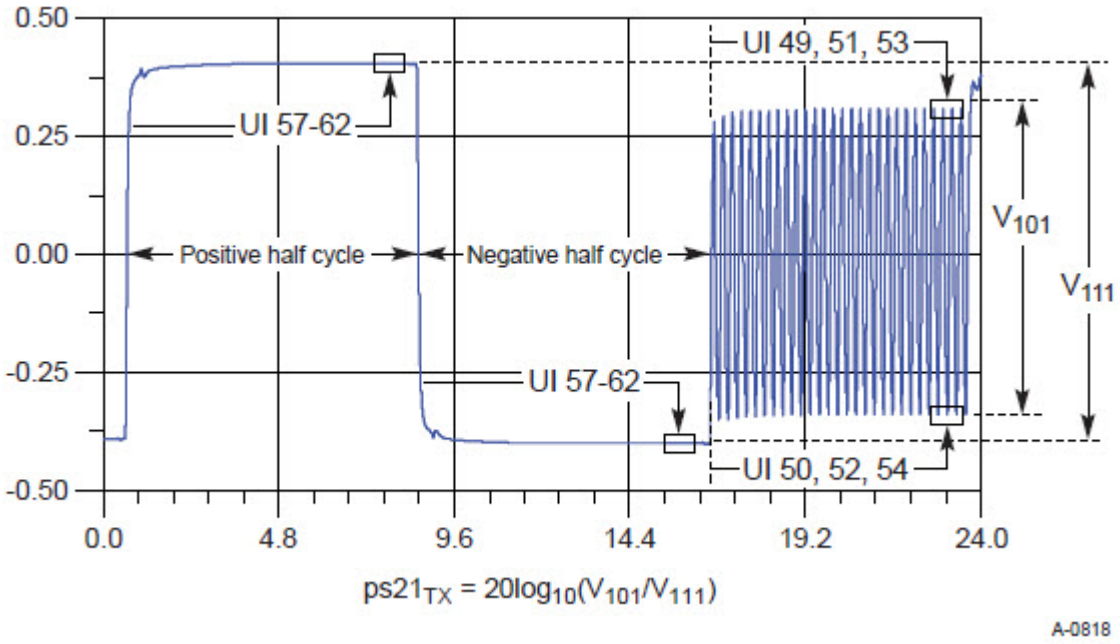


Figure 238 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Pseudo package loss.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs actual compliance testing using the SigTestWrapper.dll file.

   a Gets input test waveform data from scope.

   b Acquires scope sample waveform data (re-iterate to capture at least 1M UI).

   c Performs the transmitter compliance test function using the SigTestWrapper.dll file.

   d Gets compliance test results from SigTestWrapper.dll file.

   e Reports the number of package loss measurements taken.

   f Reports the package loss ration value.

3 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-18 is used as reference to check the compliance of the DUT.

Table 148 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- The allowed DC common mode voltage at the Transmitter pins under any conditions.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients and a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **DC common mode voltage**.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3. Sets up DC common mode voltage as follows:
   a. Enables and displays common mode measurements.
   b. Loads common mode signal to waveform memory.
   c. Loads and enhance dynamic range D+ signal and D- signal.
   d. Enables the average common mode measurement.
   e. Uses markers to indicate compliance test limit boundaries (0V to 3.6V).
4. Measures the average value of D+ and D- signal.
5. Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

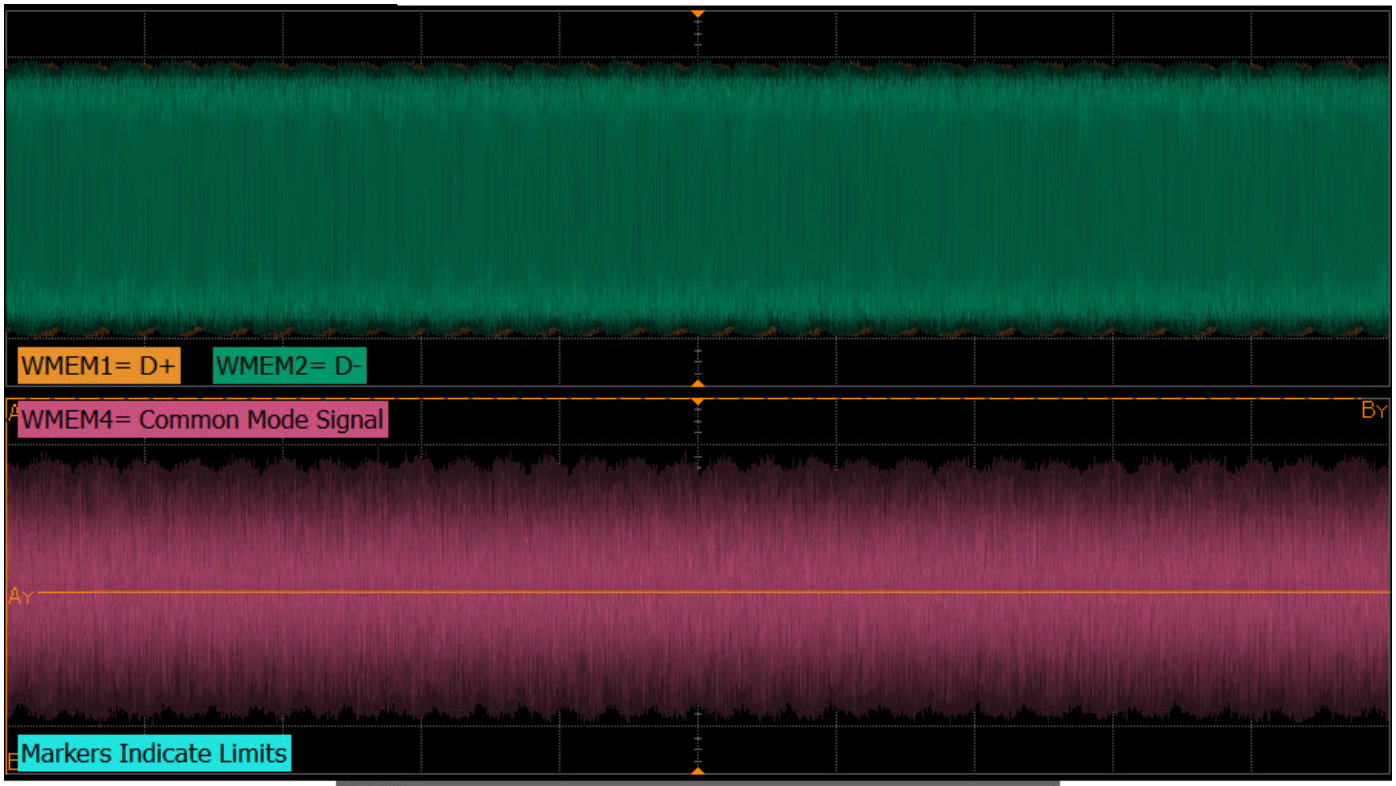


Figure 239 Reference Image for DC Common Mode Voltage Test

AC Common-Mode Voltage (4 GHz LPF) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-18 is used as reference to check the compliance of the DUT.

Table 149 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- At 8.0 GT/s, no more than 50 mVPP within 0.03 to 500 MHz range. At 5.0 GT/s, no more than 100 mVPP within 0.03 to 500 MHz range.
- $V_{TX-AC-CM-PP}$ and $V_{TX-AC-CM-P}$ are defined in Section 4.3.3.2. Measurement is made over at least 10^6 UIs.
- Tx common-mode noise for 8.0 GT/s is measured at TP1 without de-embedding the breakout channel. The parameter captures device common-mode noise only and is not intended to capture system common-mode noise. For 5.0 GT/s, an LPF with a –3 dB corner at 2.5 GHz is applied to the raw data. For 8.0 GT/s, the filter's –3 dB corner is at 4.0 GHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **AC-CM voltage (4GHz LPF)**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 4GHz to the common mode signal.

4 Measures the VPP of the filtered signal.

5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

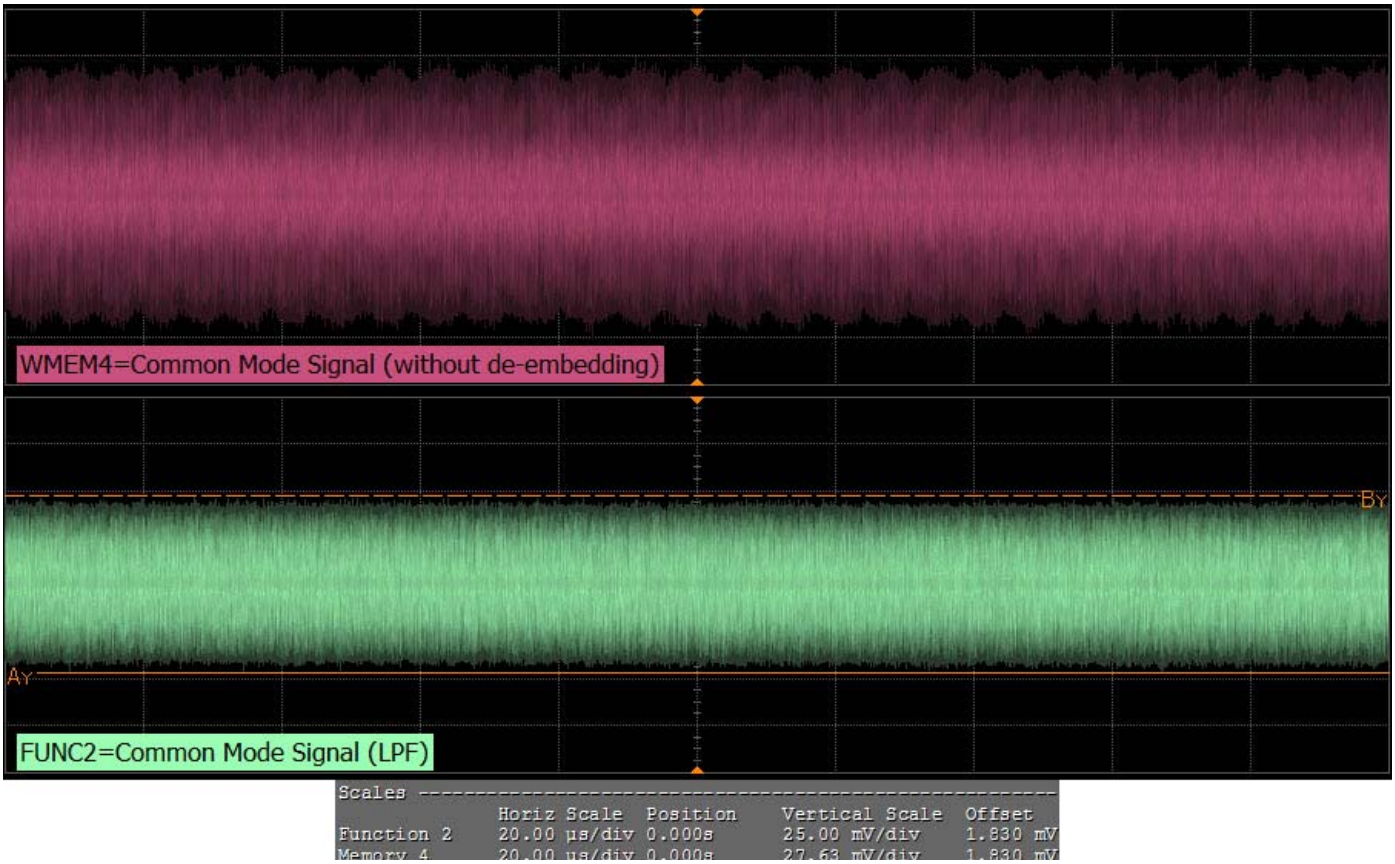


Figure 240 Reference Image for AC-CM voltage (4GHz LPF) Test

AC Common Mode Voltage (30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}CM\text{-}AC\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-18 is used as reference to check the compliance of the DUT.

Table 150 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX\text{-}CM\text{-}AC\text{-}PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- At 8.0 GT/s, no more than 50 mVPP within 0.03 to 500 MHz range. At 5.0 GT/s, no more than 100 mVPP within 0.03 to 500 MHz range.
- $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ and $V_{TX\text{-}AC\text{-}CM\text{-}P}$ are defined in Section 4.3.3.2. Measurement is made over at least 10^6 UIs.
- Tx common-mode noise for 8.0 GT/s is measured at TP1 without de-embedding the breakout channel. The parameter captures device common-mode noise only and is not intended to capture system common-mode noise. For 5.0 GT/s, an LPF with a –3 dB corner at 2.5 GHz is applied to the raw data. For 8.0 GT/s, the filter's –3 dB corner is at 4.0 GHz.

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **AC-CM voltage (30KHz - 500 MHz)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (40GHz LPF) test.

1 Gets PCIE3 compliance signal.

2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30KHz and 500 MHz.

3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

4 Measures the VPP of the filtered signal.

5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

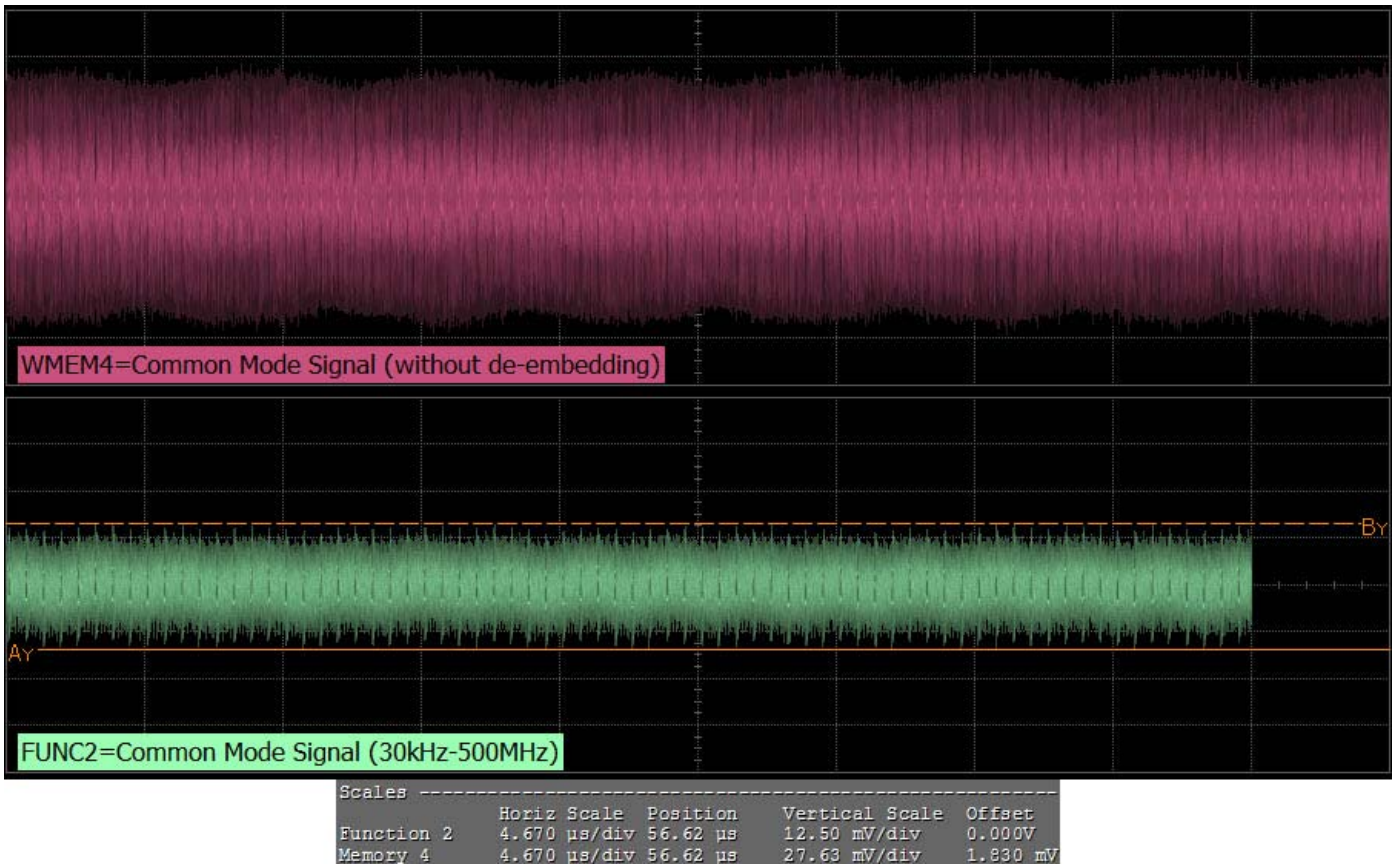


Figure 241 Reference Image for AC-CM voltage (30KHz - 500MHz) Test

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$$|V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D-[during\ L0]}| \leq 25\ mV$$

$V_{TX\text{-}CM\text{-}DC\text{-}D+}$ = $DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-}$ = $DC_{(avg)}$ of $|V_{TX\text{-}D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-18 is used as reference to check the compliance of the DUT.

Table 151 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Absolute delta of DC common mode voltage between D+ and D-**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-

2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.

3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$$

$$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}\ of\ |V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$$

$$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}\ of\ |V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2\ [electrical\ idle]$$

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13.1, Table 4-18 is used as reference to check the compliance of the DUT.

Table 152 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Absolute delta of DC common mode voltage during L0 and Idle**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.

2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.

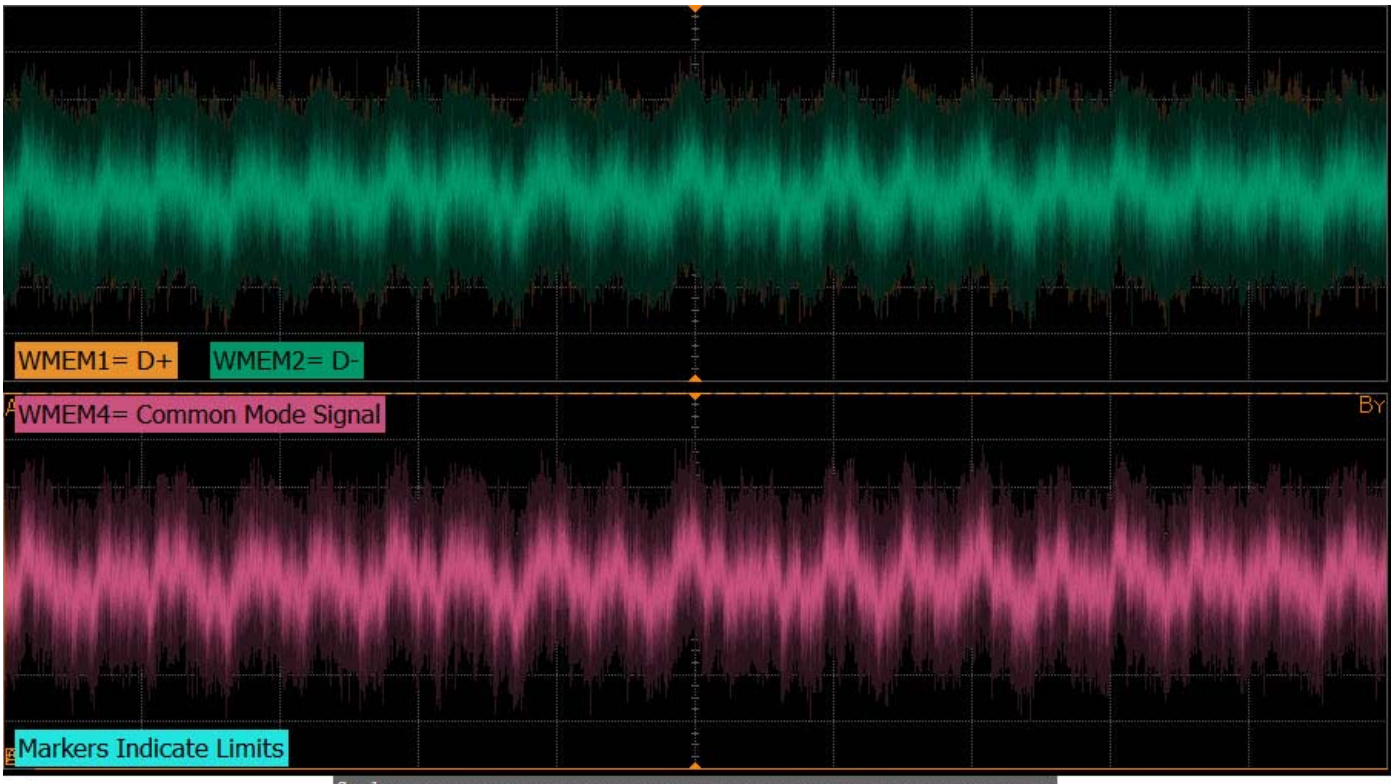
- Average DC value of the common-mode signal

3 Computes the differential between the DC of the active stage and the idle stage.

4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	20.00 µs/div	0.000s	787.5 µV/div	2.755 mV
Memory 2	20.00 µs/div	0.000s	762.5 µV/div	8.203 mV
Memory 4	20.00 µs/div	0.000s	582.5 µV/div	5.479 mV

Markers

	Source	X Position	Y Position
A	Memory 4	-1.00000000000000s	0.000000V
B	Memory 4	-1.00000000000000s	3.600000V

Figure 242 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

Running Equalization Presets Tests

Start the automated testing application as described in “Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to “Equalization Presets Tests” in the “PCIE 3.0 Tests” group.

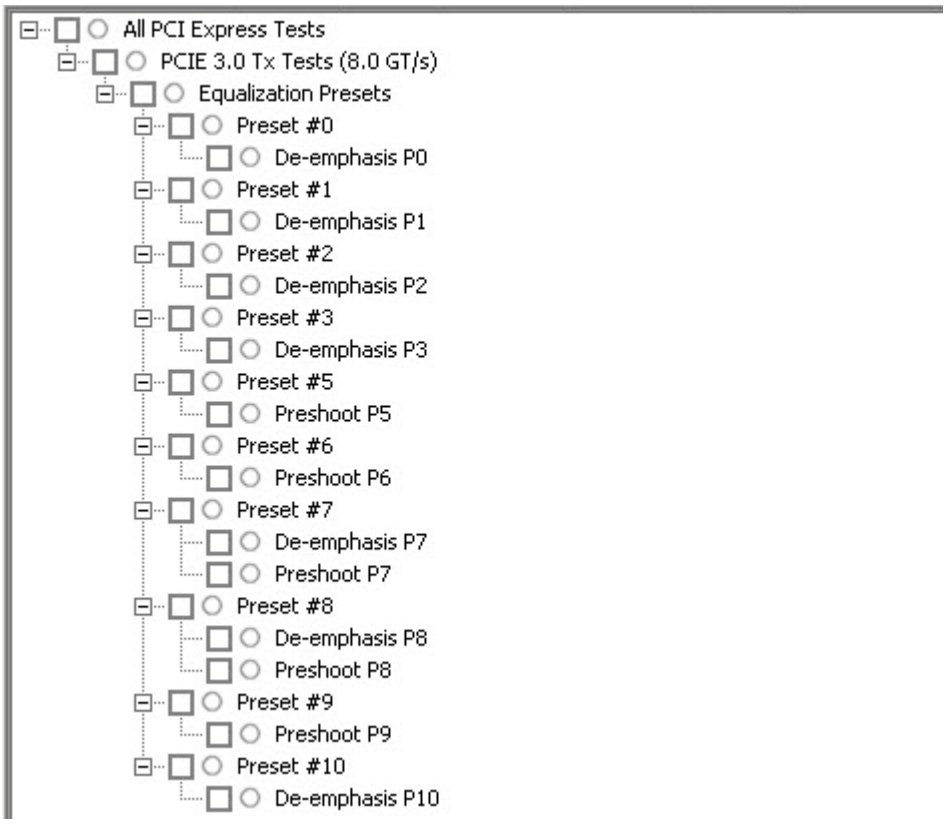


Figure 243 Selecting Equalization Presets Tests

Preset #1 Measurement (P1), De-emphasis Test

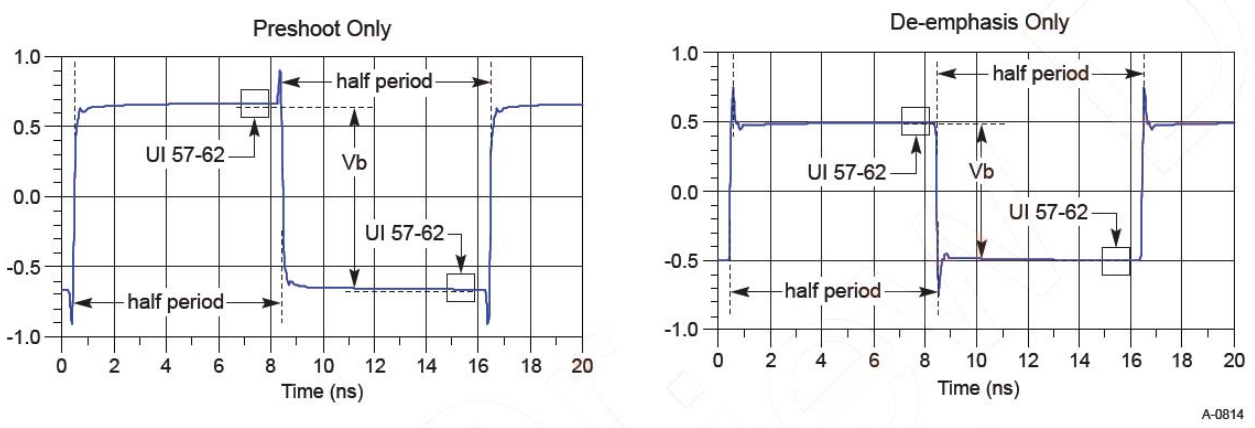
This test verifies that the de-emphasis of the preset number P1 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 153 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P1	P1/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 154 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P1	0.0	–3.5 ± 1 dB	0.000	–0.167	1.000	0.668	0.668

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **De-emphasis P1**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s):
   - Full swing Tx voltage with no TxEQ Preset #4.
   - Obtains the measurement of Vb at preset number P4 ($V_{TH\text{-}FS\text{-}NO\text{-}EQ}$).

2 Sets up grid display settings on the oscilloscope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses the MATLAB function to generate the clock recovery for the 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:
   - Searches the pattern for the 64-ones/64-zeros segment of the compliance pattern.
   - Generates an impulse signal for each segment of the signal that meets the pattern.

4 Sets up the real time eye and fold the signal using the MATLAB generated signal as the clock recovery.

5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeros segment of the compliance pattern using the histogram.

6 Obtains the measurement of Vb at preset number P1.

7 Computes the de-emphasis at preset value P1.

8 Reports the measurement of Vb during preset values P1 and P4.

9 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #0 Measurement (P0), De-emphasis

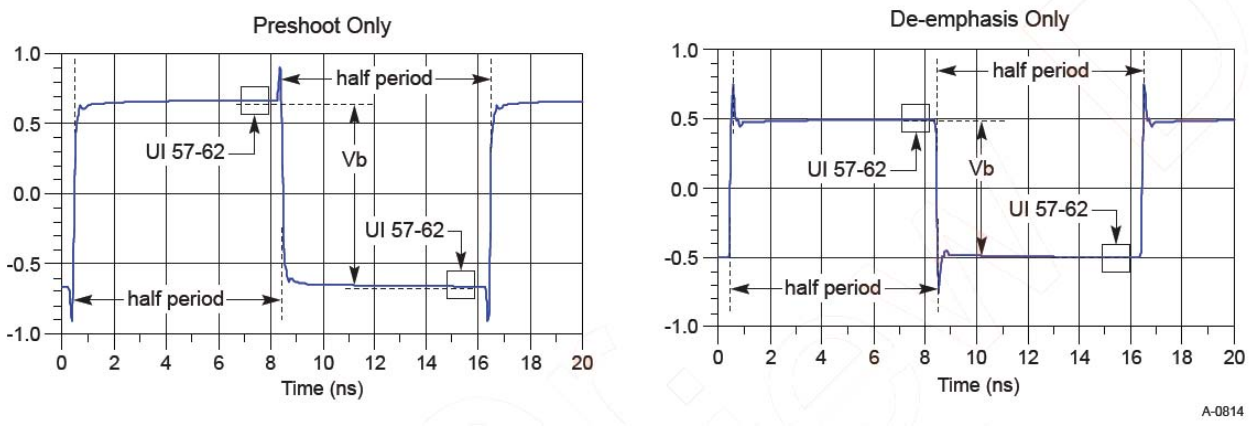
This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 155 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P0	P0/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 156 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P0	0.0	–6.0 ± 1.5 dB	0.000	–0.250	1.000	0.500	0.500

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **De-emphasis P0**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s):
   - Full swing Tx voltage with no TxEQ Preset #4.
   - Obtains the measurement of Vb at preset number P4 ($V_{TH\text{-}FS\text{-}NO\text{-}EQ}$).

2 Sets up grid display settings on the oscilloscope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses the MATLAB function to generate the clock recovery for the 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:
   - Searches the pattern for the 64-ones/64-zeros segment of the compliance pattern.
   - Generates an impulse signal for each segment of the signal that meets the pattern.

4 Sets up the real time eye and fold the signal using the MATLAB generated signal as the clock recovery.

5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeros segment of the compliance pattern using the histogram.

6 Obtains the measurement of Vb at preset number P0.

7 Computes the de-emphasis at preset value P0.

8 Reports the measurement of Vb during preset values P0 and P4.

9 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #9 Measurement (P9), Preshoot

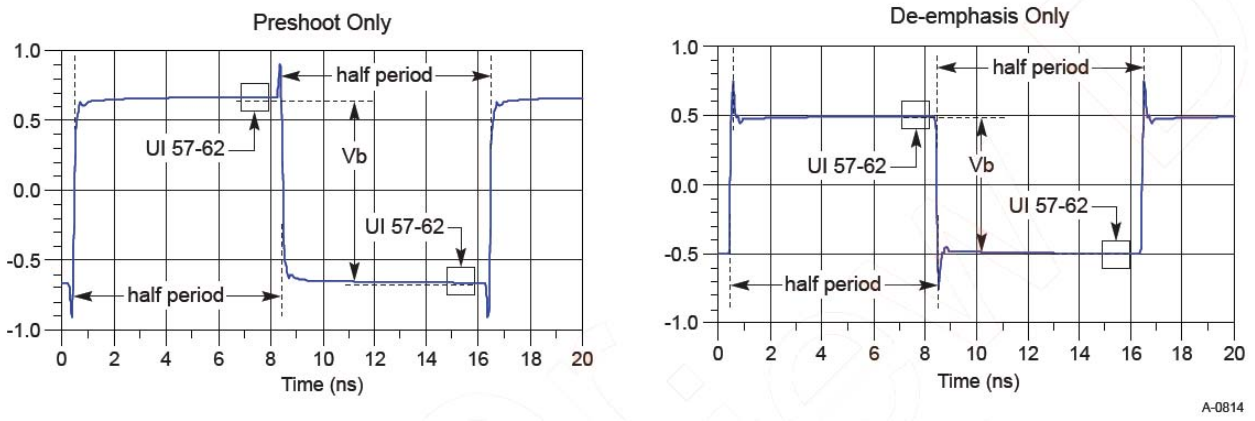
This test verifies that the preshoot of the preset number P9 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0, version 0.71.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 157 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P9	N/A	P4/P9

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 158 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P9	3.5 ± 1 dB	0.0	–0.166	0.000	0.668	0.668	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Preshoot P9**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s):

- Full swing Tx voltage with no TxEQ Preset #4.

- Obtains the measurement of Vb at preset number P4 ($V_{TH\text{-}FS\text{-}NO\text{-}EQ}$).

2 Sets up grid display settings on the oscilloscope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses the MATLAB function to generate the clock recovery for the 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:

- Searches the pattern for the 64-ones/64-zeros segment of the compliance pattern.
- Generates an impulse signal for each segment of the signal that meets the pattern.

4 Sets up the real time eye and fold the signal using the MATLAB generated signal as the clock recovery.

5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeros segment of the compliance pattern using the histogram.

6 Obtains the measurement of Vb at preset number P9.

7 Computes the preshoot at preset value P9.

8 Reports the measurement of Vb during preset values P9 and P4.

9 Compares the preshoot value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), De-emphasis

This test verifies that the de-emphasis of the preset number P8 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

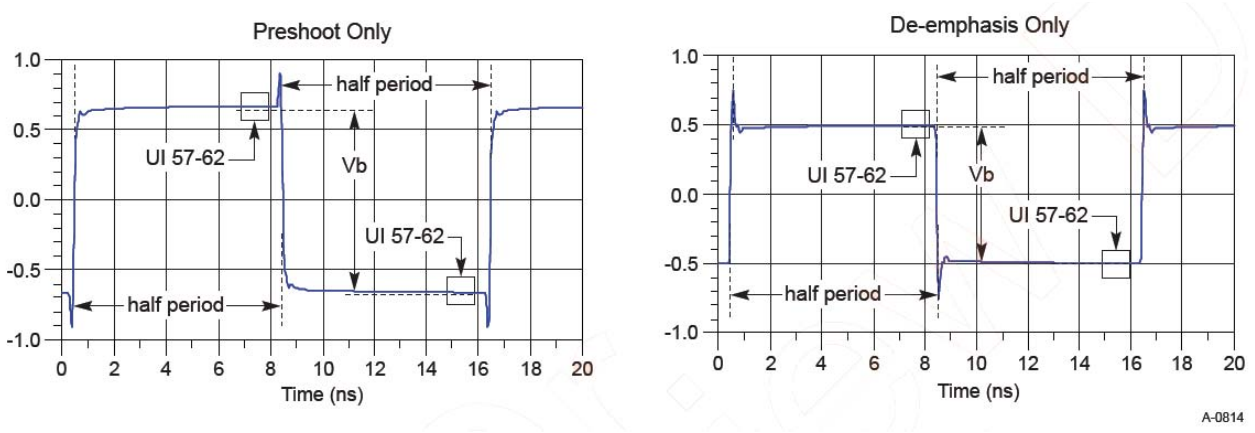
An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1}

and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 159 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 160 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 1 dB	–3.5 ± 1 dB	–0.125	–0.125	0.750	0.500	0.750

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **De-emphasis P8**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s):
   - Presets #6 measurement (P6), preshoot.
   - Obtains the measurement of Vb at preset number P6 (Vb_P6).
   - Presets #3 measurement (P3), de-emphasis.
   - Obtains the measurement of Vb at preset number P3 (Vb_P3).

2 Sets up grid display settings on the oscilloscope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses the MATLAB function to generate the clock recovery for the 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:
   - Searches the pattern for the 64-ones/64-zeros segment of the compliance pattern.
   - Generates an impulse signal for each segment of the signal that meets the pattern.

4 Sets up the real time eye and fold the signal using the MATLAB generated signal as the clock recovery.

5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeros segment of the compliance pattern using the histogram.

6 Obtains the measurement of Vb at preset number P8.

7 Computes the de-emphasis at preset value P8.

8 Reports the measurement of Vb during preset values P6 and P8.

9 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), Preshoot

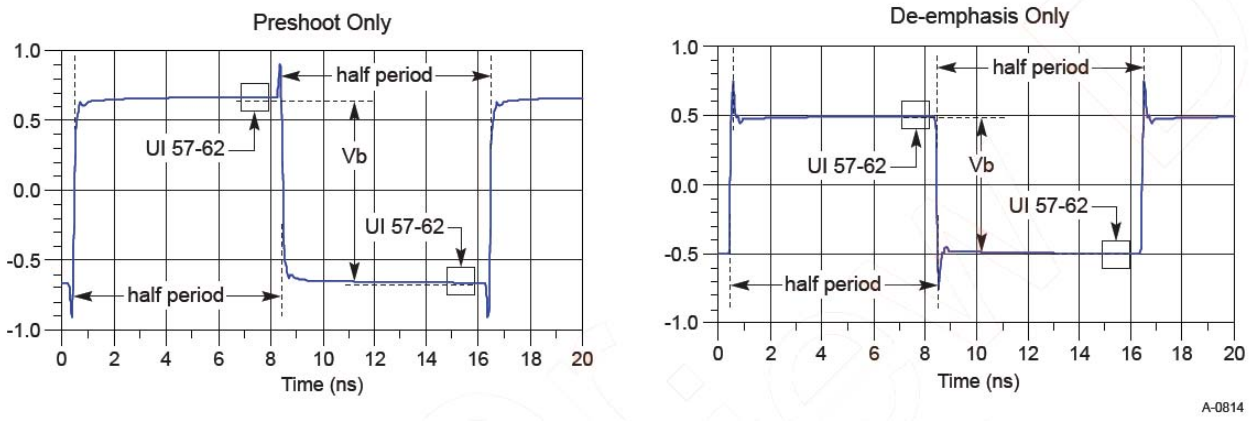
This test verifies that the preshoot of the preset number P8 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 161 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 162 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 1 dB	–3.5 ± 1 dB	–0.125	–0.125	0.750	0.500	0.750

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Preshoot P8**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s):

- Presets #8 measurement (P8), preshoot.
- Obtains the measurement of Vb at preset number P8 (Vb_P8).

- Obtains the measurement of Vb at preset number P3 (Vb_P3).
- Obtains the preshoot at preset value P8.

2 Reports the measurement of Vb during preset values P8 and P3.

3 Compares the preshoot value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), De-emphasis

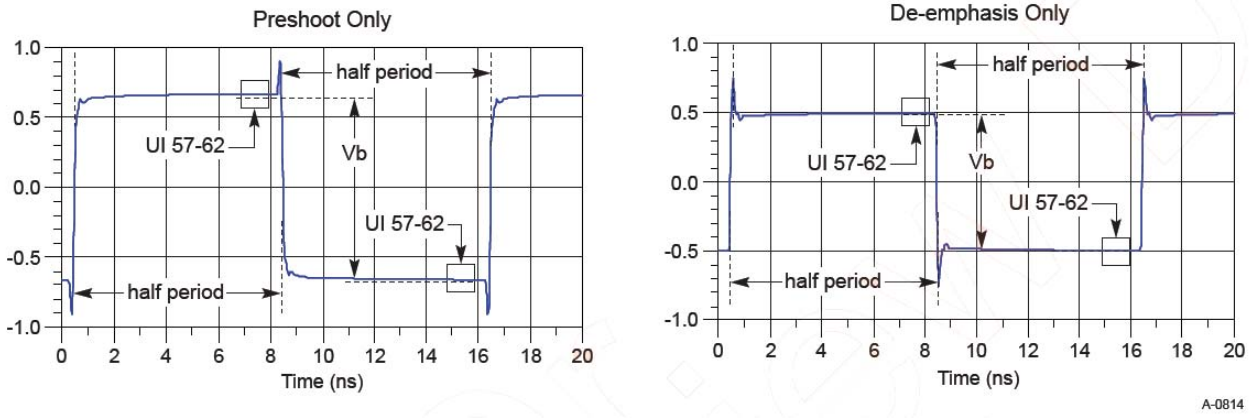
This test verifies that the de-emphasis of the preset number P7 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 163 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 164 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 1 dB	–6.0 ± 1.5 dB	–0.100	–0.200	0.800	0.400	0.600

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **De-emphasis P7**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s):

- Presets #5 measurement (P5), preshoot.

- Obtains the measurement of Vb at preset number P5 (Vb_P5).
- Presets #2 measurement (P2), de-emphasis.
- Obtains the measurement of Vb at preset number P2 (Vb_P2).

2 Sets up grid display settings on the oscilloscope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses the MATLAB function to generate the clock recovery for the 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:

- Searches the pattern for the 64-ones/64-zeros segment of the compliance pattern.
- Generates an impulse signal for each segment of the signal that meets the pattern.

4 Sets up the real time eye and fold the signal using the MATLAB generated signal as the clock recovery.

5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeros segment of the compliance pattern using the histogram.

6 Obtains the measurement of Vb at preset number P7.

7 Computes the preshoot at preset value P7.

8 Reports the measurement of Vb during preset values P5 and P7.

9 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), Preshoot

This test verifies that the preshoot of the preset number P7 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0, version 0.71.

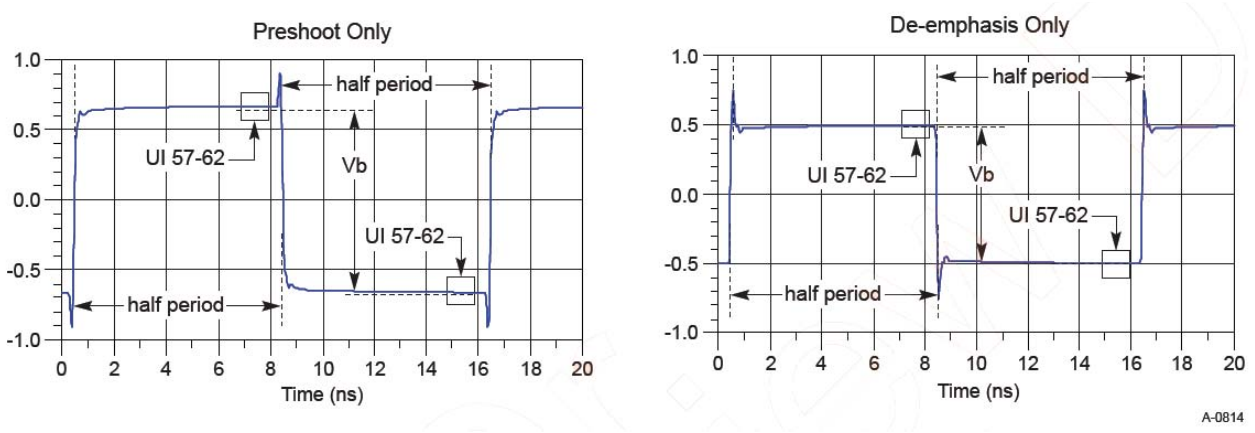
An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1}

and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 165 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 166 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 1 dB	–6.0 ± 1.5 dB	–0.100	–0.200	0.800	0.400	0.600

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Preshoot P7**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s):
   - Preset #7 measurement (P7), de-emphasis.
   - Obtains the measurement of Vb at preset number P7 (Vb_P7).
   - Obtains the measurement of Vb at preset number P2 (Vb_P2).
   - Obtains the preshoot at preset value P7.

2 Reports the measurement of Vb during preset values P7 and P2.

3 Compares the preshoot value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (P5), Preshoot

This test verifies that the preshoot of the preset number P5 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0, version 0.71

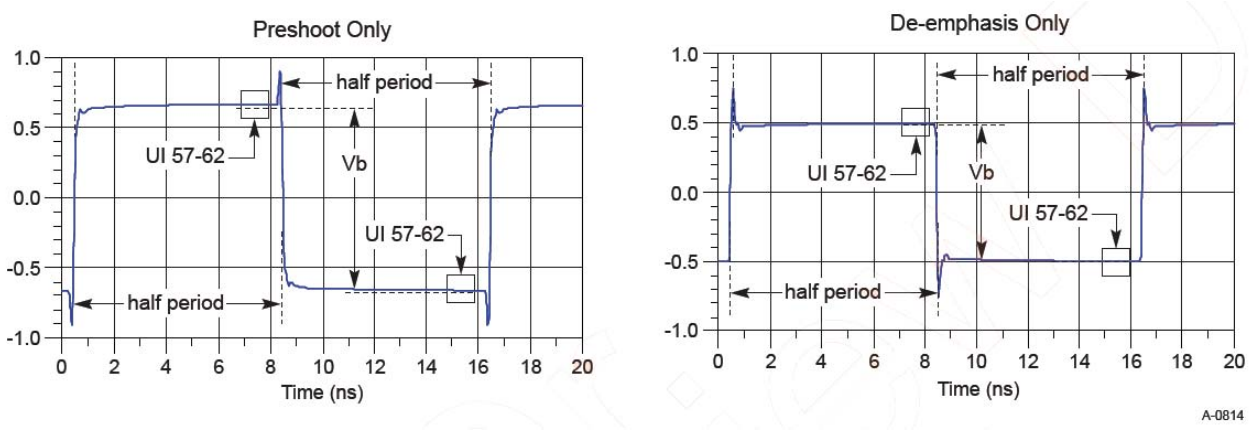
An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot

and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 167 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P5	N/A	P4/P5

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 168 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P5	1.9 ± 1 dB	0.0	–0.100	0.000	0.800	0.800	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Preshoot P5**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s):
   - Full swing Tx voltage with no TxEQ Preset #4.
   - Obtains the measurement of Vb at preset number P4 ($V_{TH\text{-}FS\text{-}NO\text{-}EQ}$).
2 Sets up grid display settings on the oscilloscope and zoom to the 64-ones/64-zeros segment of the compliance pattern.
3 Uses the MATLAB function to generate the clock recovery for the 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:
   - Searches the pattern for the 64-ones/64-zeros segment of the compliance pattern.
   - Generates an impulse signal for each segment of the signal that meets the pattern.
4 Sets up the real time eye and fold the signal using the MATLAB generated signal as the clock recovery.
5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeroes segment of the compliance pattern using the histogram.
6 Obtains the measurement of Vb at preset number P5.
7 Computes the preshoot at preset value P5.
8 Reports the measurement of Vb during preset values P5 and P4.
9 Compares the preshoot value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in

the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #6 Measurement (P6), Preshoot

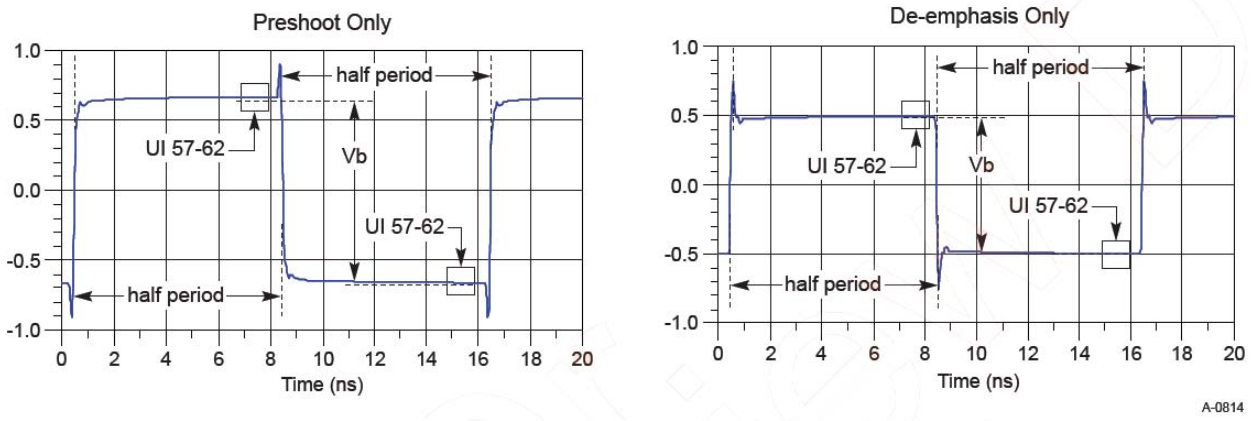
This test verifies that the preshoot of the preset number P6 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 169 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P6	N/A	P4/P6

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 170 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P6	2.5 ± 1 dB	0.0	–0.125	0.000	0.750	0.750	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **Preshoot P6**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s):

- Full swing Tx voltage with no TxEQ Preset #4

- Obtains the measurement of Vb at preset number P4 ($V_{TH\text{-}FS\text{-}NO\text{-}EQ}$)

2 Sets up grid display settings on the oscilloscope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses the MATLAB function to generate the clock recovery for the 64-ones/64-zeros segment of the compliance pattern.

4 The MATLAB function does the following:

- Searches the pattern for the 64-ones/64-zeros segment of the compliance pattern.
- Generates an impulse signal for each segment of the signal that meets the pattern.

5 Sets up the real time eye and fold the signal using the MATLAB generated signal as the clock recovery.

6 Measures the voltage level at UI 57-62 for each 64-ones/64-zeros segment of the compliance pattern using the histogram.

7 Obtains the measurement of Vb at preset number P6.

8 Computes the preshoot at preset value P6.

9 Reports the measurement of Vb during preset values P6 and P4.

10 Compares the preshoot value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #3 Measurement (P3), De-emphasis

This test verifies that the de-emphasis of the preset number P3 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0, version 0.71.

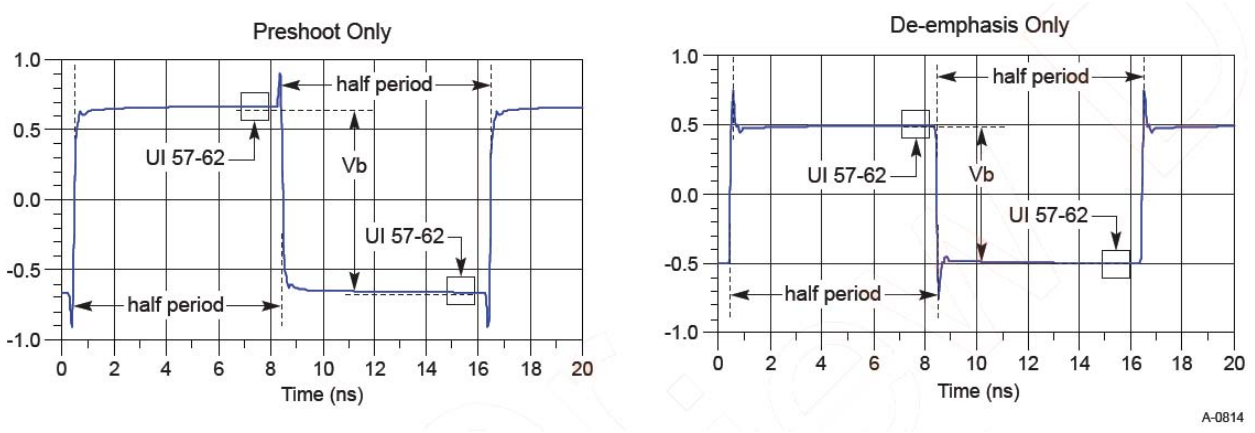
An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1}

and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 171 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P3	P3/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 172 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P3	0.0	–2.5 ± 1 dB	0.000	–0.125	1.000	0.750	0.750

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **De-emphasis P3**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s).
   - Full swing Tx voltage with no TxEQ Preset #4s
   - Obtains the measurement of Vb at preset number P4 ($V_{TH\text{-}FS\text{-}NO\text{-}EQ}$)s

2 Sets up grid display settings on the oscilloscope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses the MATLAB function to generate the clock recovery for the 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:
   - Searches the pattern for the 64-ones/64-zeros segment of the compliance pattern.
   - Generates an impulse signal for each segment of the signal that meets the pattern.

4 Sets up the real time eye and fold the signal using the MATLAB generated signal as the clock recovery.

5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeros segment of the compliance pattern using the histogram.

6 Obtains the measurement of Vb at preset number P3.

7 Computes the de-emphasis at preset value P3.

8 Reports the measurement of Vb during preset values P3 and P4.

9 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #2 Measurement (P2), De-emphasis

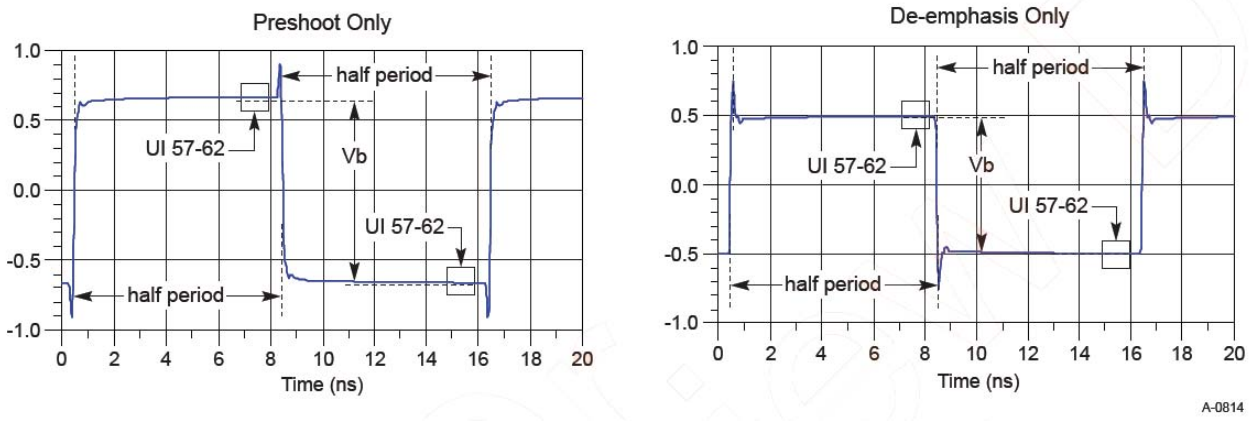
This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 173 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P2	P2/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 174 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P2	0.0	–4.4 ± 1.5 dB	0.000	–0.200	1.000	0.600	0.600

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **De-emphasis P2**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s).

- Full swing Tx voltage with no TxEQ Preset #4.

- Obtains the measurement of Vb at preset number P4 ($V_{TH-FS-NO-EQ}$).

2 Sets up grid display settings on the oscilloscope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses the MATLAB function to generate the clock recovery for the 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:

- Searches the pattern for the 64-ones/64-zeros segment of the compliance pattern.
- Generates an impulse signal for each segment of the signal that meets the pattern.

4 Sets up the real time eye and fold the signal using the MATLAB generated signal as the clock recovery.

5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeroes segment of the compliance pattern using the histogram.

6 Obtains the measurement of Vb at preset number P2.

7 Computes the de-emphasis at preset value P2.

8 Reports the measurement of Vb during preset values P2 and P4.

9 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #10 Measurement (P10), De-emphasis

This test verifies that the de-emphasis of the preset number P10 is within the conformance limits specified in Table 4-16 of the PCIE Base Specification, rev. 3.0.

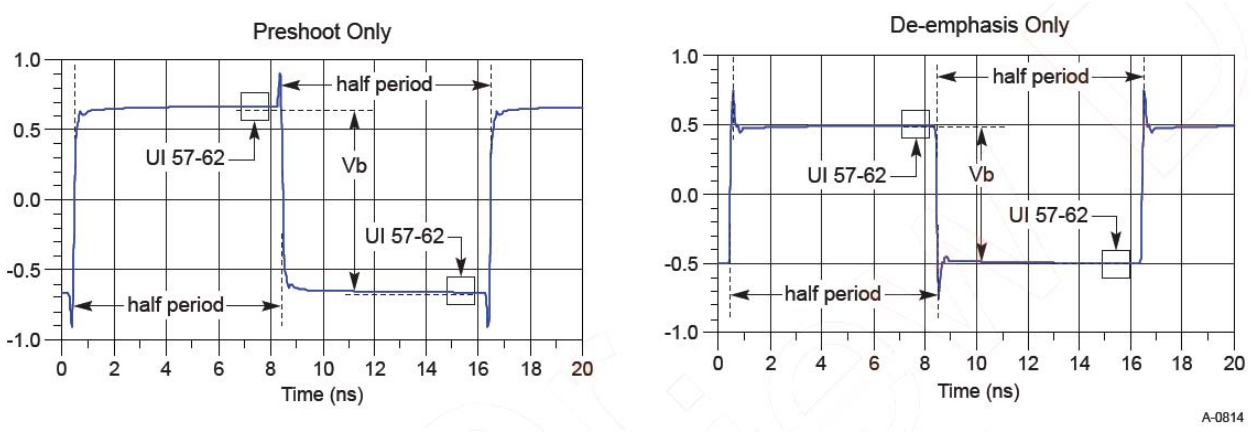
An 8.0 GT/s transmitter must support a limited number of presets. Presets are defined in terms of two ratios, relating the precursor and postcursor equalization voltages. The precursor (Vc) is referred to as preshoot, while the postcursor (Va) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s/5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1}

and c_{-1} are nonzero, the swings of Va and Vb do not reach the maximum as defined by Vd. The high frequency nature of 8.0 GT/s signaling makes the measurement of single UI pulse heights impractical.

Table 175 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P10	P10/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.



Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16 is used as reference to check the compliance of the DUT.

Table 176 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P10	0.0	See below Note.	0.000	See below Note.	1.000	See below Note.	See below Note.

Test Definition Notes from the Specification

P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The allowable P10 boost range is defined by the coefficient space lying between the two diagonal lines in Figure 4-50. This approach permits both full and reduced swing transmitters to use P10 for testing to their respective boost limits.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Tx Tests" on page 472 and select **De-emphasis P10**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 This test requires the following pre-requisite test(s).
   - Full swing Tx voltage with no TxEQ
   - Obtains the measurement of Vb at preset number P4 ($V_{TH\text{-}FS\text{-}NO\text{-}EQ}$)

2 Sets up grid display settings on the oscilloscope and zoom to the 64-ones/64-zeros segment of the compliance pattern.

3 Uses the MATLAB function to generate the clock recovery for the 64-ones/64-zeros segment of the compliance pattern. The MATLAB function does the following:
   - Searches the pattern for the 64-ones/64-zeros segment of the compliance pattern.
   - Generates an impulse signal for each segment of the signal that meets the pattern.

4 Sets up the real time eye and fold the signal using the MATLAB generated signal as the clock recovery.

5 Measures the voltage level at UI 57-62 for each 64-ones/64-zeros segment of the compliance pattern using the histogram.

6 Obtains the measurement of Vb at preset number P10.

7 Computes the de-emphasis at preset value P10.

8 Reports the measurement of Vb during preset values P10 and P4.

9 Compares the de-emphasis value to the compliance test limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

25
Add-In Card (Tx) Tests, 8.0 GT/s, PCI-E 3.0

This section provides the Methods of Implementation (MOIs) for Transmitter (Tx) tests of PCI-E 3.0 using an Agilent 90000X series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for Add-In Card Compliance

Connecting the Compliance Base Board for Add-in Card Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the Add-in card fixture power supply powered off, connect the power supply connector to the Add-in card test fixture, and connect the device under test add-in card to the by-16 connector slot.

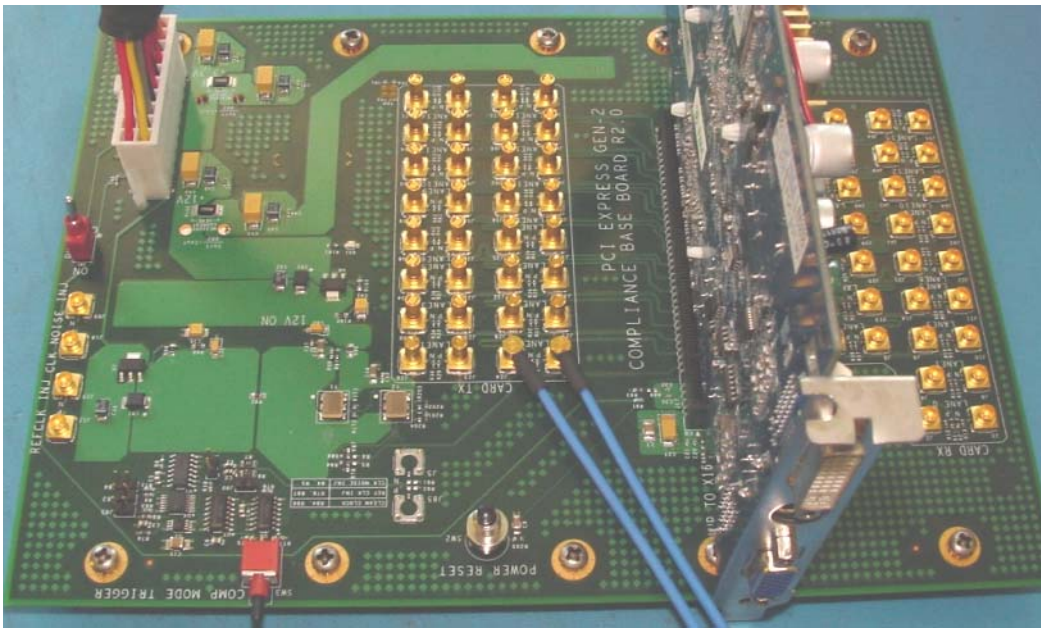


Figure 244 Compliance Base Board (CBB) Add-in Card Fixture

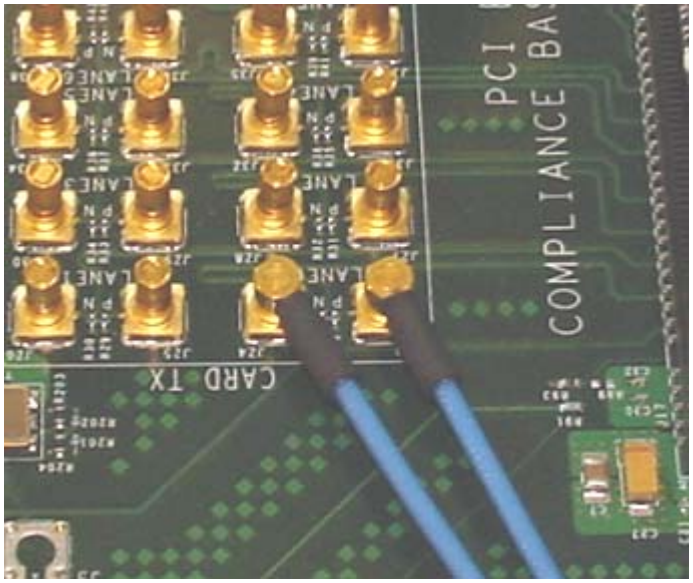


Figure 245 Compliance Base Board (CBB) 2.0 SMP Probing Option

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

   a Digital Storage Oscilloscope channel 1 to the D+ (where Lane 1 is under test in this example shown in Figure 245 above).

   b Digital Storage Oscilloscope channel 3 to the D- (where Lane 1 is under test in this example shown in Figure 245 above).

   When SMP probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 626).

   Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

   When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

4 Connect adequate load to the power supply to assure it is regulating and turned on. Generally, one IDE hard drive will provide adequate load.

5 Turn on the power supply. DS1 LED (located near the ATX power supply connector) should turn on. If the LED is on, but the power supply does not turn on, check that the jumper J7 is installed between J7-1 and J7-2.

Running Add-In Card Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "Add-In Card (Tx) Tests" group.

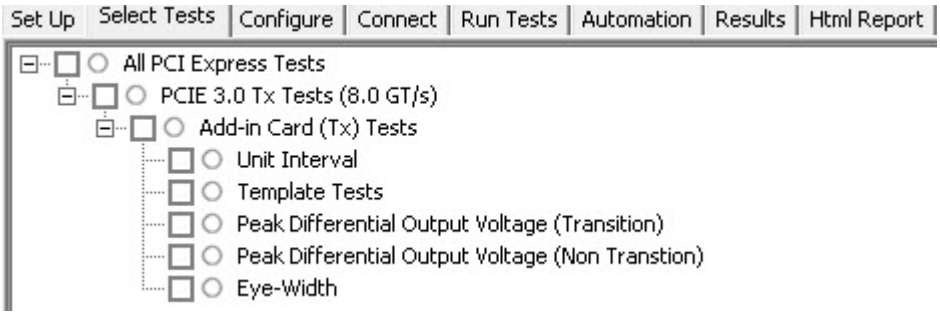


Figure 246 Selecting Add-In Card (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

PCI Express Base Specification, Rev 2.0, Section 4.3.3.13, Table 4-18 is used as reference to check the compliance of the DUT.

Table 177 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	124.9625 ps	125.0375 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Add-In Card Tests" on page 543 and select **Unit Interval**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

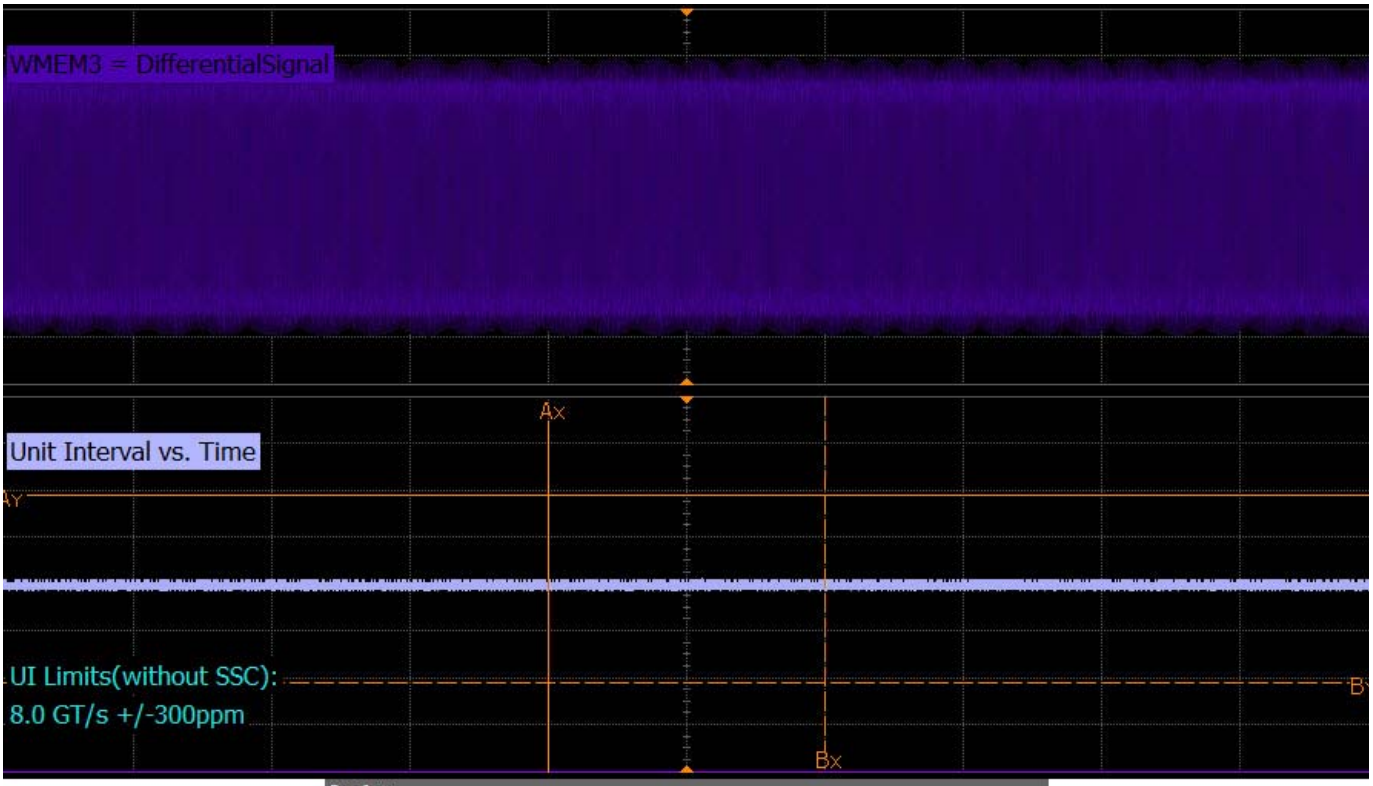
4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 3.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	20.00 µs/div	0.000s	20.00 fs/div	125.0 ps
Memory 3	20.00 µs/div	0.000s	190.0 mV/div	5.851 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-20.0000000076000 µs	100 pV
B	Function 3	20.0000000076000 µs	100 pV

Figure 247 Reference Image for Unit Interval Test

Template Tests

Add-in cards must meet the **Add-in Card Transmitter Path Compliance Eye-Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 3.0, Section 4.8.3, Table 4-11 as measured at the card edge-fingers. This test does not validate the receiver's tolerance, rather it validates that the signal at the receiver meets the specifications in Figure 4-7.

All links are assumed active while generating this eye diagram. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (Vtx_{A_d}).

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.8.3 is used as reference to check the compliance of the DUT.

Table 178 Template Test Details

Symbol	Min	Max
V_{TXA}	34 mV	1200 mV
V_{TXA_d}	34 mV	1200 mV
T_{TXA}	41.25 ps	

Test Definition Notes from the Specification

- A worst case reference clock with 1 ps RMS jitter is assumed for this revision of the specification. All links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (PCI Express Base Specification, Revision 3.0, Section 4.2.10) is being transmitted during the test.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER 10^{-6} is 46mV.

- The values in Table 4-11 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 ohm trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0GT/s Add-in Card Test Channel. S-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up must be removed. Note that the Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

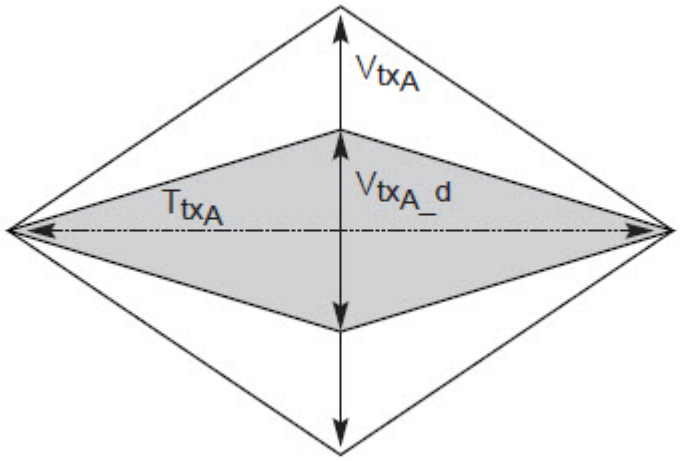


Figure 248 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running Add-In Card Tests" on page 543 and select **Template Tests -3.5dB**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 2.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is

captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

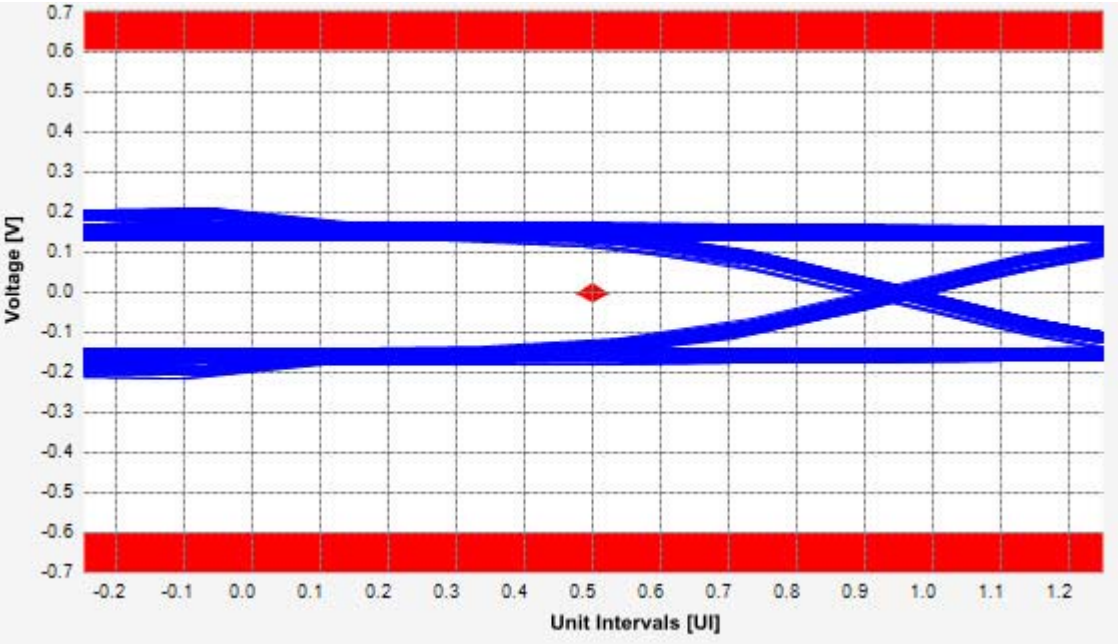


Figure 249 Reference Image for Template (Transition) Test

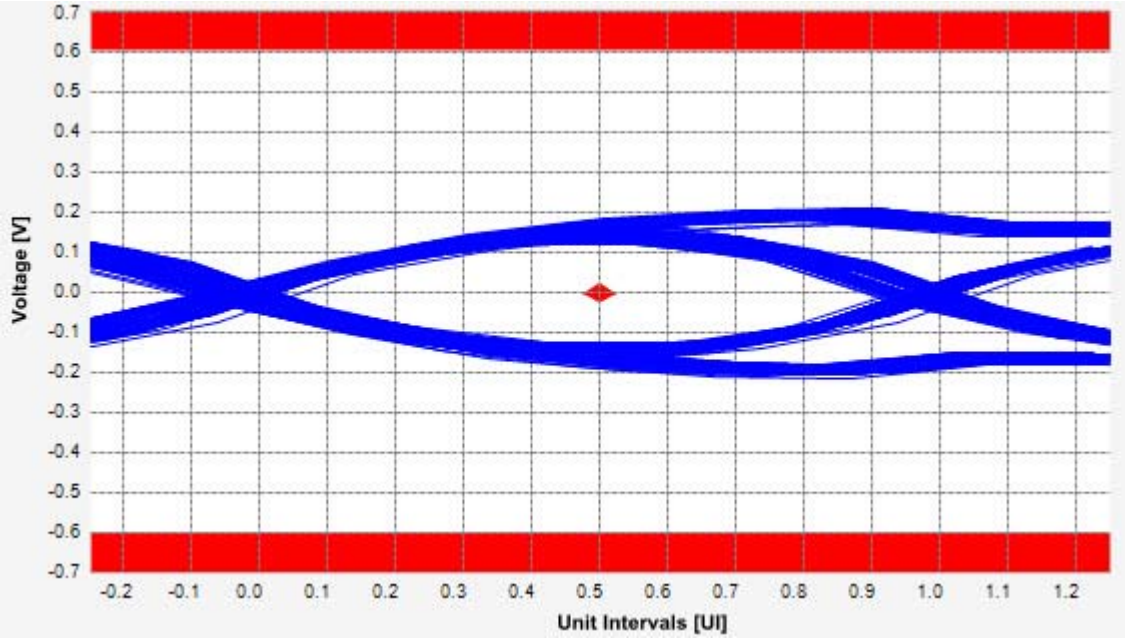


Figure 250 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.8.3, Table 4-11 used as reference to check the compliance of the DUT.

Table 179 Peak Differential Output Voltage (Transition) Test Details

Symbol	Min	Max
V_{TXA}	34 mV	1200 mV
V_{TXA_d}	34 mV	1200 mV
T_{TXA}	41.25 ps	

Test Definition Notes from the Specification

- A worst case reference clock with 1 ps RMS jitter is assumed for this revision of the specification. All links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (PCI Express Base Specification, Revision 3.0, Section 4.2.10) is being transmitted during the test.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER 10^{-6} is 46mV.

- The values in Table 4-11 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 ohm trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0GT/s Add-in Card Test Channel. S-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up must be removed. Note that the Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard

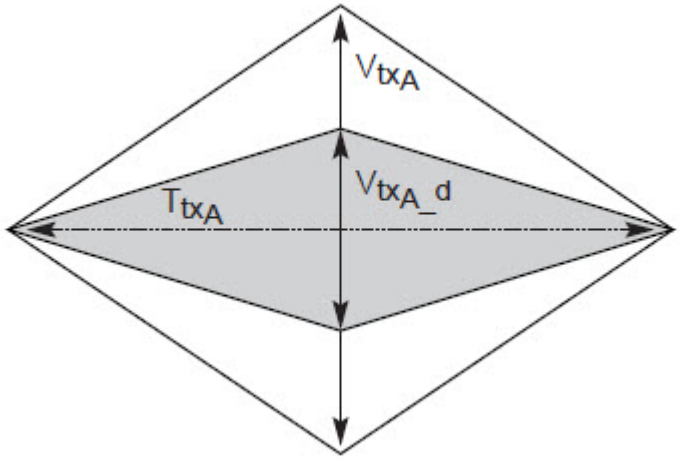


Figure 251 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 543 and select **Peak Differential Output Voltage -3.5dB (Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE3.0

Data Rate: 8.0GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

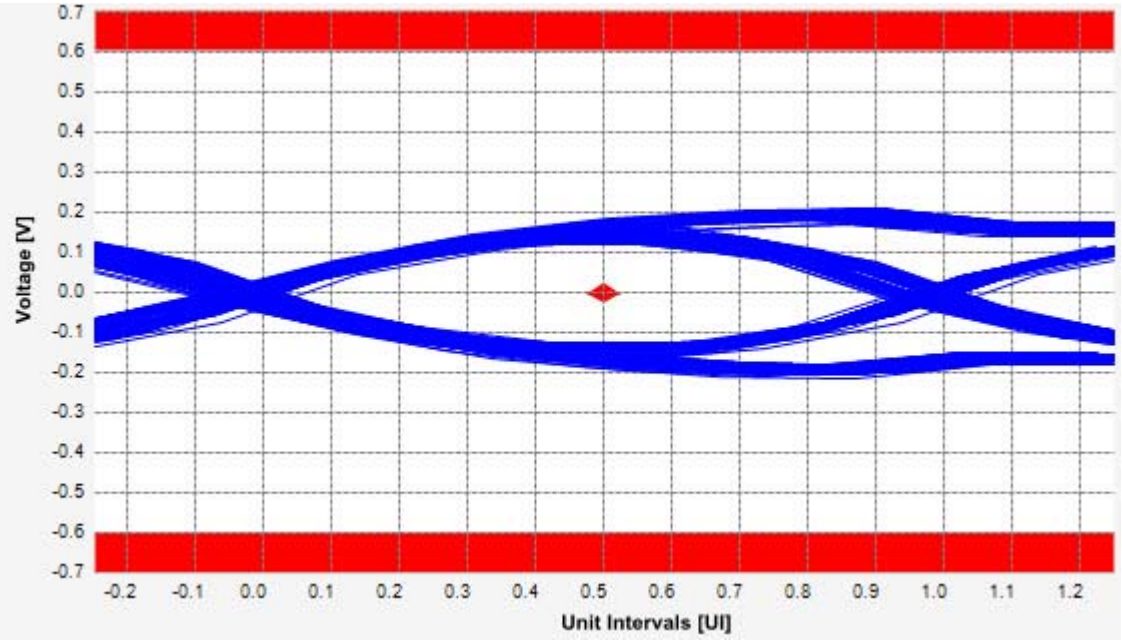


Figure 252 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 2.0, Section 4.8.3, Table 4-11 is used as reference to check the compliance of the DUT.

Table 180 Peak Differential Output Voltage (Non-transition) Test Details

Symbol	Min	Max
V_{TXA}	34 mV	1200 mV
V_{TXA_d}	34 mV	1200 mV
T_{TXA}	41.25 ps	

Test Definition Notes from the Specification

- A worst case reference clock with 1 ps RMS jitter is assumed for this revision of the specification. All links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (PCI Express Base Specification, Revision 3.0, Section 4.2.10) is being transmitted during the test.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER 10^{-6} is 46mV.

- The values in Table 4-11 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 ohm trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0GT/s Add-in Card Test Channel. S-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up must be removed. Note that the Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

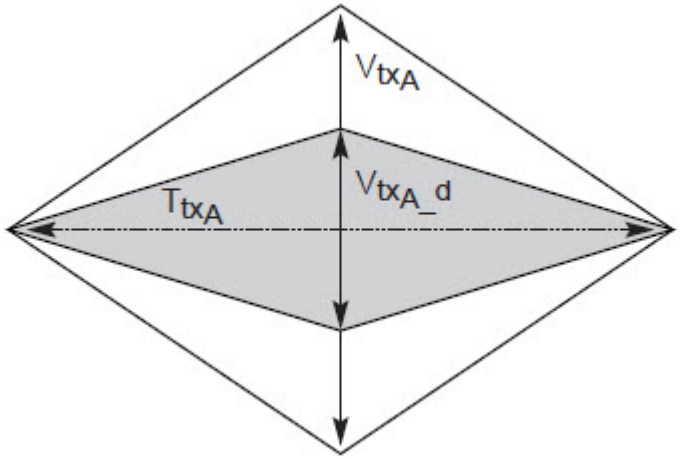


Figure 253 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 543 and select **Peak Differential Output Voltage -3.5dB (Non Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE3.0

Data Rate: 8.0GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (non transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

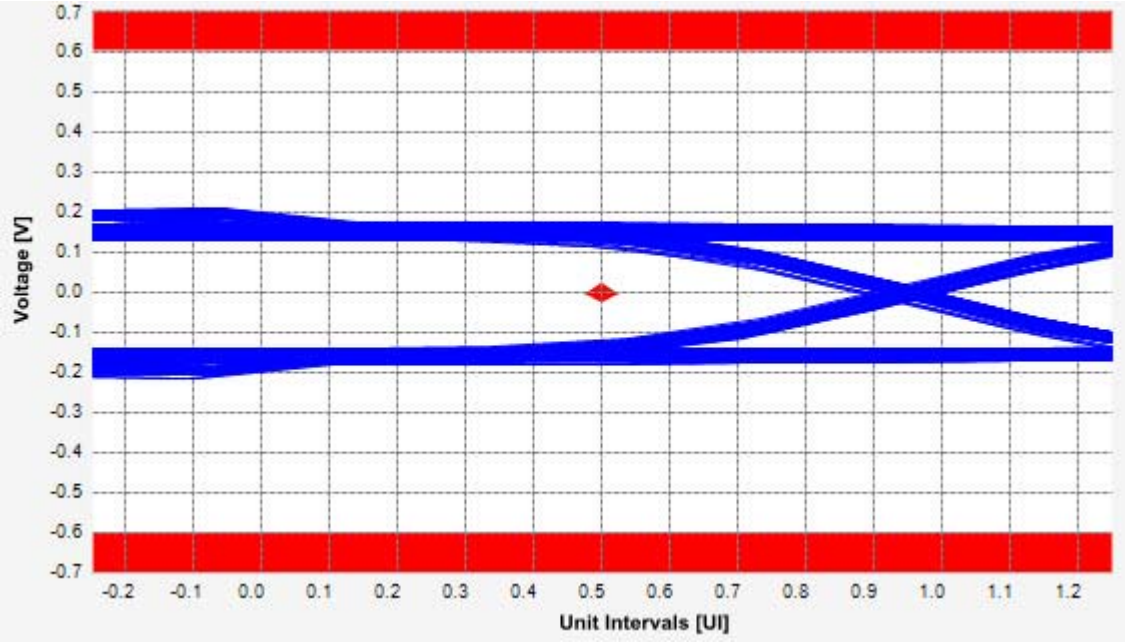


Figure 254 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER-12]$$

Test Reference

PCI Express CEM Specification, Rev 3.0, Section 4.8.3 is used as reference to check the compliance of the DUT.

Table 181 Eye Width - 3.5dB (with or without crosstalk) Test Details

Symbol	Min	Max
V_{TXA}	34 mV	1200 mV
V_{TXA_d}	34 mV	1200 mV
T_{TXA}	41.25 ps	

Test Definition Notes from the Specification

- A worst case reference clock with 1 ps RMS jitter is assumed for this revision of the specification. All links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (PCI Express Base Specification, Revision 3.0, Section 4.2.10) is being transmitted during the test.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER 10^{-6} is 46mV.
- The values in Table 4-11 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 ohm trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0GT/s Add-in Card Test Channel. S-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up must be removed. Note that the Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

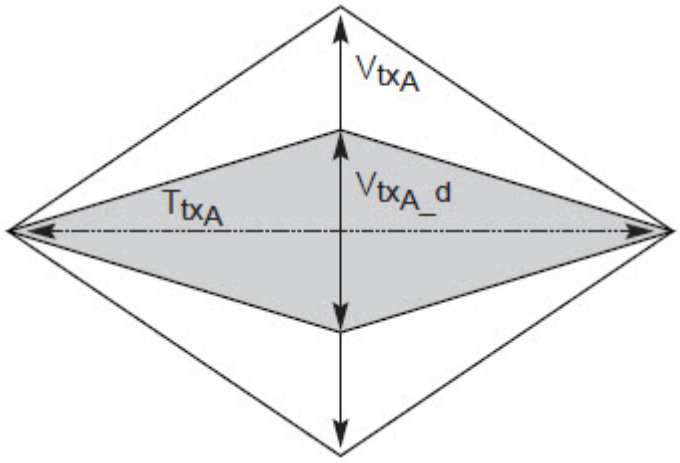


Figure 255 Add-in Card Transmitter Path Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running Add-In Card Tests" on page 543 and select **Eye Width -3.5dB with crosstalk**

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE3.0

Data Rate:8.0GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to

view the details. For information about the test results, refer to **Viewing Results** in the online help.

26
System Board (T_X) Tests, PCI-E 3.0

This section provides the Methods of Implementation (MOIs) for Transmitter (Tx) tests of PCI-E 3.0 using an Agilent 90000X series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

Probing the Link for System Board Compliance

Connecting the Signal Quality Load Board for System/Motherboard Testing

There are multiple pairs of SMP connectors on the PCI Express Signal Quality Test Fixtures. Each pair maps to the transmit differential pair or receive differential pair for the Add-in Card or System/motherboard transmitter lane under test.

1 With the system/motherboard powered off, connect the Compliance PCI Express Signal Quality Load Board into the connector under test. The are 2 types of PCI Express Signal Quality Load Board edge fingers combination available - x1 and x16 connectors, as well as x4 and x8 connectors.

   The PCI Express Signal Quality Load Board will cause a PCI Express 2.0 Base Specification System/motherboard to enter the compliance sub-state of the polling state. During this state the device under test will repeatedly send out the compliance pattern defined in the PCI Express Base Specification.

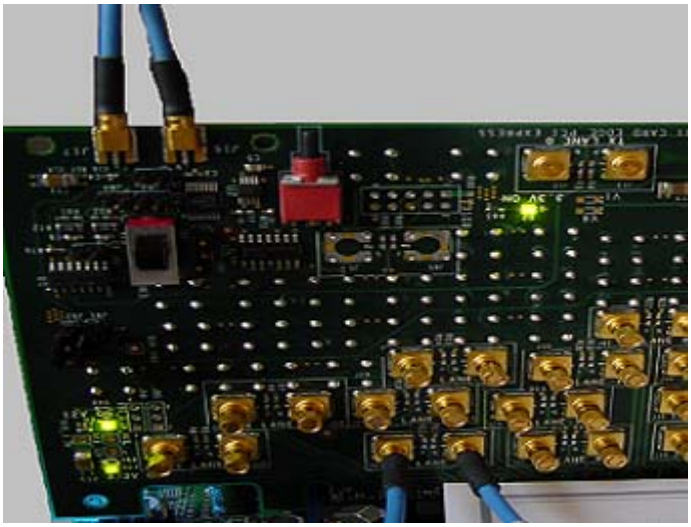


Figure 256 SMP Probing Option

2 Provide the proper Compliance Test Pattern by clicking the toggle switch until you reach the desired mode. The available options are 2.5 GHz at -3.5 dB de-emphasis mode, 5.0 GHz at -3.5 dB and 5.0 GHz at 6.0 dB.

3 Connect cables up as follows:

a Digital Storage Oscilloscope channel 1 to Data and Channel 3 to Clock OR

b Digital Storage Oscilloscope channel 2 to Data and Channel 4 to Clock.

When SMP probing and two channels are used, channel-to-channel deskew is required (see "Channel-to-Channel De-skew" on page 626).

Not all lanes have SMP probing options. For signal quality testing of the remaining lanes you will need to use a high bandwidth differential or single ended probes. For more information on the probe amplifiers and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

When using differential probe heads, make sure the polarity is correct. The polarity of the probe is identified on the end of the probe amplifier.

Running System Board Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to the "System Board (Tx) Tests" group.

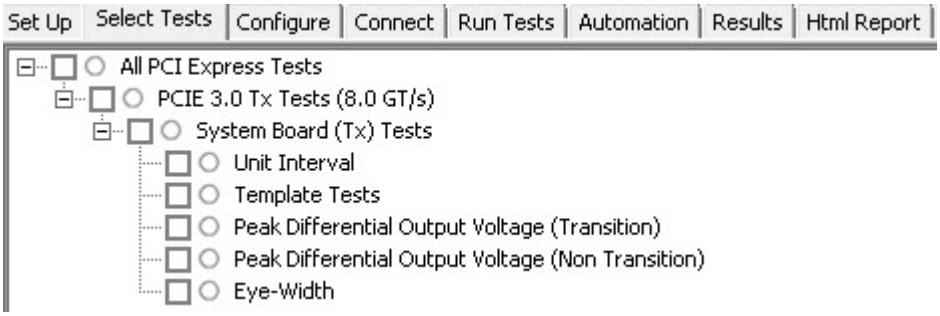


Figure 257 Selecting System Board (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 3500 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \quad UI(p) = Mean \quad (UI(n))$$

Where,

'n' is the index of UI in the current 3500 UI clock recovery window.

'p' indicates the p^{th} 3500 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 3500 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

NOTE The UI range for this test is not specified in the CEM specifications document. This test provides informative test only.

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.3.13, Table 4-18 is used as reference to check the compliance of the DUT.

Figure 258 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	124.9625 ps	125.0375 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.
- SSC permits a +0, -5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33KHz.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running System Board Tests" **on page 563** and select **Unit Interval.**

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.

   a Selects **Unit Interval** as data measurement analysis unit.

   b Configures the **Smoothing Points** to 3499 in the Measurement Trend dialog box.

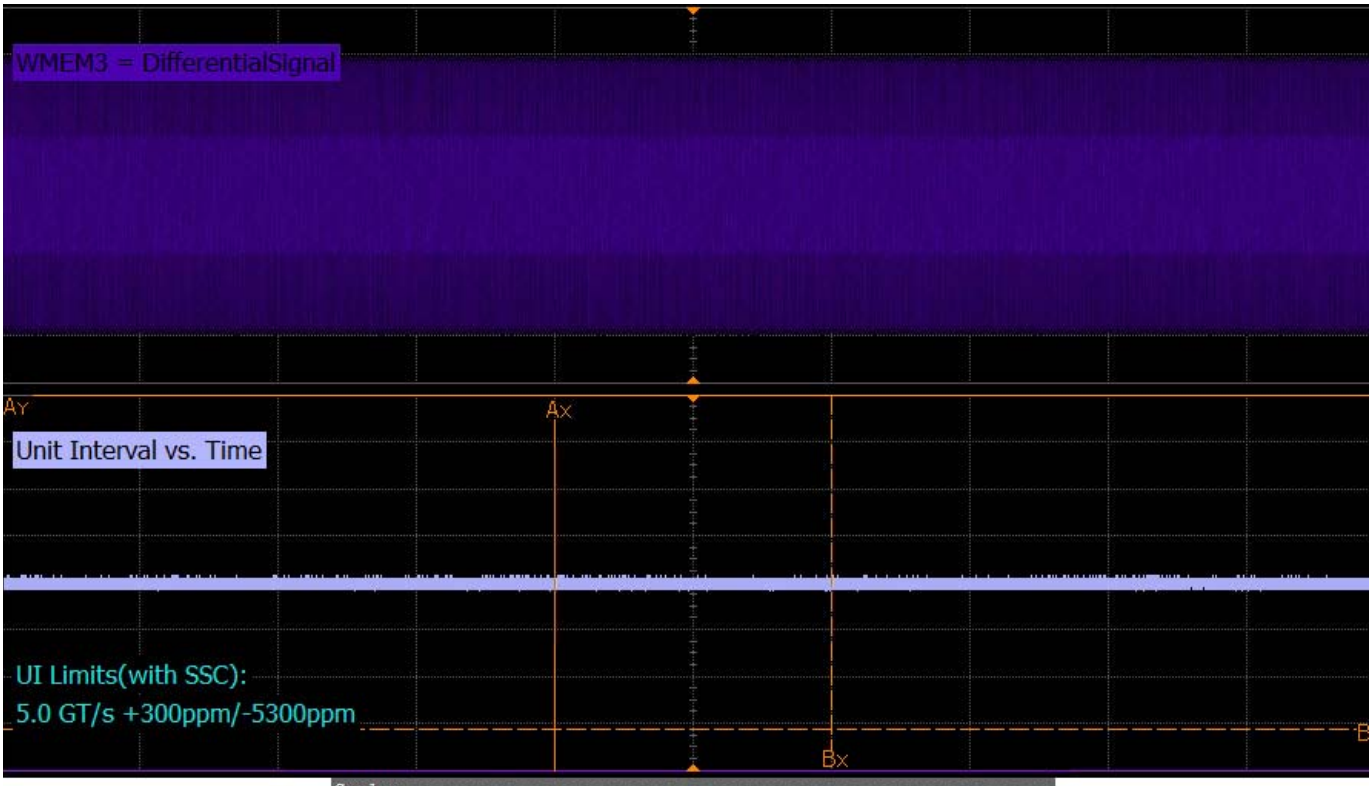
4 Indicates the upper and lower limit of the measured data using markers.

5 Measures the minimum, mean and maximum values of the UI.

6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 3.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	32.00 µs/div	0.000s	20.00 fs/div	200.0 ps
Memory 3	32.00 µs/div	0.000s	162.5 mV/div	3.356 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-32.0000000080000 µs	200 pV
B	Function 3	32.0000000080000 µs	200 pV

Figure 259 Reference Image for Unit Interval Test

Template Tests

System boards must meet the **System Board Transmitter Path Compliance Eye Diagram** requirements as specified in PCI Express Card Electromechanical Specification (CEM) Rev 3.0, Section 4.8.9, Table 4-19 as measured after the connector with an ideal load.

Test Reference

PCI Express CEM Specification, Rev 3.0, Section 4.8.9 is used as reference to check the compliance of the DUT.

Table 182 Template Test Details

Symbol	Min	Max
V_{TXA}	34 mV	1200 mV
V_{TXA_d}	34 mV	1200 mV
T_{TXA}	41.25 ps	

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (PCI Express Base Specification, Revision 3.0, Section 4.2.10) is being transmitted during the test.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER 10^{-6} is 46mV.
- The values in Table 4-19 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 ohm trace, followed by a reference receiver package behind a standard PCI Express edge finger. This channel shall be referenced as the 8.0GT/s System Board Test Channel. The s-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up must be removed. Note that the System Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant add-in card.

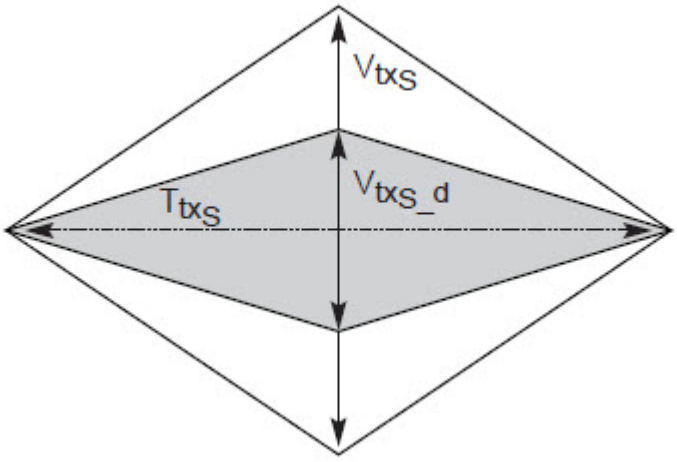


Figure 260 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 2.0. To execute the test, follow the procedure in "Running System Board Tests" on page 563 and select **Template Tests**.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Performs compliance testing using the SigTestWrapper.dll file.

   a Calls the add-in card compliance test function from the SigTestWrapper.dll file.

   b Gets transition failure and non-transition failure test results from the SigTestWrapper.dll file.

3 Identifies mask failures in both the transition and non-transition eye diagrams and reports the test as failed in case mask failure is encountered.

4 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express CEM Specification, Rev 2.0 and the total number of mask violation is zero.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

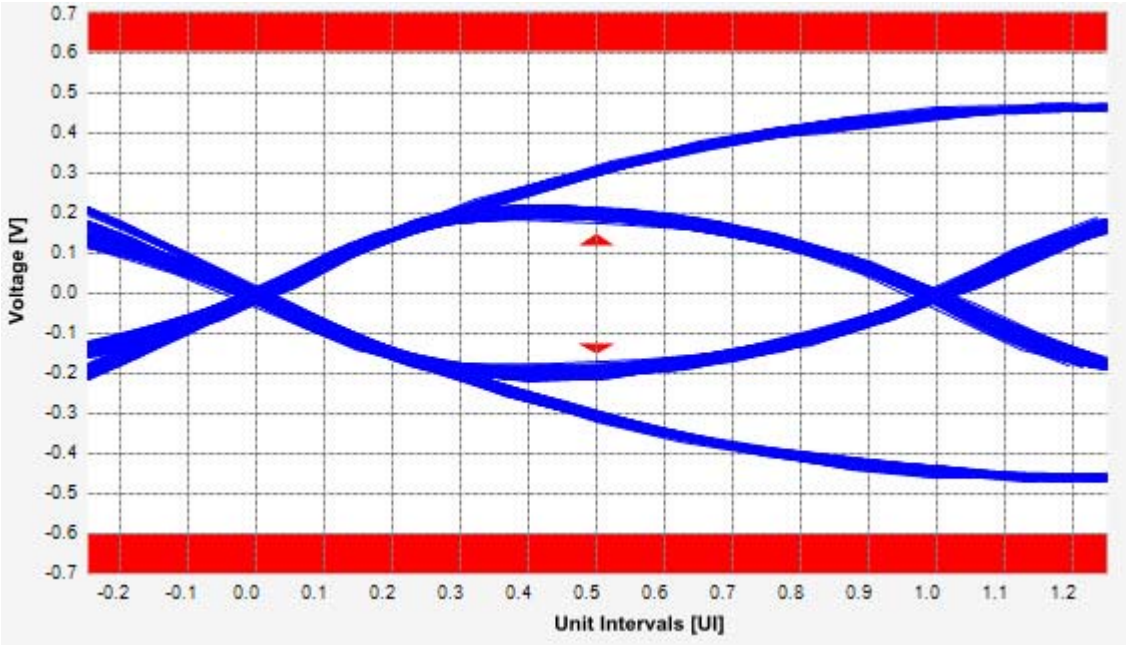


Figure 261 Reference Image for Template (Transition) Test

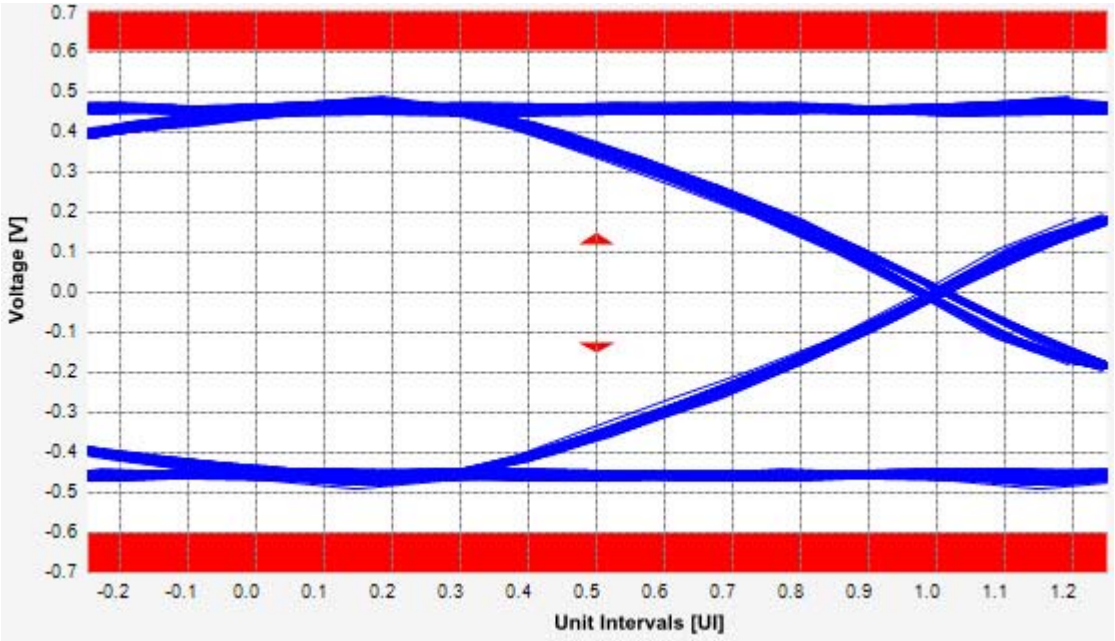


Figure 262 Reference Image for Template (Non-Transition) Test

Peak Differential Output Voltage (Transition) Test

The **Peak Differential Output Voltage** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 3.0, Section 4.8.9 is used as reference to check the compliance of the DUT.

Table 183 Peak Differential Output Voltage (Transition) Test Details

Symbol	Min	Max
V_{TXA}	34 mV	1200 mV
V_{TXA_d}	34 mV	1200 mV
T_{TXA}	41.25 ps	

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (PCI Express Base Specification, Revision 3.0, Section 4.2.10) is being transmitted during the test.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER 10^{-6} is 46mV.
- The values in Table 4-19 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 ohm trace, followed by a reference receiver package behind a standard PCI Express edge finger. This channel shall be referenced as the 8.0GT/s System Board Test Channel. The s-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up must be removed. Note that the System Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant add-in card.

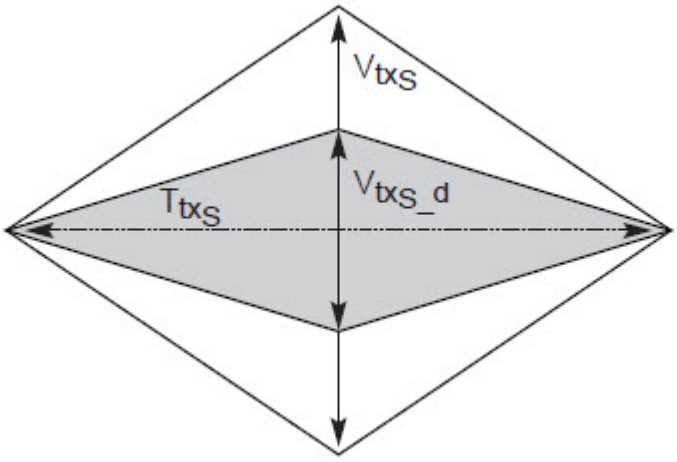


Figure 263 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 563 and select **Peak Differential Output Voltage (Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE3.0

Data Rate: 8.0GT/s

1 Extracts the transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest transition amplitude (outer eye), smallest transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (transition) value to the compliance test limits.

5 Reports the measurement results.

6

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

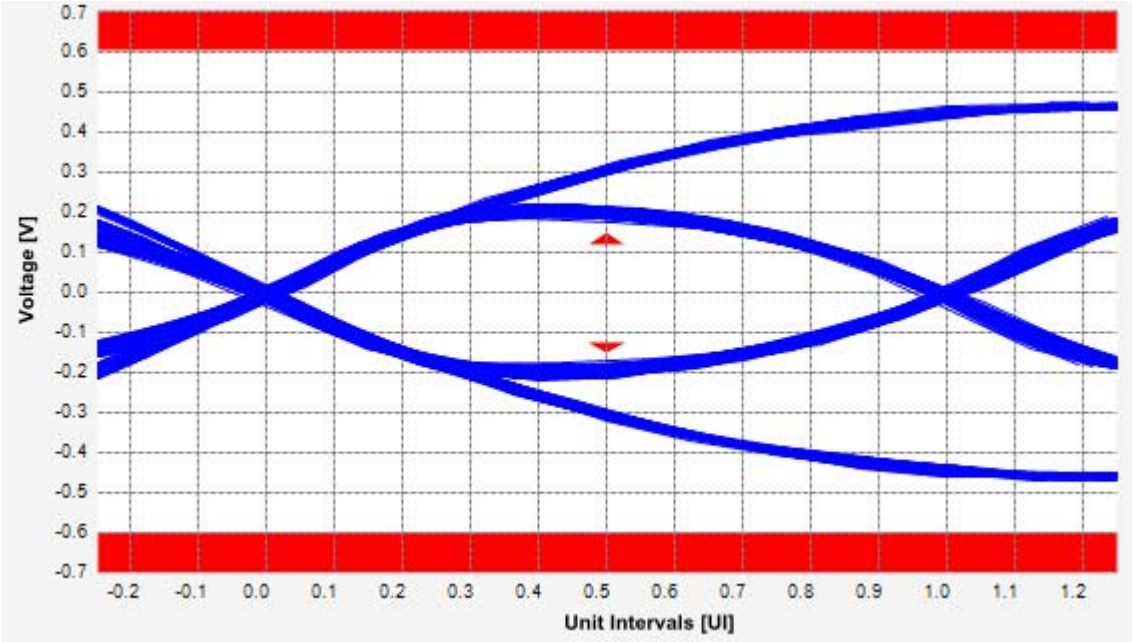


Figure 264 Reference Image for Peak Differential Output Voltage Test

Peak Differential Output Voltage (Non-Transition) Test

The **Peak Differential Output Voltage (non-transition)** test measures and returns two times the larger of the minimum or maximum statistic of the differential voltage waveform and is calculated using the following formula:

$$V_{TX-DIFF-p-p} = 2*Max(Max(V_{DIFF(i)}),Min(V_{DIFF(i)}))$$

Where,

'i' is the index of all waveform values.

'V_{DIFF}' is the differential voltage signal.

Test Reference

PCI Express CEM Specification, Rev 3.0, Section 4.8.9 is used as reference to check the compliance of the DUT.

Table 184 Peak Differential Output Voltage (Non Transition) Test Details

Symbol	Min	Max
V_{TXA}	34 mV	1200 mV
V_{TXA_d}	34 mV	1200 mV
T_{TXA}	41.25 ps	

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (PCI Express Base Specification, Revision 3.0, Section 4.2.10) is being transmitted during the test.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER 10^{-6} is 46mV.
- The values in Table 4-19 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 ohm trace, followed by a reference receiver package behind a standard PCI Express edge finger. This channel shall be referenced as the 8.0GT/s System Board Test Channel. The s-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up must be removed. Note that the System Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant add-in card.

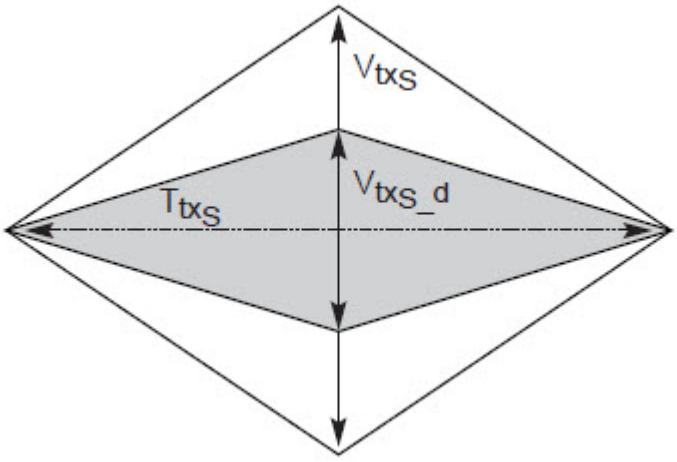


Figure 265 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 563 and select **Peak Differential Output Voltage (Non Transition)**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE3.0

Data Rate: 8.0GT/s

1 Extracts the non transition eye diagram data from the SigTestWrapper.dll file.

2 Gets largest non transition amplitude (outer eye), smallest non transition amplitude (inner eye) test results from SigTestWrapper.dll file.

3 Finds the peak differential output voltage (non transition) mean value from the center of UI.

4 Compares the measured peak differential output voltage (non transition) value to the compliance test limits.

5 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

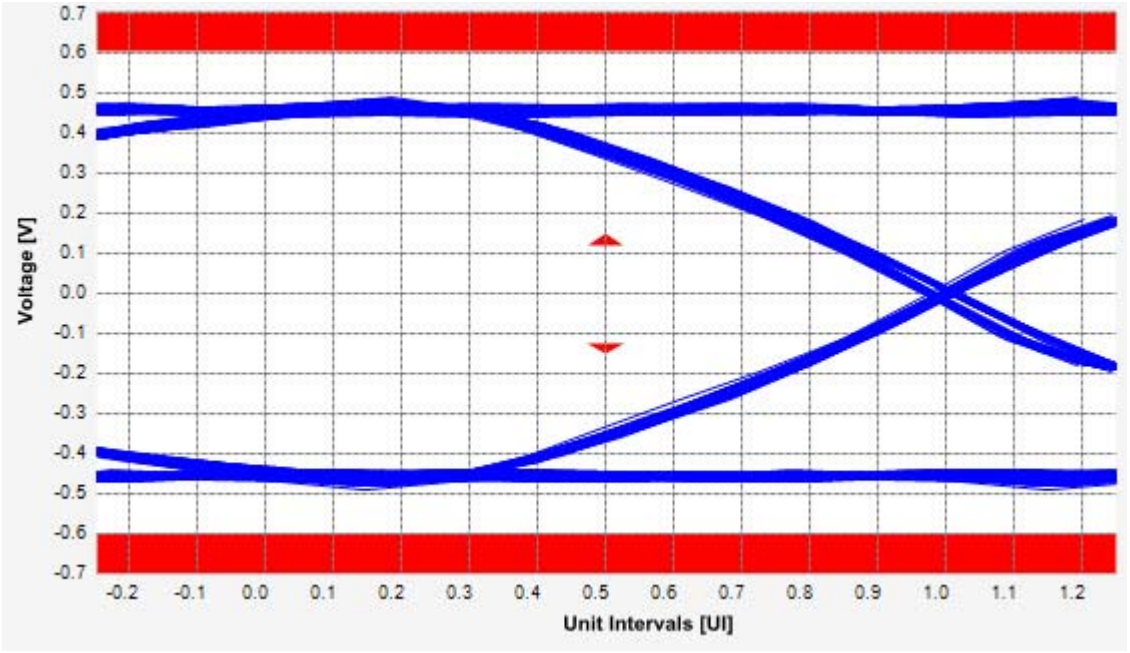


Figure 266 Reference Image for Peak Differential Output Voltage Test

Eye-Width Test

The **Eye-Width** test measures the compliance width of the compliance eye. This parameter is measured with the equivalent of a zero jitter reference clock. The eye-width is computed using the following formula:

$$Eye-width = [MeanUnitInterval] - [TotalJitteratBER-12]$$

Test Reference

PCI Express CEM Specification, Rev 3.0, Section 4.8.9 is used as reference to check the compliance of the DUT.

Table 185 Eye Width Test Details

Symbol	Min	Max
V_{TXA}	34 mV	1200 mV
V_{TXA_d}	34 mV	1200 mV
T_{TXA}	41.25 ps	

Test Definition Notes from the Specification

- All links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (PCI Express Base Specification, Revision 3.0, Section 4.2.10) is being transmitted during the test.
- Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER 10^{-6} is 46mV.
- The values in Table 4-19 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 ohm trace, followed by a reference receiver package behind a standard PCI Express edge finger. This channel shall be referenced as the 8.0GT/s System Board Test Channel. The s-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up must be removed. Note that the System Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant add-in card.

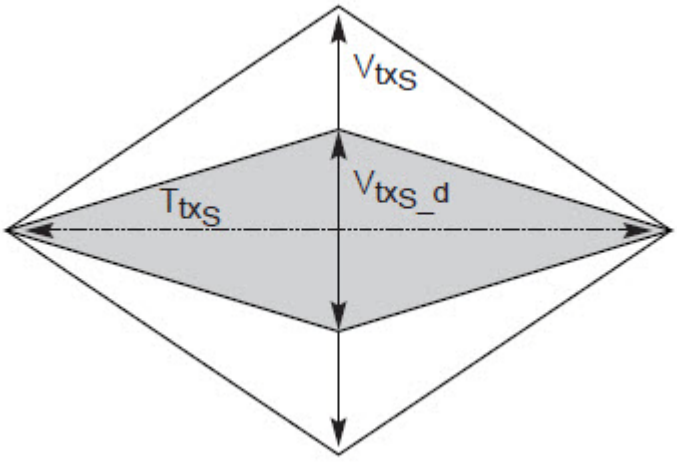


Figure 267 System Board Transmitter Path Composite Compliance Eye Diagram

Understanding the Test Flow

NOTE To execute the test, follow the procedure in "Running System Board Tests" on page 563 and select **Eye-Width with crosstalk/Eye-Width without crosstalk**.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the template test with the following specifications:

Device: PCIE3.0

Data Rate: 8.0GT/s

1 Obtains the eye-width test results from SigTestWrapper.dll file.

2 Compares the measured eye-width values to the compliance limits as specified in the PCI Express CEM Specification, Rev 2.0.

3 Reports the measured eye-width value as the measurement result and verifies that the measured value is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to

view the details. For information about the test results, refer to **Viewing Results** in the online help.

27
Reference Clock Tests, PCI-E 3.0

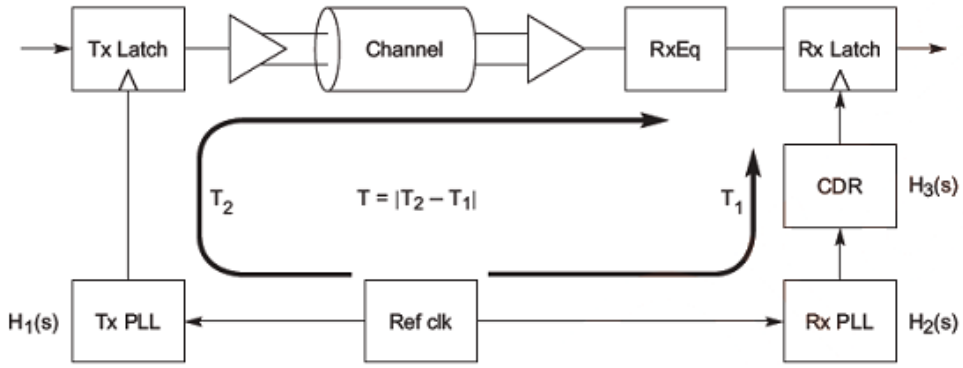
This section provides the Methods of Implementation (MOIs) for Reference Clock tests using a 90000X Series Infiniium oscilloscope, 1169A probes, and the PCI Express Automated Test Application.

Reference Clock Architectures

For PCI-E 3.0, there are two main reference clock architectures — common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1}^2 + \omega_{n1}^2}\right] \quad H_2(s) = \left[\frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2}^2 + \omega_{n2}^2}\right] \quad H_3(s) = \frac{s}{s + \omega_3}$$

$$\left.\begin{aligned} H(s) &= [H_1(s)e^{-sT} - H_2(s)]H_3(s) \text{ or} \\ H'(s) &= [H_2(s)e^{-sT} - H_1(s)]H_3(s) \end{aligned}\right\} \text{Need to compute both}$$

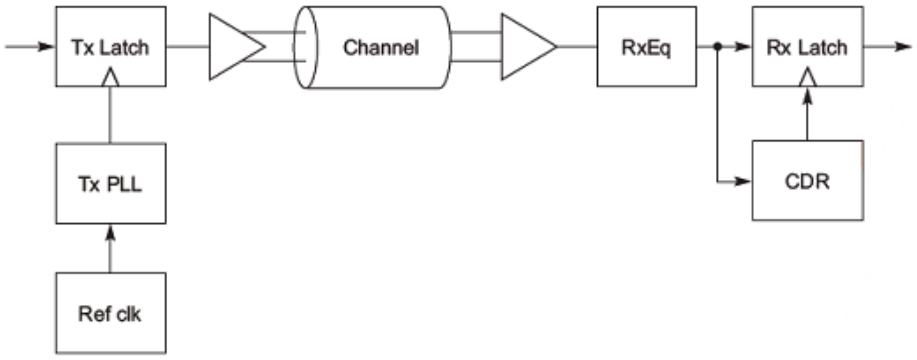
	0.01 dB Peaking	2.0 dB Peaking
$BW_{PLL}(min)$ = 2.0 MHz	ω_{n1} = 0.448 Mrad/s, ζ_1 = 14	ω_{n1} = 6.02 Mrad/s, ζ_1 = 0.73
$BW_{PLL}(max)$ = 4.0 MHz	ω_{n1} = 0.896 Mrad/s, ζ_1 = 14	ω_{n1} = 12.04 Mrad/s, ζ_1 = 0.73

	0.01 dB Peaking	1.0 dB Peaking
$BW_{PLL}(min)$ = 2.0 MHz	ω_{n2} = 0.448 Mrad/s, ζ_2 = 14	ω_{n2} = 4.62 Mrad/s, ζ_2 = 1.15
$BW_{PLL}(max)$ = 5.0 MHz	ω_{n2} = 1.12 Mrad/s, ζ_2 = 14	ω_{n2} = 11.53 Mrad/s, ζ_2 = 1.15

A-0842

Data Clock Architecture

This section describes the data driving architecture.



$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1}^2 + \omega_{n1}^2}\right] \qquad H_3(s) = \left[\frac{2s\zeta_3\omega_{n3} + \omega_{n3}^2}{s^2 + 2s\zeta_3\omega_{n3}^2 + \omega_{n3}^2}\right]$$

$$H(s) = H_1(s)[1 - H_3(s)]$$

	0.01 dB Peaking	2.0 dB Peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1} = 0.448 Mrad/s, ζ_1 = 14	ω_{n1} = 6.02 Mrad/s, ζ_1 = 0.73
BW_{PLL}(max) = 4.0 MHz	ω_{n1} = 0.896 Mrad/s, ζ_1 = 14	ω_{n1} = 12.04 Mrad/s, ζ_1 = 0.73

	0.01 dB Peaking	1.0 dB Peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n2} = 0.448 Mrad/s, ζ_2 = 14	ω_{n2} = 4.62 Mrad/s, ζ_2 = 1.15
BW_{PLL}(max) = 5.0 MHz	ω_{n2} = 1.12 Mrad/s, ζ_2 = 14	ω_{n2} = 11.53 Mrad/s, ζ_2 = 1.15

	0.5 dB Peaking	2.0 dB Peaking
BW_{CDR}(min) = 10 MHz	ω_{n3} = 16.57 Mrad/s, ζ_3 = 1.75	ω_{n3} = 33.8 Mrad/s, ζ_3 = 0.73

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Probing the Link for Reference Clock Compliance

Reference Clock tests are done by connecting the device under test to a test fixture and probing the SMA connectors on the test fixture. To probe the reference clock link, you can:

- Use two 50-ohm coax cables with SMA male connectors, two precision 3.5 mm BNC to SMA male adapters (included with the oscilloscope), and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.

- Use two differential probe heads with two 1169A probe amplifiers (with the negative lead grounded for single-ended measurements) and the channel 1 and channel 3 inputs of an oscilloscope that has 20 GS/s sample rate available on two channels.
- Use one differential probe head with the 1169A probe amplifier and the channel 2 input of an oscilloscope that has 20 GS/s sample rate available on that channel.

When the link is broken and terminated into a 50 ohm load (by the test load), the Compliance Pattern defined in section 4.2.8 (Card Electromechanical Specification) will be transmitted.

Table 186 Probing Options for Reference Clock Testing

	Probing Configurations			Captured Waveforms		Oscilloscope Specifications	
	Probing Method	**Break Serial Link**	**Channels Used**	**Differential Mode**	**Common Mode**	**System Band Width**	**Rise* Time (20-80)**
DUT Connection	Single-Ended SMA (2 x 50-Ohm SMA Cables)	Y	2	Pseudo	Yes	6 GHz	70 ps
	Single-Ended (2 x 1169A w/ Differential Probe Heads)	Y/N	2	Pseudo	Yes	6 GHz	70 ps
	Differential (1 x 1169A w/ Differential Probe Head)	Y/N	1	True	No	6 GHz	70 ps

*Typical

Single-Ended SMA Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 – Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

This probing technique requires breaking the link and terminating into the 50 ohm/side termination into the oscilloscope. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Channel-to-Channel deskew is required using this technique because two channels are used.

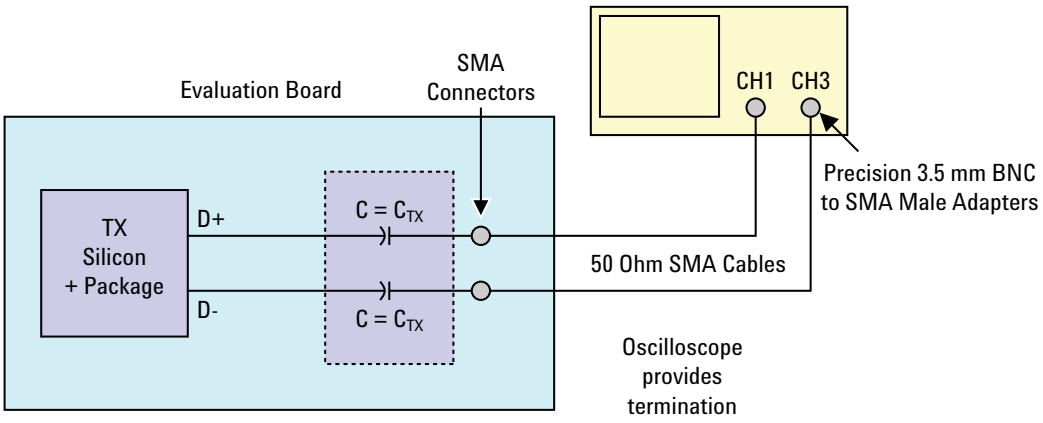

Figure 268 Single-Ended SMA Probing using Channel 1 and Channel 3

Single-Ended Probing

The differential signal is created by the PCI Express Automated Test Application software from the math waveform Source 1 – Source 2. The Sources can be either channels 1 and 3 or channels 2 and 4. The Common mode measurements are also available in this configuration from the common mode waveform (Source 1 + Source 2)/2.

Make sure to probe equal distances from the reference clock, as close as possible to the reference clock. Place single-ended grounds as close to the signal line's reference ground as possible. Channel-to-Channel deskew is required using this probing technique because two channels are used.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, "InfiniiMax Probing Options," starting on page 632.

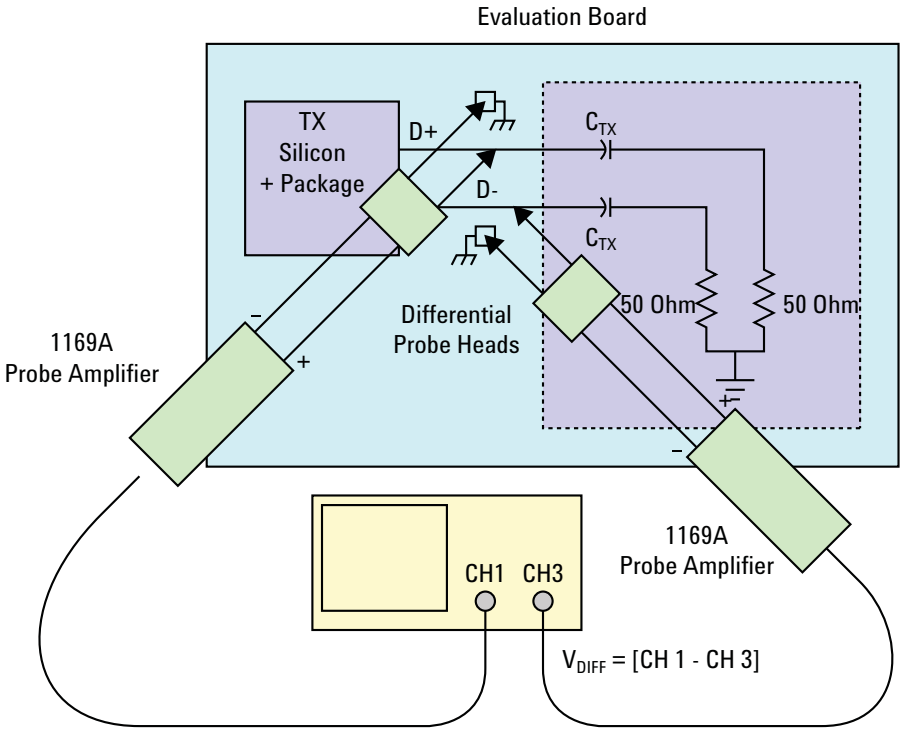

Figure 269 Single-Ended Probing

Differential Probing

The differential signal is measured directly by the differential probe head.

Make sure to probe equal distances from the reference clock, as close as possible to the reference clock.

This probing technique requires breaking the link and terminating into 50 ohm/side. While in this mode, the PCI Express SerDes will transmit the 640 bit Jitter test pattern designed to maximize data dependent jitter.

Only one channel of the oscilloscope is used.

For more information on the 1169A probe amplifier and differential probe heads, see Appendix B, “InfiniiMax Probing Options,” starting on page 632.

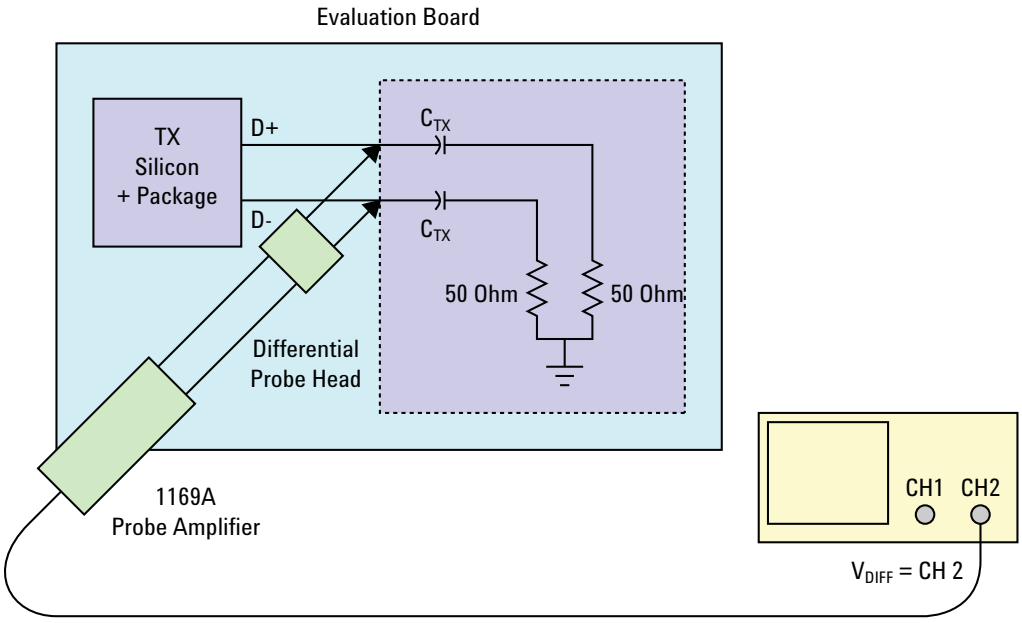

Figure 270 Differential Probing

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in Figure 4-25 of the Card Electromechanical Specification.

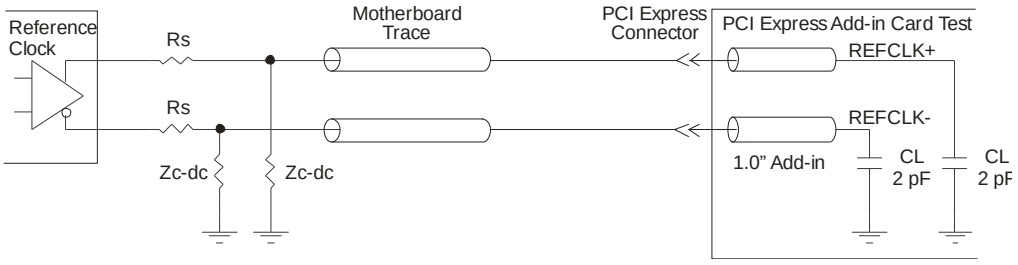

Figure 271 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Automated Test Application" on page 26. Then, when selecting tests, navigate to "Reference Clock Tests" in the "PCIE 3.0 Tests" group.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

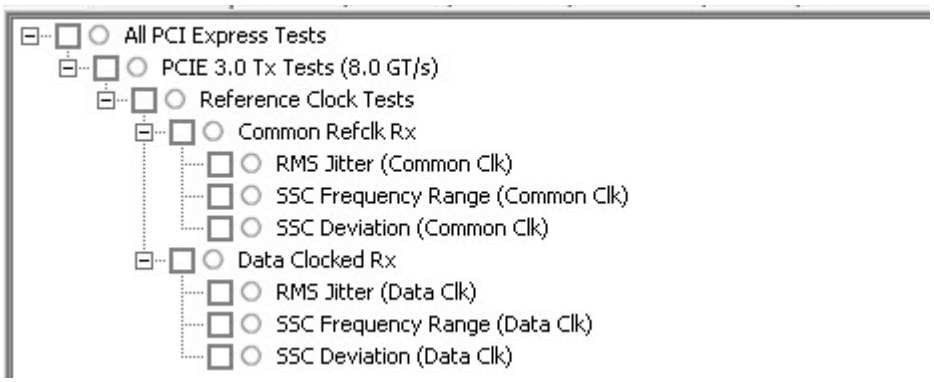

Figure 272 Selecting Reference Clock Tests when SSC is Selected

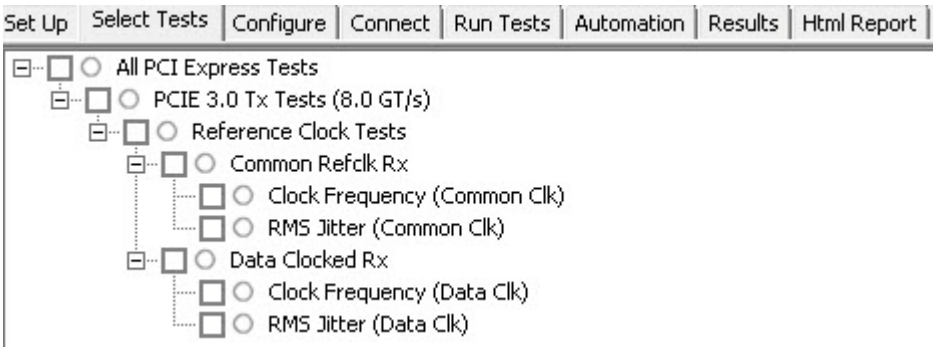

Figure 273 Selecting Reference Clock Tests when Clean Clock is Selected

Clock Frequency (Common Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in Table 4-34 of the PCIE Base Specification, rev. 3.0

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.8.2, Table 4-34 is used as reference to check the compliance of the DUT.

Table 187 Clock Frequency Test Details

Symbol	Description	Min	Max
F_{REFCLK}	Refclk frequency	99.97 MHz	100.03 MHz

Test Definition Notes from the Specification

Before application of SSC.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 588 and select **Clock Frequency (Common Clk)**.

1 Gets the reference clock signal.

2 Verifies that the signal period is ~100MHz.

3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

4 Sets the time scale to 5 ns.

5 Fits and displays all sample data on the screen.

6 Enables jitter analysis so that measurements are made on all edges.

7 Measures the clock frequency.

8 Reports the mean frequency.

9 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

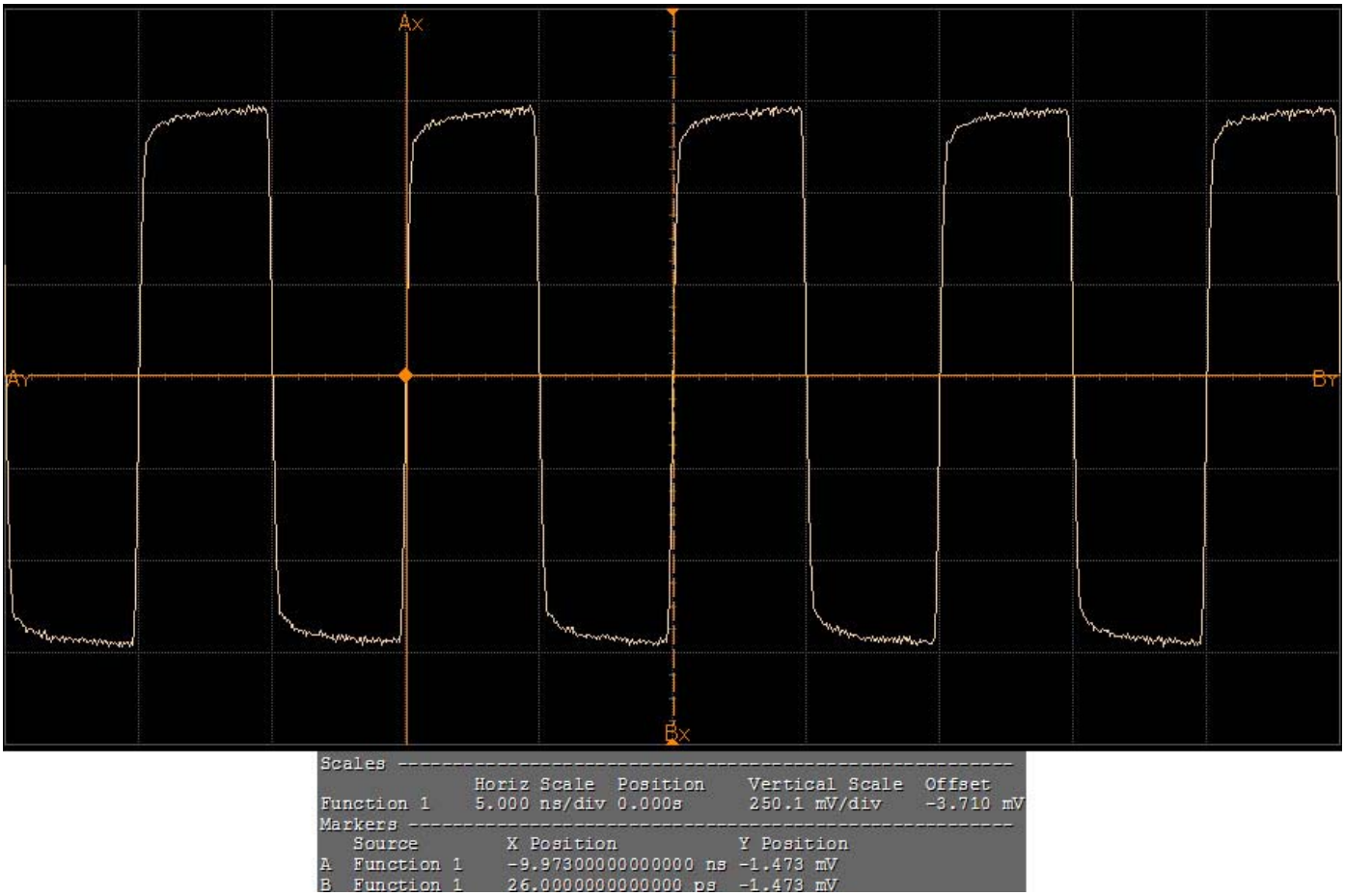

Figure 274 Reference Clock Frequency (Common Clock) Test

RMS Jitter (Common Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in Table 4-34 of the PCIE Base Specification, rev. 3.0

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.8.2, Table 4-34 is used as reference to check the compliance of the DUT.

Table 188 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	1.0 ps RMS

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 588 and select **RMS Jitter (Common Clk)**.

1. Gets the reference clock signal.
2. Verifies that the signal period is ~100MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5. Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9. Stitches each acquired acquisition to make a continuous TIE data.
10. Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
    a. Converts time domain TIE data to frequency domain.
    b. Applies the PLL filter using parameters for common clocked architecture.
    c. Converts back the frequency domain TIE data to time domains.
    d. Computes the filtered peak-peak jitters and RMS jitter.
11. Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

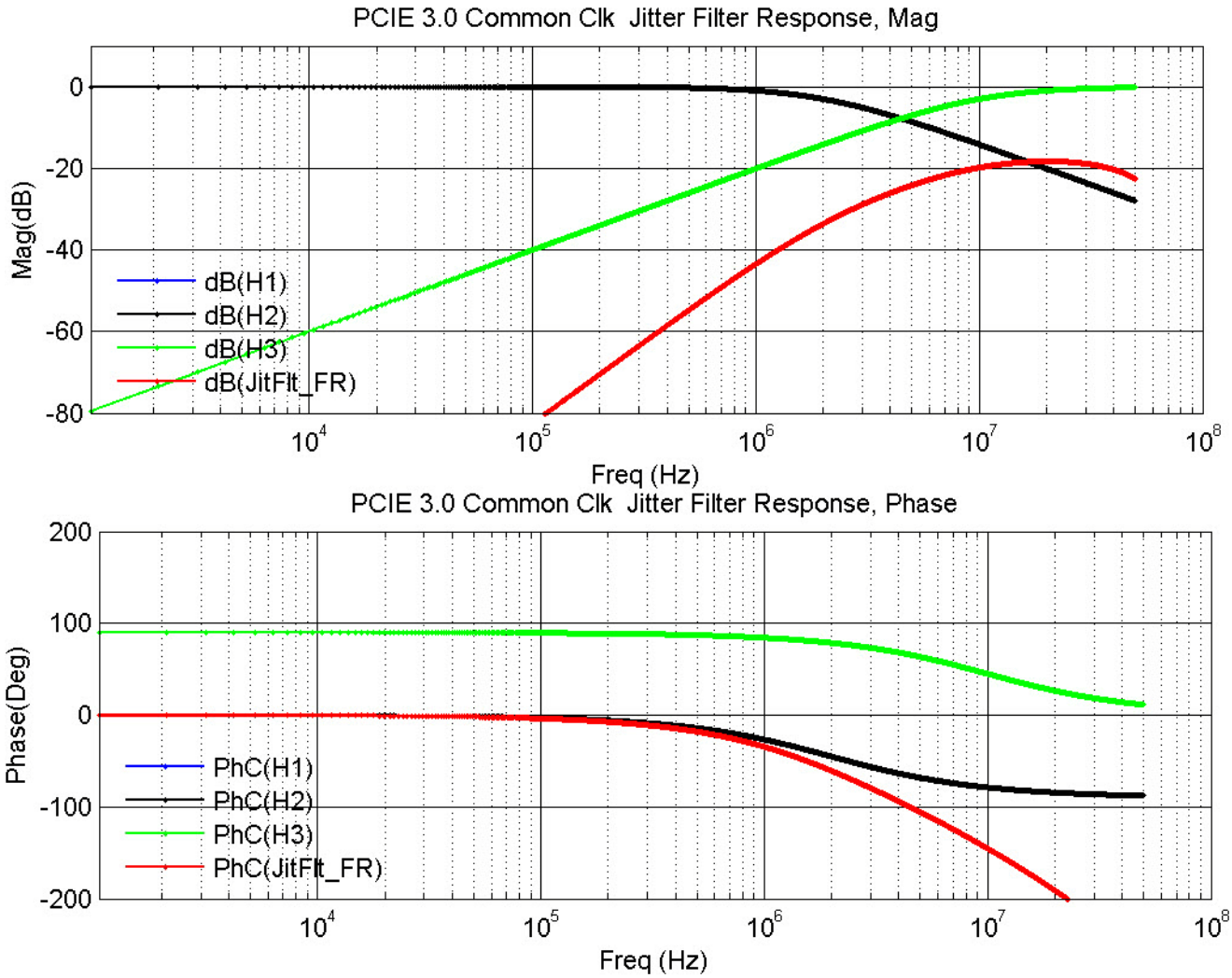

Figure 275 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

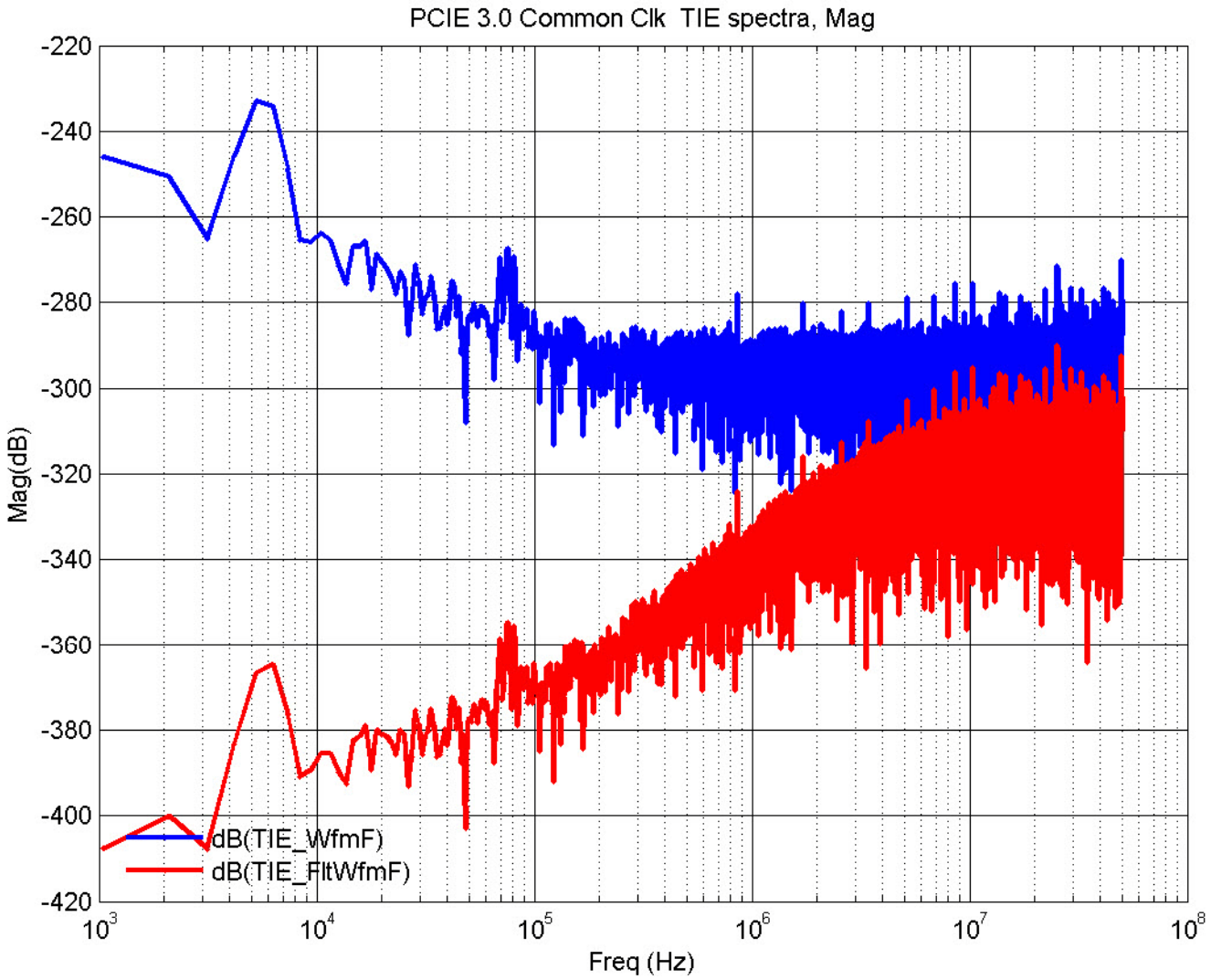

Figure 276 Reference Image for Common Clock TIE Spectra RMS Jitter Test

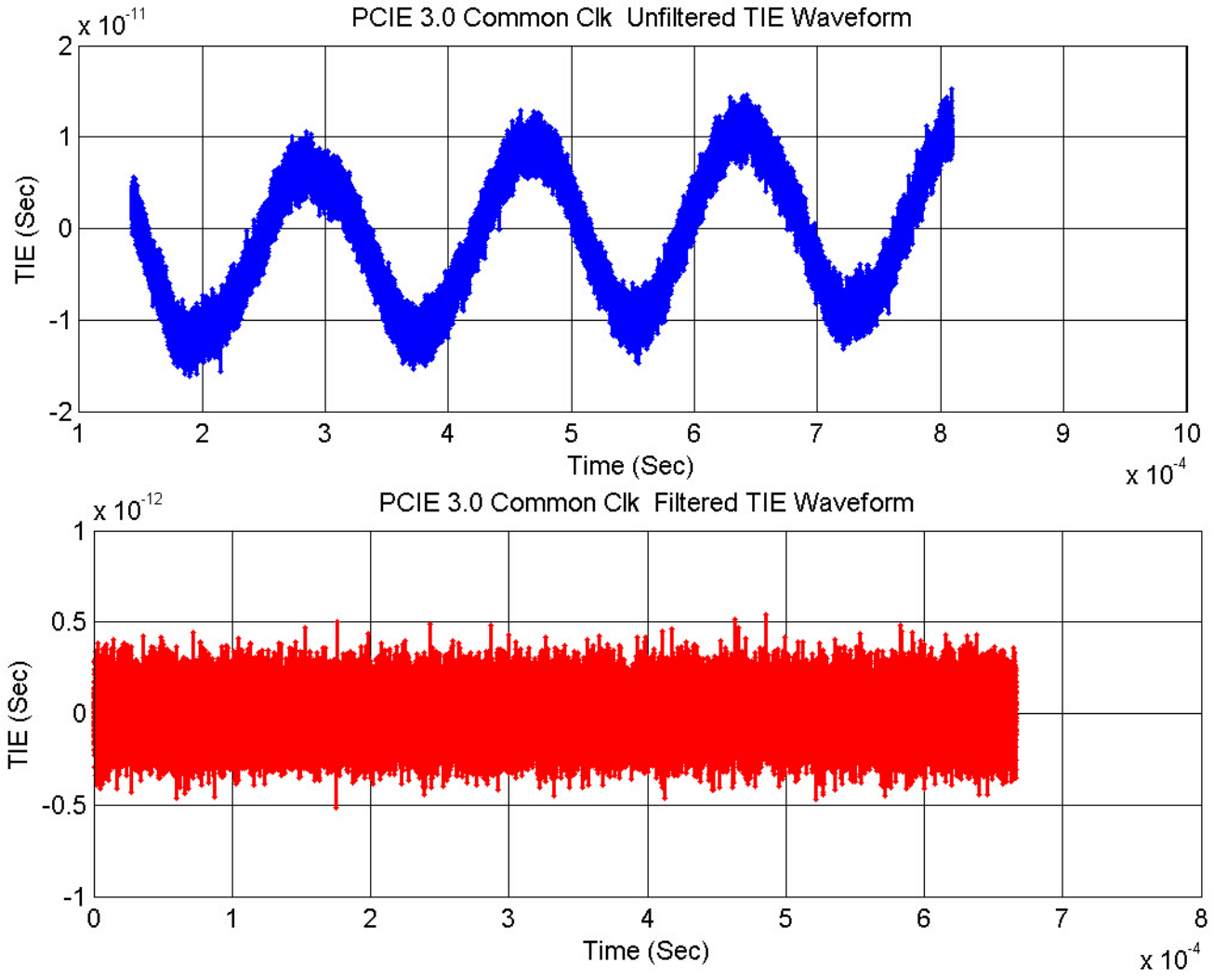

Figure 277 Reference Image for TIE Waveform RMS Jitter Test

SSC Frequency Range (Common Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in Table 4-34 of the PCIE Base Specification, rev. 3.0

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.8.2, Table 4-34 is used as reference to check the compliance of the DUT.

Table 189 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 KHz	33 KHz

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 588 and select **SSC Frequency Range (Common Clk)**.

1. Gets the reference clock signal.
2. Verifies that the signal period is ~ 100MHz.
3. Sets up labels and grid display settings on the oscilloscope.
4. Sets the scale and offset of the input channels to their optimum values.
5. Configures the **Sample Rate** to 20GSa/s and **Memory Depth** to 10 Mpts using **Acquisition Setup**.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Measures the frequency of the jitter TREND on FUNC3. This is the frequency of the SSC.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Deviation (Common Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in Table 4-34 of the PCIE Base Specification, rev. 3.0

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.8.2, Table 4-34 is used as reference to check the compliance of the DUT.

Table 190 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	+0.0/–0.5%

Test Definition Notes from the Specification

It is sufficient to define SSC deviation only without specifying anything about the shape of the modulation envelope. Envelopes with very large df/dt will fail the $T_{REFCLK\text{-}RMS\text{-}CC}$ parameter.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 588 and select **SSC Deviation (Common Clk)**.

1. Gets the reference clock signal.
2. Verifies that the signal period is ~ 100MHz.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures the **Sample Rate** to 20GSa/s and **Memory Depth** to 10 Mpts using **Acquisition Setup**.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Uses marker to indicate upper and lower limit (Trend data of Period measurements).
9. Measures Period_max, Period_min and Period_average.
10. Computes SSC deviation Max(%) = ((1/Period_min) - 100MHz) / 100MHz * 100

11 Computes SSC deviation Min(%) = ((1/Period_max) - 100MHz) / 100MHz * 100

12 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Clock Frequency (Data Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in Table 4-35 of the PCIE Base Specification, rev. 3.0

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.8.3, Table 4-35 is used as reference to check the compliance of the DUT.

Table 191 Clock Frequency Test Details

Symbol	Description	Min	Max
F_{REFCLK}	Refclk frequency	99.97 MHz	100.03 MHz

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 588 and select **Clock Frequency (Data Clk)**.

1 Gets the reference clock signal.

2 Verifies that the signal period is ~ 100MHz.

3 Sets up labels and grid display settings on the oscilloscope.

4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

5 Sets time scale to 5ns.

6 Fits and displays all sample data on the screen.

7 Enables jitter analysis so that measurements are made on all edges.

8 Measures the clock frequency.

9 Reports the mean frequency.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

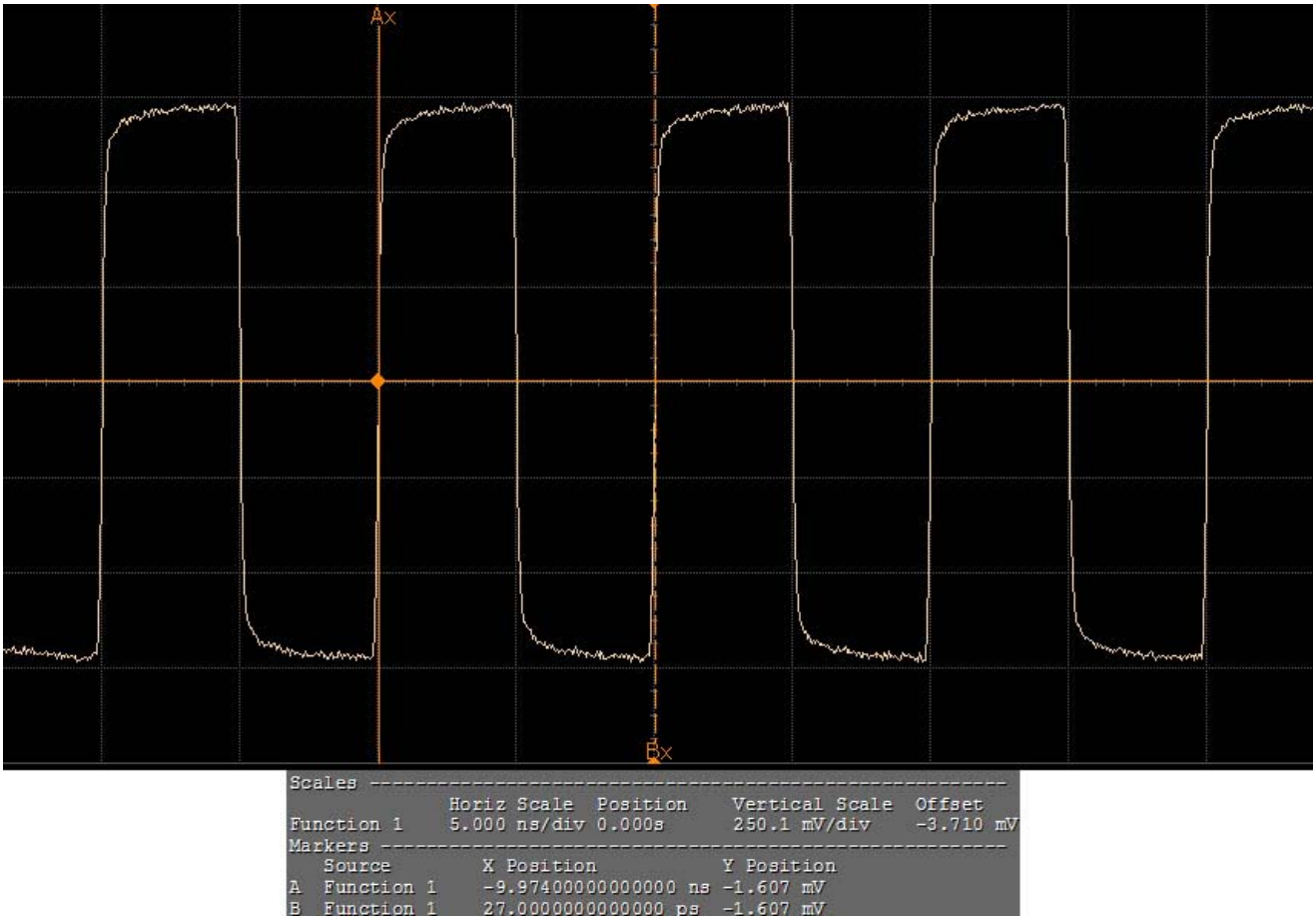

Figure 278 Reference Image for Clock Frequency (Data Clock) Test

RMS Jitter (Data Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in Table 4-35 of the PCIE Base Specification, rev. 3.0

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.8.3, Table 4-35 is used as reference to check the compliance of the DUT.

Table 192 RMS Jitter Test Details

Symbol	Parameter	Max
$T_{REFCLK-RMS-DC}$	RMS Refclk jitter for data clocked architecture	1.0 ps RMS

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 588 and select **RMS Jitter (Data Clk)**.

1. Gets the reference clock signal.
2. Verifies that the signal period is ~ 100MHz.
3. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4. Configures the **Sample Rate** to 20GSa/s and **Memory Depth** to 10 Mpts using **Acquisition Setup**.
5. Configures **Memory Depth** to **50.0000Mpts** as **Manual** using **Acquisition Setup**. If the desired option is not available, then it configures it to the highest available memory depth.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200

points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

9 Stitches each acquired acquisition to make a continuous TIE data.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies the PLL filter using parameters for common clocked architecture.

   c Converts back the frequency domain TIE data to time domains.

   d Computes the filtered peak-peak jitters and RMS jitter.

11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

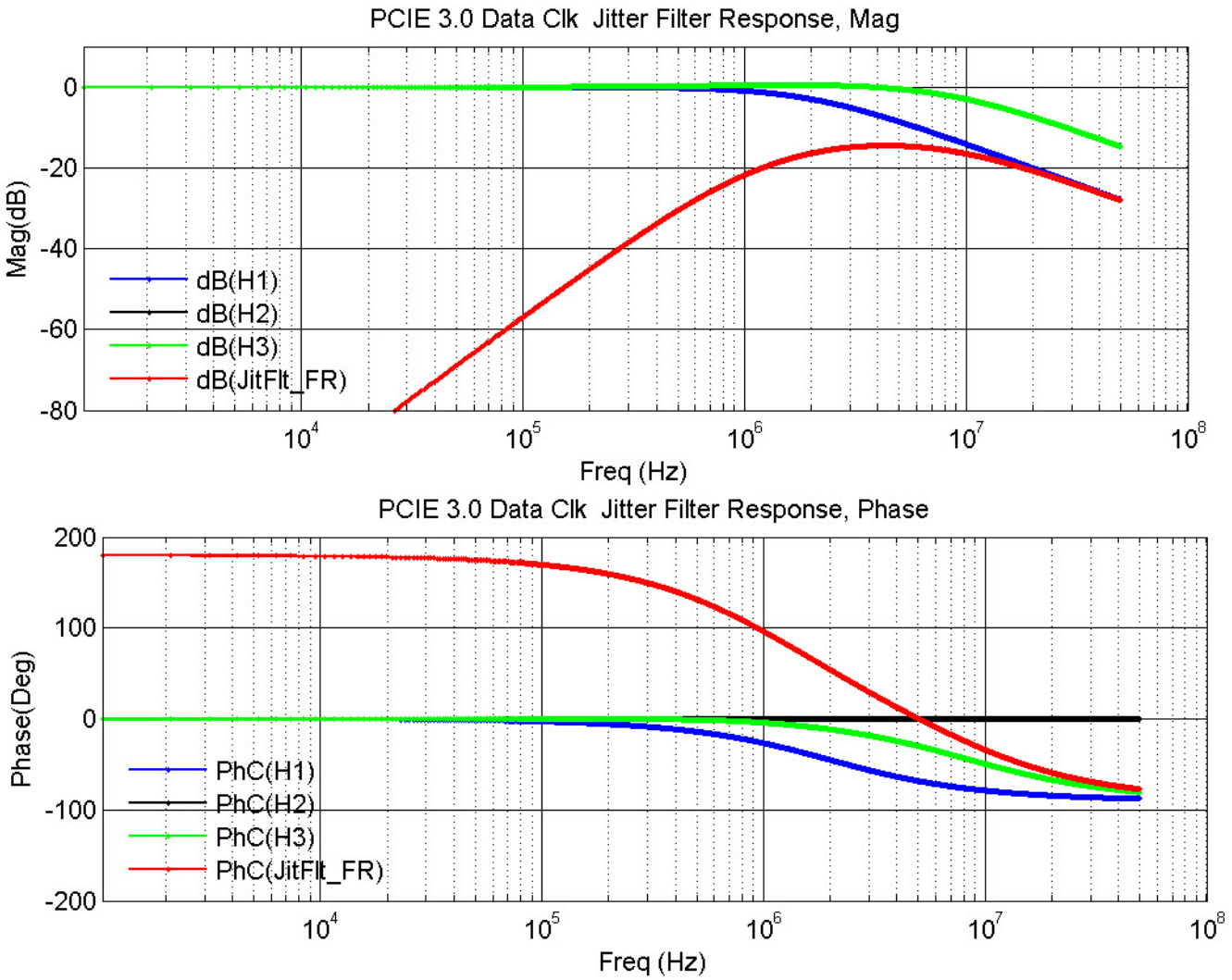

Figure 279 Reference Image for Jitter Filter Response (Data Clock) RMS Jitter Test

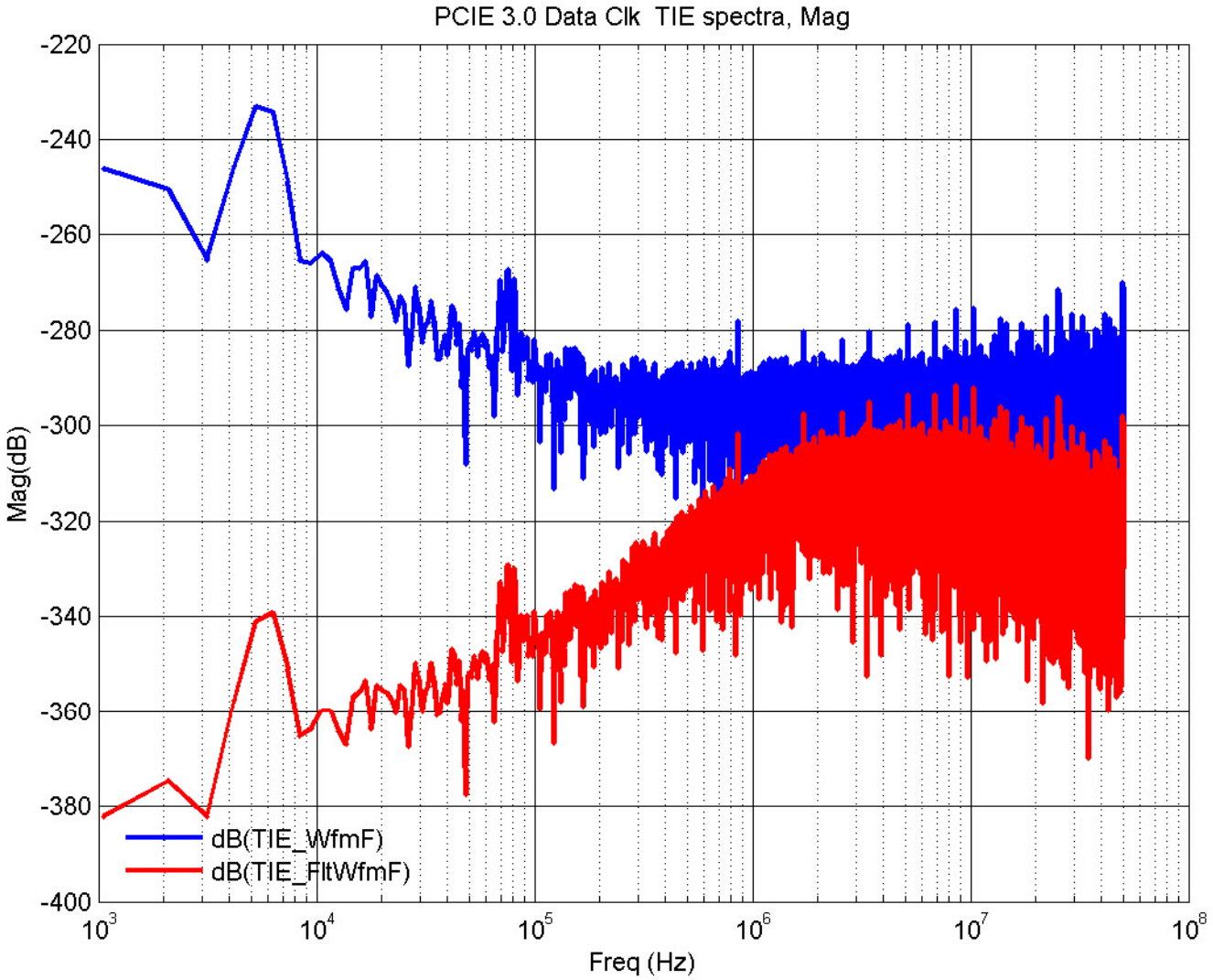

Figure 280 Reference Image for Data Clock TIE Spectra RMS Jitter Test

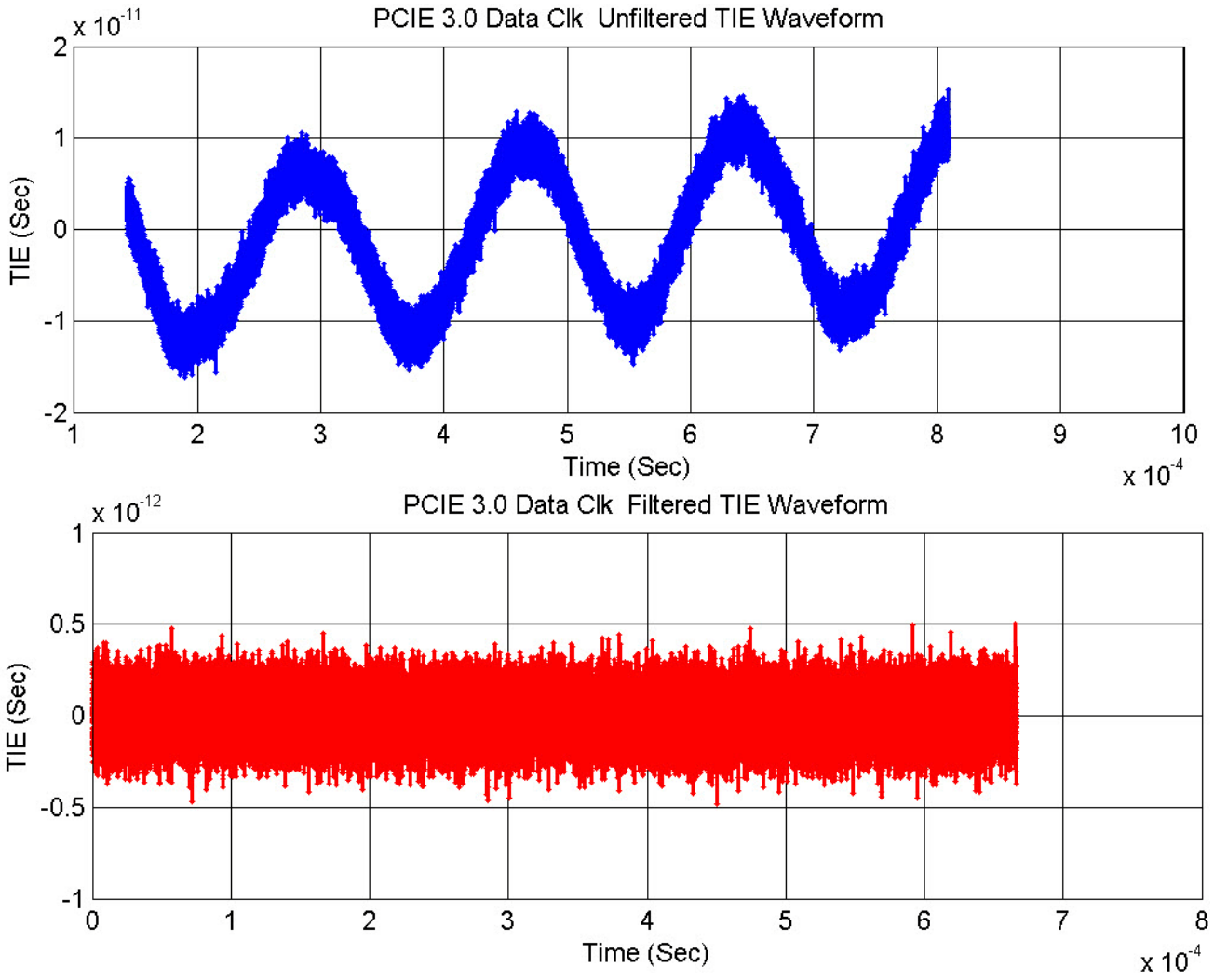

Figure 281 Reference Image for TIE Waveform RMS Jitter Test

SSC Frequency Range (Data Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in Table 4-35 of the PCIE Base Specification, rev. 3.0

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.8.3, Table 4-35 is used as reference to check the compliance of the DUT.

Table 193 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 KHz	33 kHz

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 588 and select **SSC Frequency Range (Data Clk)**.

1. Gets the reference clock signal.
2. Verifies that the signal period is ~ 100MHz.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures the **Sample Rate** to 20GSa/s and **Memory Depth** to 10 Mpts using **Acquisition Setup**.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Measures the frequency of the jitter TREND on FUNC3. This is the frequency of the SSC.
9. Reports the mean frequency.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

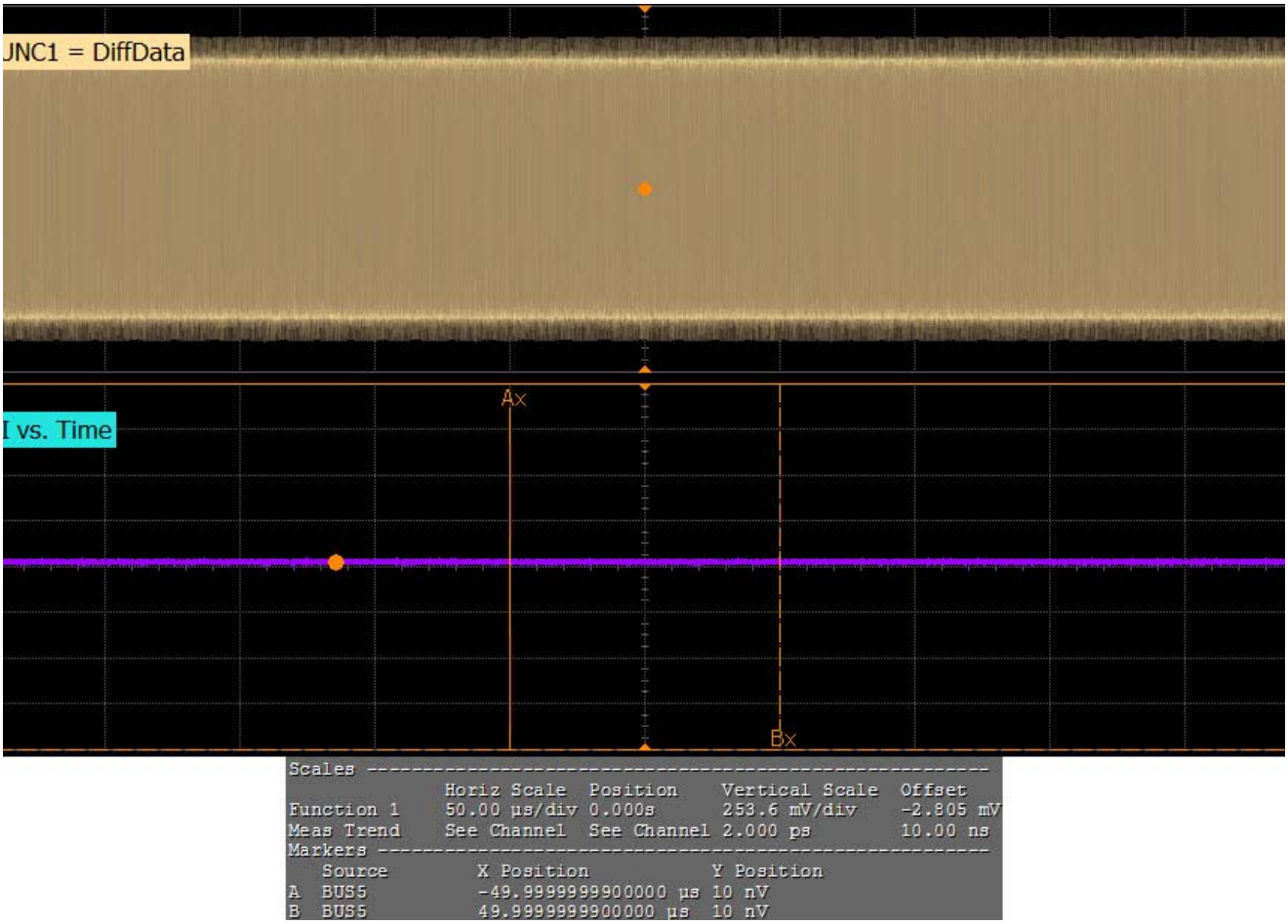

Figure 282 Reference Image for SSC Frequency Range (Data Clock) Test

SSC Deviation (Data Clk) Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in Table 4-35 of the PCIE Base Specification, rev. 3.0

Test Reference

PCI Express Base Specification, Rev 3.0, Section 4.3.8.3, Table 4-35 is used as reference to check the compliance of the DUT.

Table 194 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	+0.0/–0.5 (max)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 3.0. To execute the test, follow the procedure in "Running Reference Clock Tests" on page 588 and select **SSC Deviation (Common Clk)**.

1. Gets the reference clock signal.
2. Verifies that the signal period is ~ 100MHz.
3. Sets up labels and grid display settings on the oscilloscope.
4. Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5. Configures the **Sample Rate** to 20GSa/s and **Memory Depth** to 10 Mpts using **Acquisition Setup**.
6. Fits and displays all sample data on the screen.
7. Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8. Uses marker to indicate upper and lower limit on FUNC3 (Trend data of Period measurements)
9. Measures Period_max, Period_min and Period_average.
10. Computes SSC deviation Max(%) = ((1/Period_min) - 100MHz) / 100MHz * 100
11. Computes SSC deviation Min(%) = ((1/Period_max) - 100MHz) / 100MHz * 100
12. Compares the SSC deviation Max and SSC deviation Min and reports worst case value as active result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Part VIII
Appendices

Agilent Technologies

A
Calibrating the Digital Storage Oscilloscope

This appendix describes the Agilent digital storage oscilloscope calibration procedures.

Required Equipment for Calibration

To calibrate the oscilloscope in preparation for running the PCI Express automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, qty = 2, (provided with the Agilent Infiniium oscilloscope).
- Calibration cable.
- BNC shorting cap.

Figure 283 below shows a drawing of the above connector items.

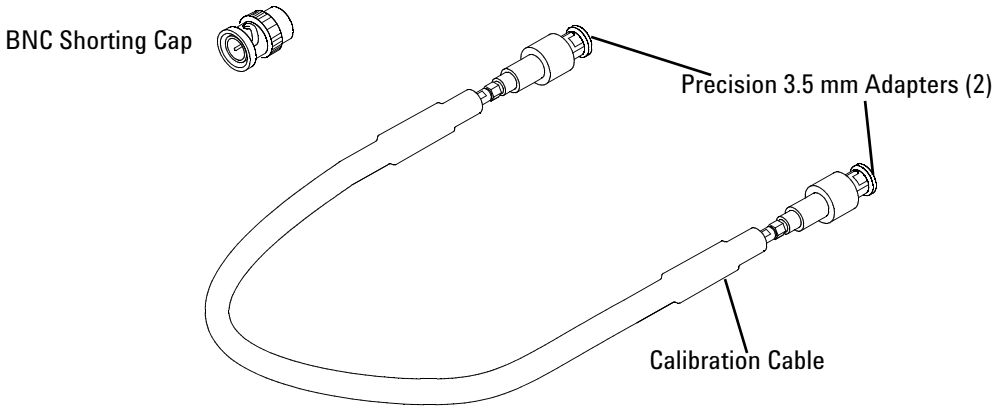

Figure 283 Accessories Provided with the Agilent Oscilloscope

- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG316/U or similar, qty = 2, matched length.
- SMA T-adapter.
- BNC to SMA male adapter, qty = 1.

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.

   b If SigTest is being used on the oscilloscope, then connect a second monitor to the VGA connector located near the LAN port, on the rear of the oscilloscope.

   c Plug in the power cord.

   d Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.

   e Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

   a Locate the BNC shorting cap.

   b Locate the calibration cable.

   c Locate the two Agilent precision SMA/BNC adapters.

   d Attach one SMA adapter to one end of the calibration cable - hand tighten snugly.

   e Attach the other SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 284 below, perform the following steps:

   a Click on the Utilities>Calibration menu to open the Calibration window.

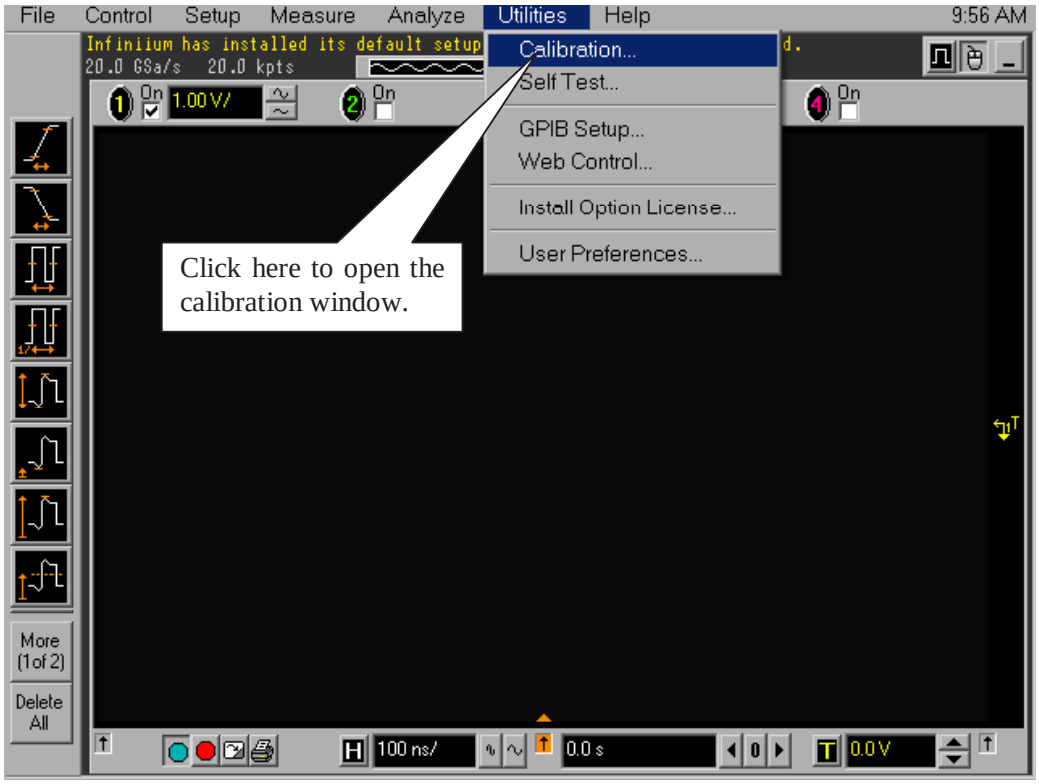

Figure 284 Accessing the Calibration Menu.

4 Referring to Figure 285 below, perform the following steps to start the calibration:

   a Uncheck the Cal Memory Protect checkbox.

   b Click the Start button to begin the calibration.

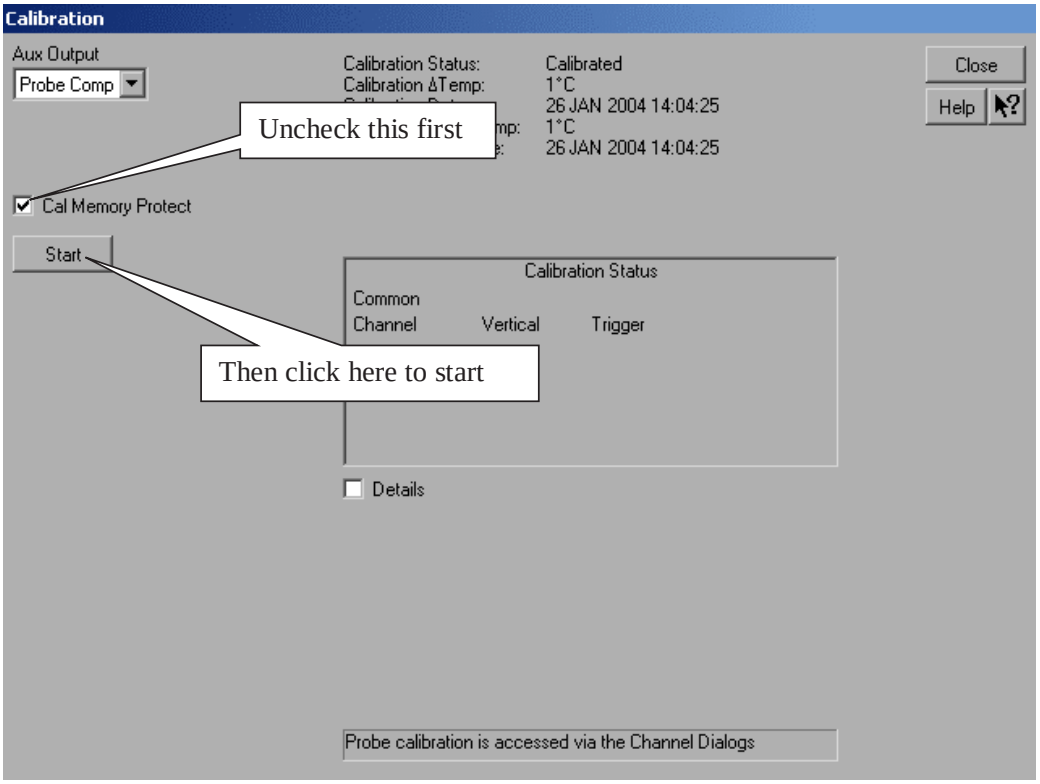

Figure 285 Oscilloscope Calibration Menu.

5 Follow the on-screen instructions:

a You will be prompted to disconnect everything from all the inputs, click the OK button.

b Then, you will be prompted to connect BNC shorting cap to a specified input. Install the BNC shorting cap by pressing it on the specified input BNC, and turning right. Click the OK button after moving the BNC cap to each specified channel.

c Then you will be prompted to connect the calibration cable with SMA adapters between the Aux Out and a specified input, as shown in the example in Figure 286 below. Install the SMA adapter by pressing it on input BNC, and hand tightening the outer ring turning right. Click the OK button after connecting the cable as prompted.

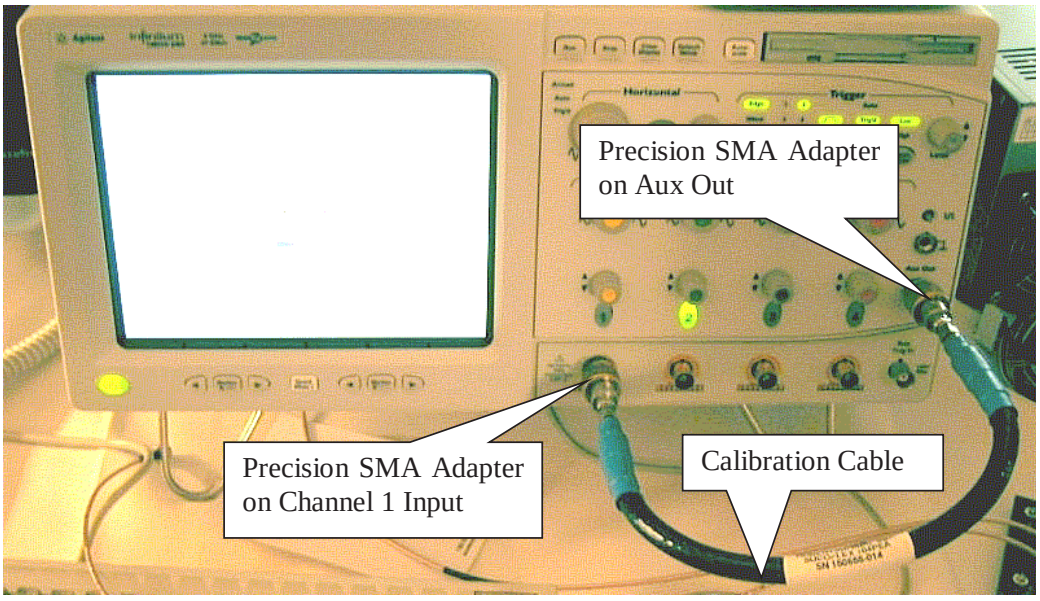

Figure 286 Calibration Cable Connection Example.

d Early during the calibration of channel 1, you will be prompted to perform a Time Scale Calibration, as shown in Figure 287 below.

e Click on the Default button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

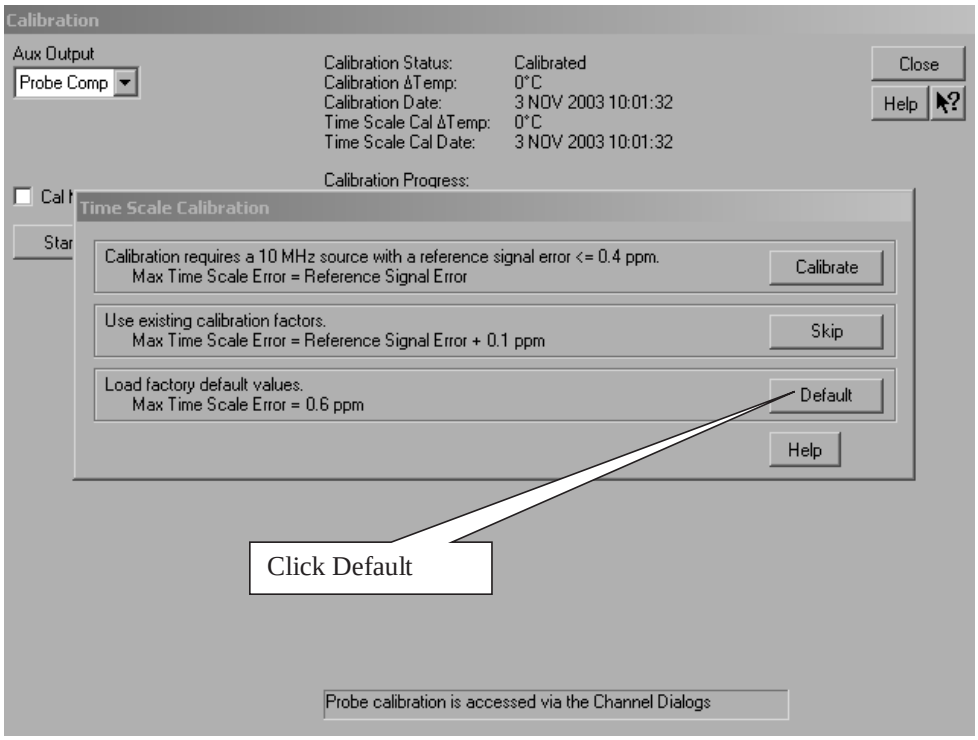

Figure 287 Time Scale Calibration Menu.

6 Referring to Figure 288 below, perform the following steps:

- **a** Confirm that the Vertical and Trigger Calibration Status for all Channels passed.
- **b** Click the Close button to close the calibration window.
- **c** The internal calibration is completed.
- **d** Read NOTE below.

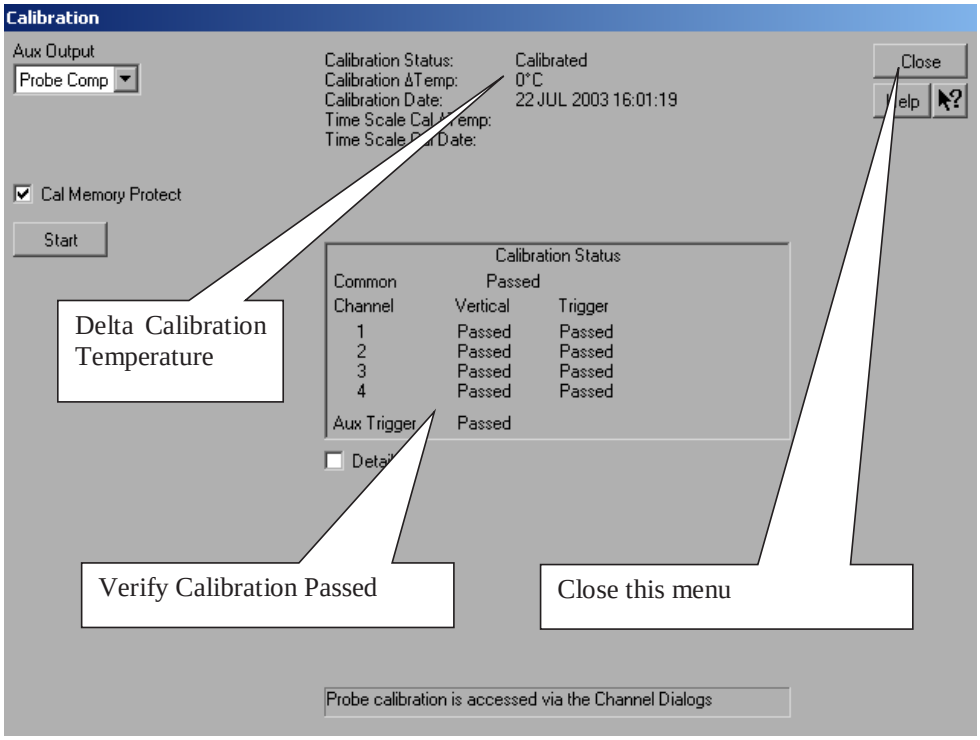

Figure 288 Calibration Status Screen.

NOTE

These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Cable and Probe Calibration

Perform a 50-ohm direct-coupled input calibration for the SMA interface of channel 1 and channel 3. This calibration compensates for gain, offset, and skew errors in cables and probes. Perform the following steps.

1 Referring to the Figure 289 below, perform the following steps:

- **a** Locate and connect one of the Agilent precision SMA adapters to the Channel 1 oscilloscope input.
- **b** Locate and connect the other Agilent precision SMA adapter to the Channel 3 oscilloscope input.
- **c** Locate and connect one end of one of the RG-316 cables to the SMA adapter on Channel 1.
- **d** Locate and connect one end of the other RG-316 cable to the SMA adapter on Channel 3.
- **e** Locate and connect the non-Agilent SMA/BNC adapter to the Aux Out BNC on the oscilloscope.
- **f** Connect the other end of the cable attached to Channel 1 to the SMA adapter on the Aux Out.

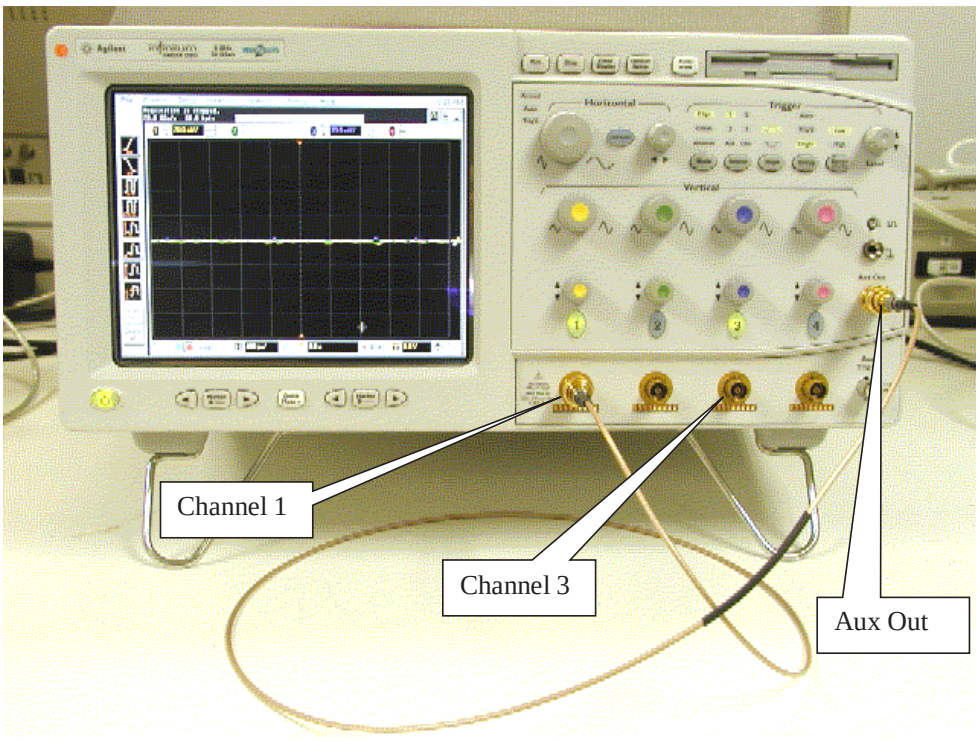

Figure 289 Vertical Input Calibration Connections (Cable on Channel 3 not shown).

2 Referring to Figure 290 below, perform the following steps:

a Click on the Setup>Channel 1 menu to open the Channel Setup window.

b Click the Probes button in the Channel Setup window, to open the Probe Setup window.

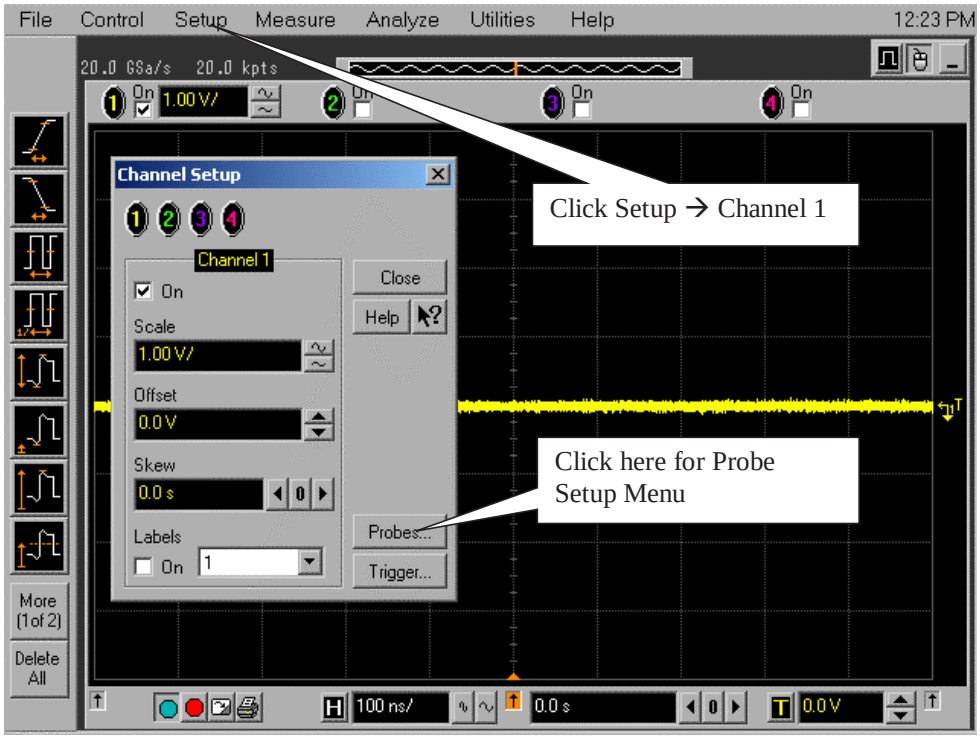

Figure 290 Channel Setup Window.

3 Referring to Figure 291 below, perform the following steps:

a Click the Configure Probing System button, and then click on User Defined Probes.

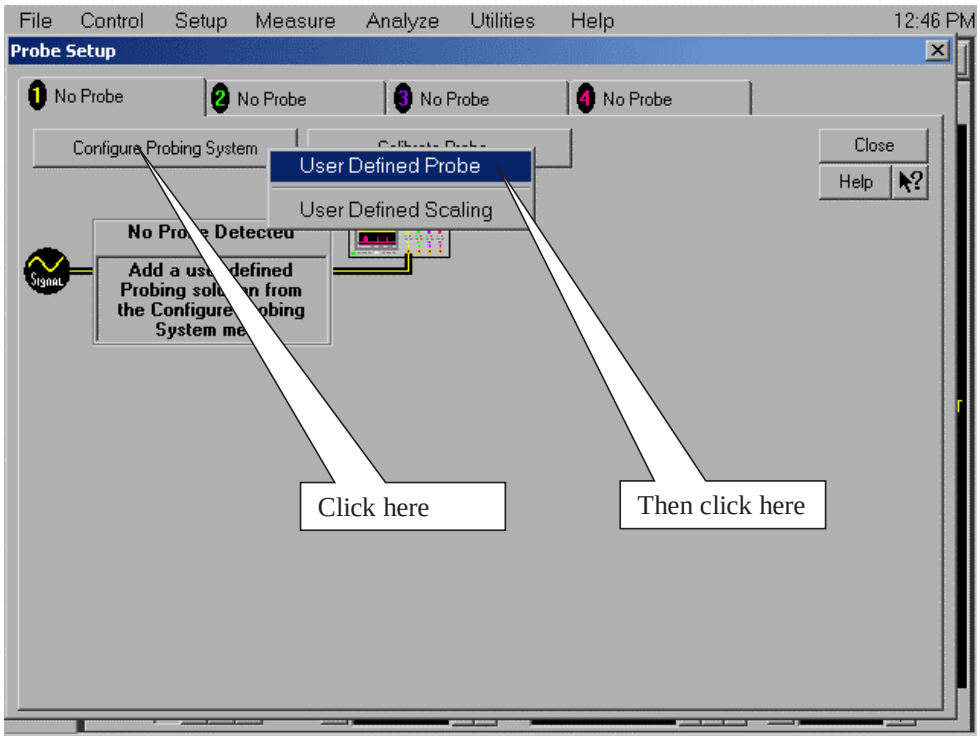

Figure 291 Probe Setup Window.

4 Referring to Figure 292 below, perform the following steps:

a Click on the Calibrate Probe button to open the Probe Calibration window.

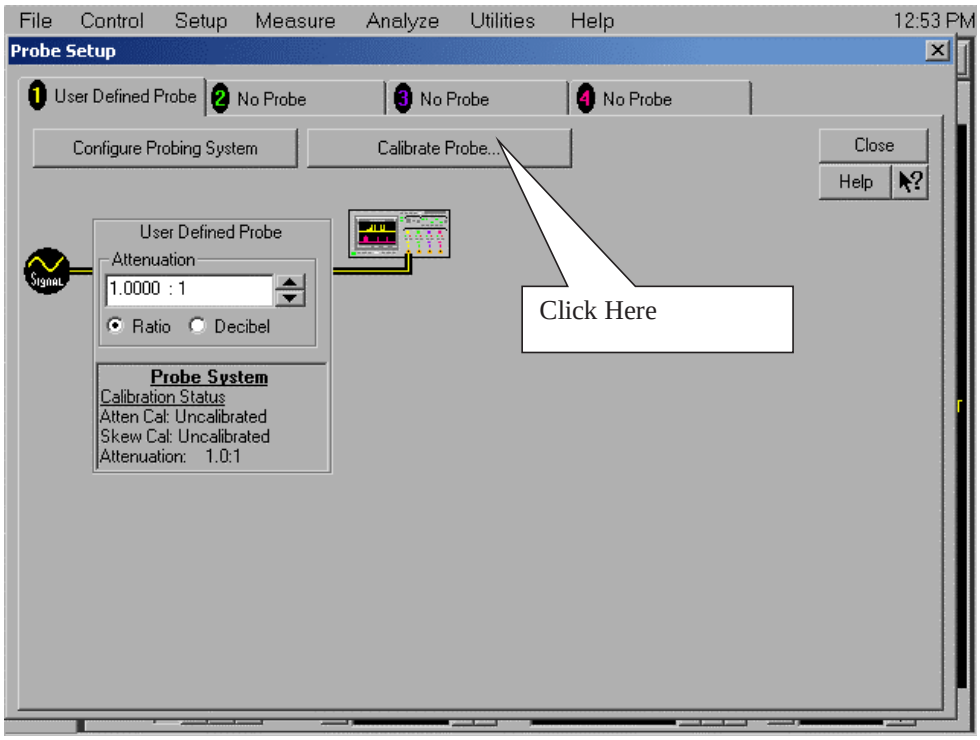

Figure 292 User Defined Probe Window.

5 Referring to Figure 293 below, perform the following steps:

a Select the Calibrated Atten/Offset Radio Button

b Click the Start Atten/Offset Calibration Button to open the Calibration window.

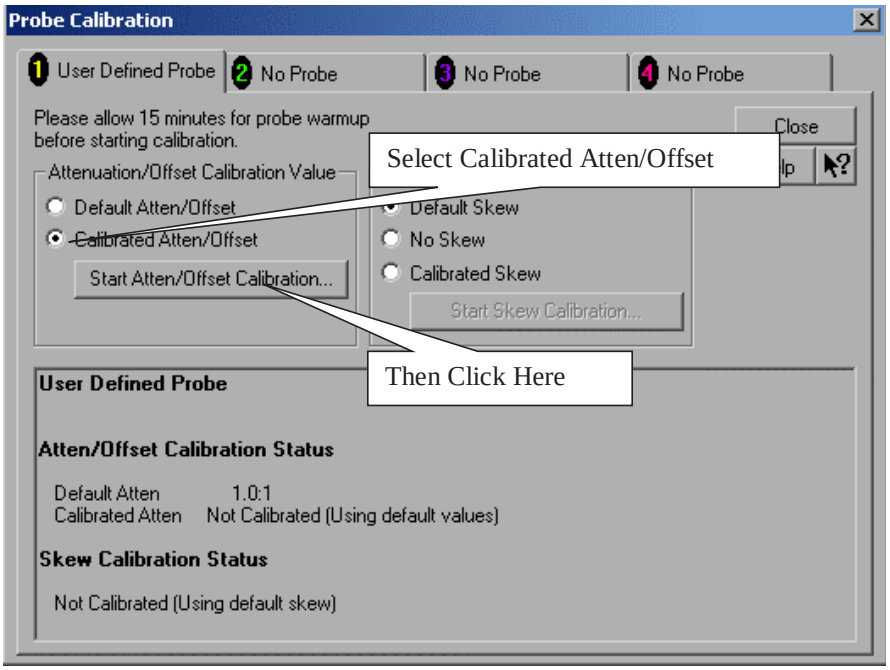

Figure 293 Probe Calibration Window.

6 Referring to Figure 294 shown below, perform the following steps:

- **a** Ignore the instructions shown in the dialog box.
- **b** Click the OK button on the Calibration window.
- **c** The calibration should complete in about 10 seconds.

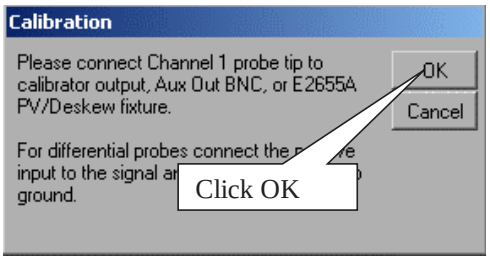

Figure 294 Calibration Window.

7 Referring to Figure 295 below, perform the following steps:

a Click OK to close the Probe Calibration Done window.

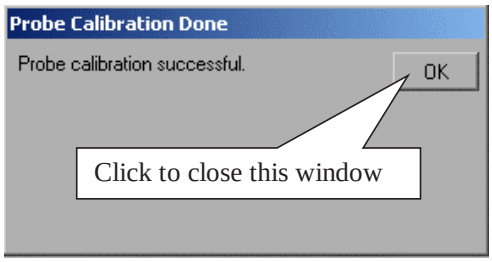

Figure 295 Probe Calibration Done Window.

8 Referring to Figure 296 below, perform the following steps:

a Select the Calibrated Skew Radio button in the Probe Calibration window

b Click the Start Skew Calibration button

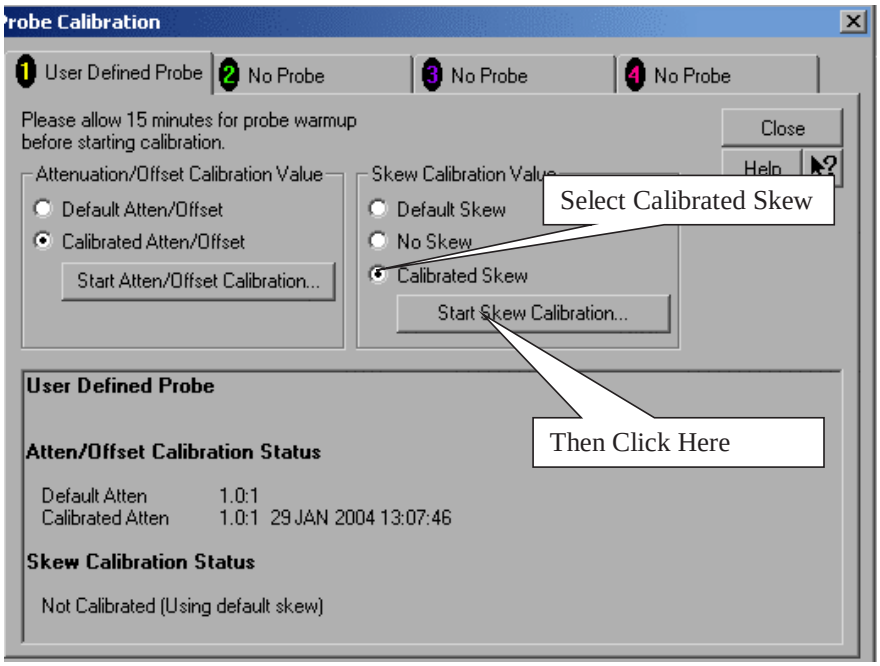

Figure 296 Probe Calibration Window.

9 Referring to Figure 297 shown below, perform the following steps:

a Ignore the instructions shown in the dialog box.

b Click the OK button on the Calibration window.

c The calibration should complete in about 10 seconds.

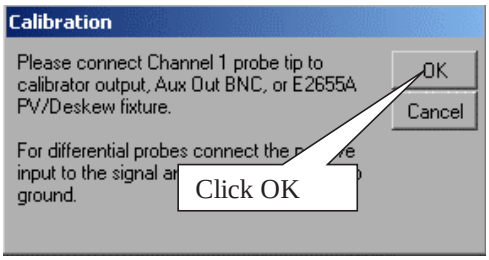

Figure 297 Calibration Window.

10 Referring to Figure 298 below, perform the following steps:

a Click OK to close the Probe Calibration Done window.

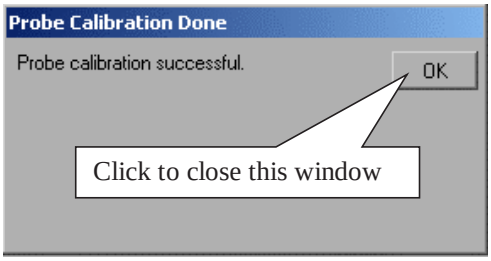

Figure 298 Calibration Window.

11 Referring to Figure 299 below, perform the following steps:

a Click the Close button to close this window.

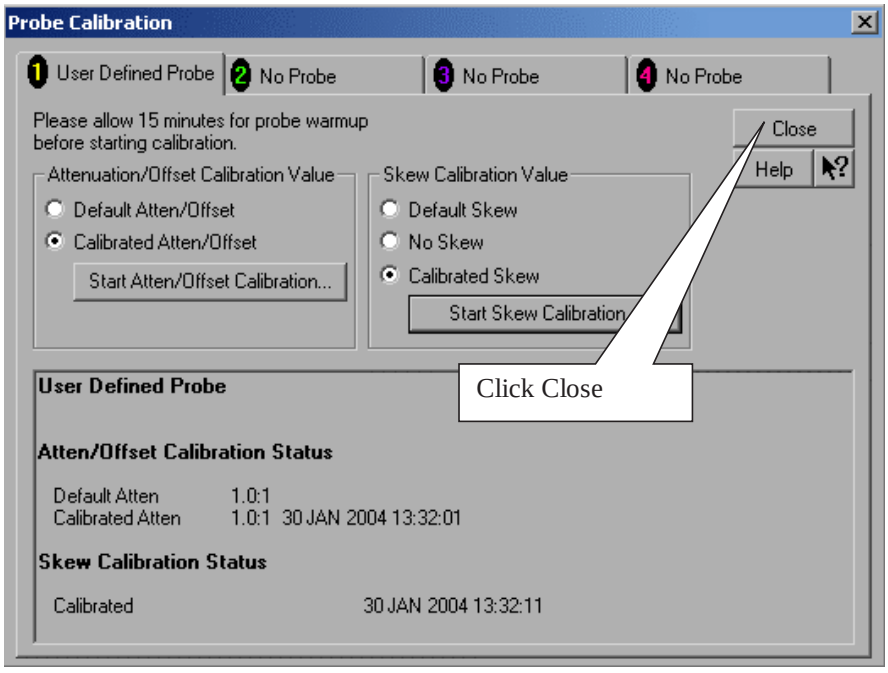

Figure 299 Calibration Window.

12 Referring to Figure 300 below, perform the following steps:

a Click on the Channel 3 tab.

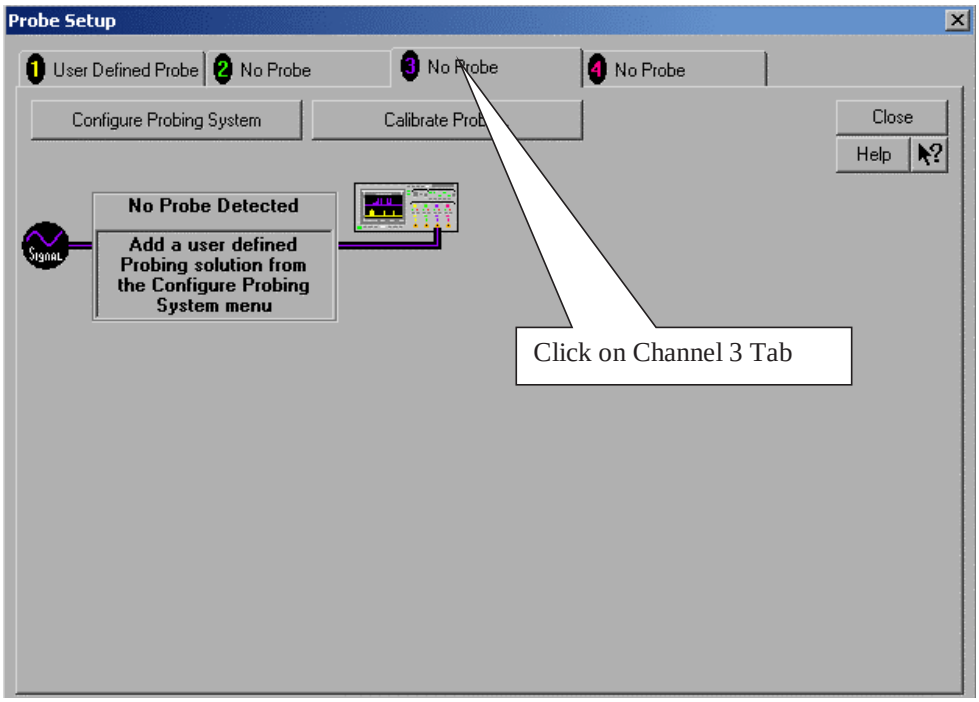

Figure 300 Calibration Window.

13 Referring to Figure 289 on page 617, perform the following steps:

a Disconnect the RG-316 cable connected to the SMA adapter on the Aux Out.

b Connect the other end of the RG-316 cable connected to the SMA adapter on Channel 3, to the SMA adapter on the Aux Out.

14 Repeat steps 3 through 11 of this section to calibrate the cable on Channel 3.

15 Click the Close button on the Probe Setup window (Figure 300) to close this window.

16 Click the Close button on the Channel Setup window (Figure 290 on page 618) to close this window.

17 The Cable and Probe calibration is complete.

18 Read the NOTE below.

NOTE Each cable is now calibrated for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the cables be labeled with the channel they were calibrated for.

Channel-to-Channel De-skew

This procedure ensures that the timing skew errors between channel 1 and channel 3 are minimized. Perform the following steps:

1 Referring to Figure 301 below, perform the following steps:

- **a** Do not disconnect the RG-316 cables from either the Channel 1 or Channel 3 SMA adapters.
- **b** If not already installed, install the non-Agilent SMA adapter on the oscilloscope Aux Out.
- **c** Disconnect any cable connected to the SMA adapter on the Aux Out.
- **d** Locate and connect the middle branch of the SMA Tee to the SMA adapter on the Aux Out BNC.
- **e** Connect the far end of the cable from the Channel 1 SMA adapter, to one branch of the SMA Tee on the Aux Out.
- **f** Connect the far end of the cable from the Channel 3 SMA adapter, to the other branch of the SMA Tee on the Aux Out.

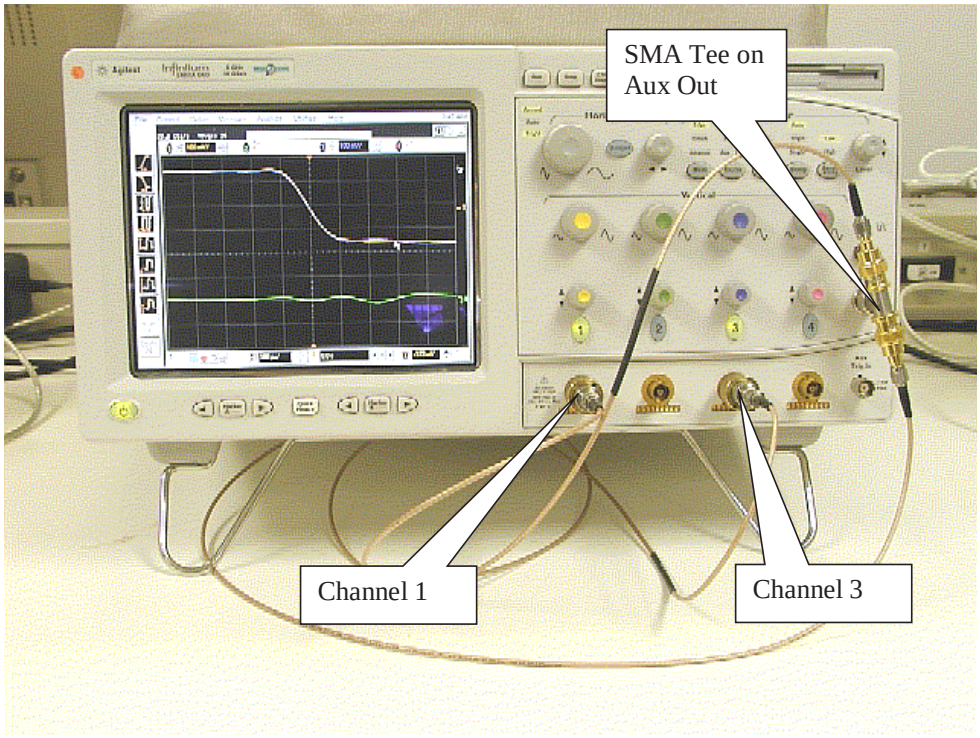

Figure 301 De-skew Connection.

2 Referring to Figure 302 below, perform the following steps:

- **a** Select the File>Load>Setup menu to open the Load Setup window.
- **b** Navigate to the directory location that contains the INF_SMA_Deskew.set setup file. If the setup file is not available, it can be created by following the instructions in Appendix C, “INF_SMA_Deskew.set Setup File Details”.
- **c** Select the INF_SMA_Deskew.set setup file by clicking on it.
- **d** Click the Load button to configure the oscilloscope from this setup file.

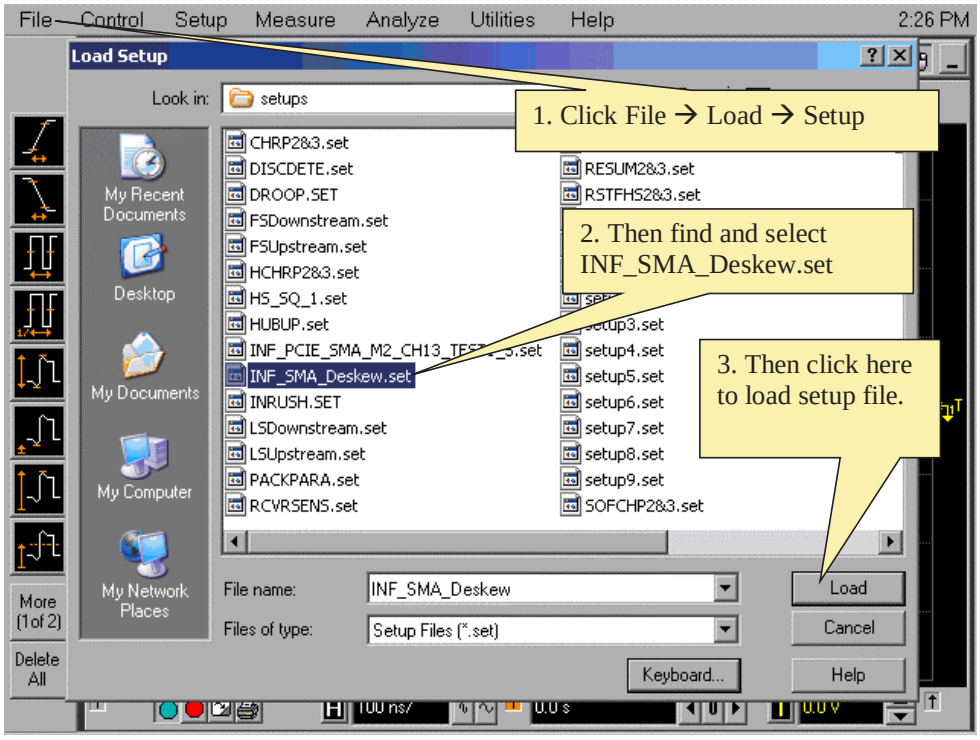

Figure 302 Load De-skew Setup.

The oscilloscope display should look similar to Figure 303 below. A falling edge of the square wave is shown in a 200 ps/div horizontal scale. The upper portion of the screen shows channel 1 (yellow trace) and channel 3 (purple trace) superimposed on one another. The lower portion of the screen is the differential signal (green trace) of channel 1 minus channel 3. The top two traces provide for visual inspection of relative time skew between the two channels. The bottom trace provides for visual presentation of unwanted differential mode signal resulted from relative channel skew (and to a much lesser extent from other inevitable channel mismatch parameters like gain and non-linearity). Figure 303 is an example of exaggerated skew between channel 1 and channel 3, measured to be about 50 ps with the cursor.

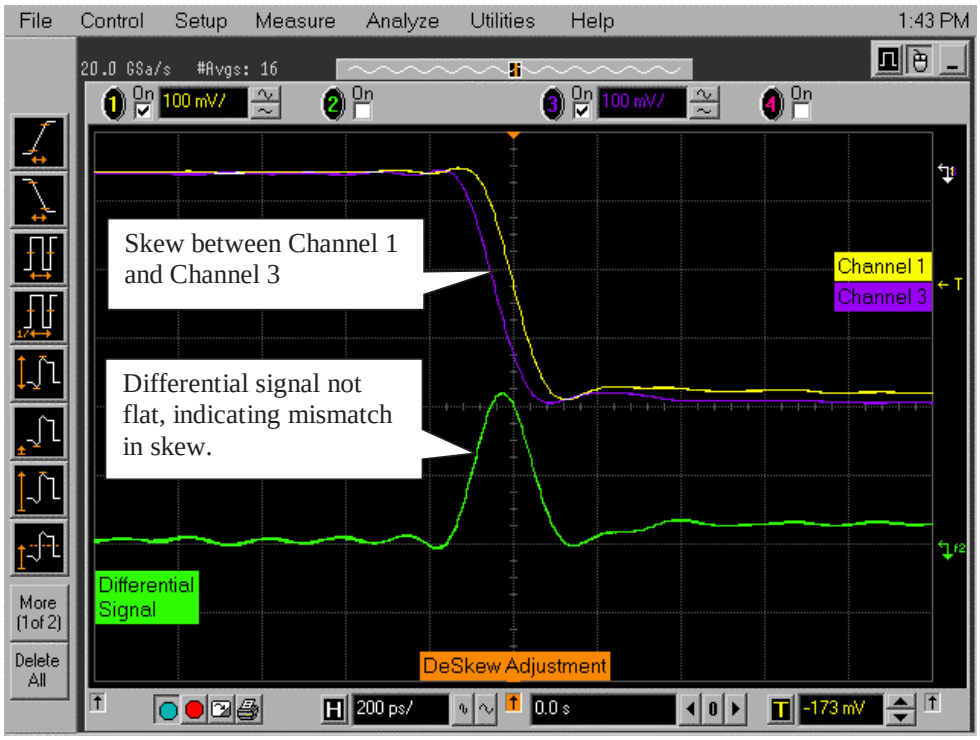

Figure 303 Channel Skew.

Figure 304 below shows the desired effect of no skew between the cables. Note that the channel 1 (yellow trace), channel 3 (purple trace) traces overlap, and the differential signal (green trace) is flat. If this is not the case, then perform the following steps to reduce the skew between channels 1 and 3.

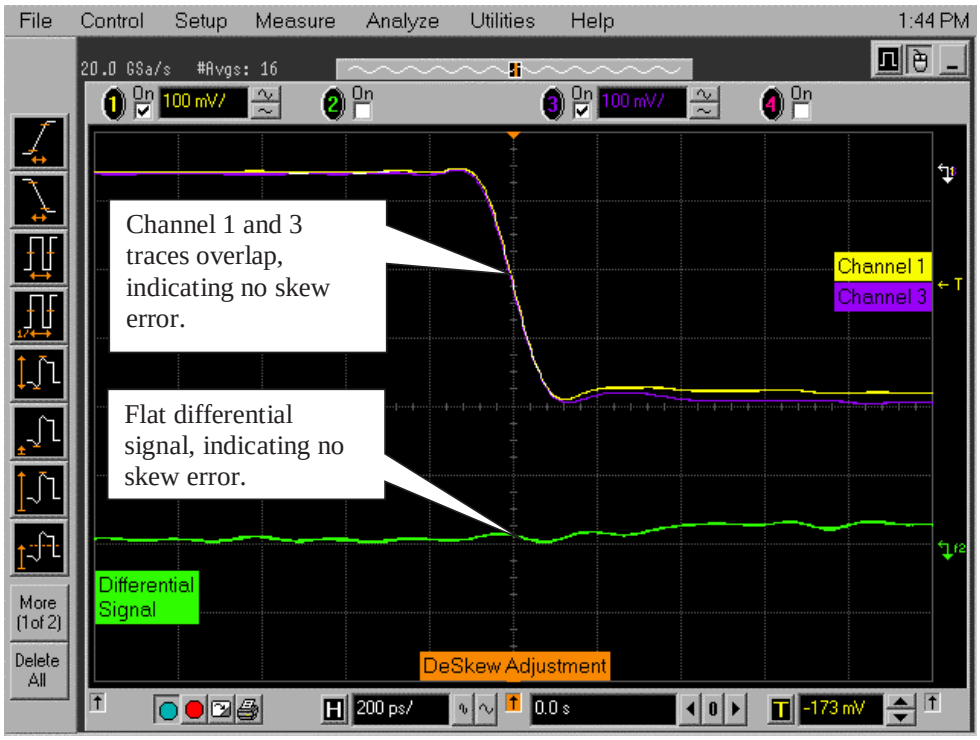

Figure 304 Skew Minimized.

3 Referring to Figure 305, perform the following steps to de-skew the channels:

- **a** Click on the Setup>Channel 1 menu to open the Channel Setup window.
- **b** Move the Channel Setup window to the left so you can see the traces.
- **c** Adjust the Skew by clicking on the < or > arrows, to achieve the flattest response on the differential signal (green trace).
- **d** Click the Close button on the Channel Setup window to close it.
- **e** The de-skew operation is complete.
- **f** Disconnect the cables from the Tee on the Aux Out BNC. Leave the cables connected to the Channel 1 and Channel 3 inputs.
- **g** Read the NOTE below.

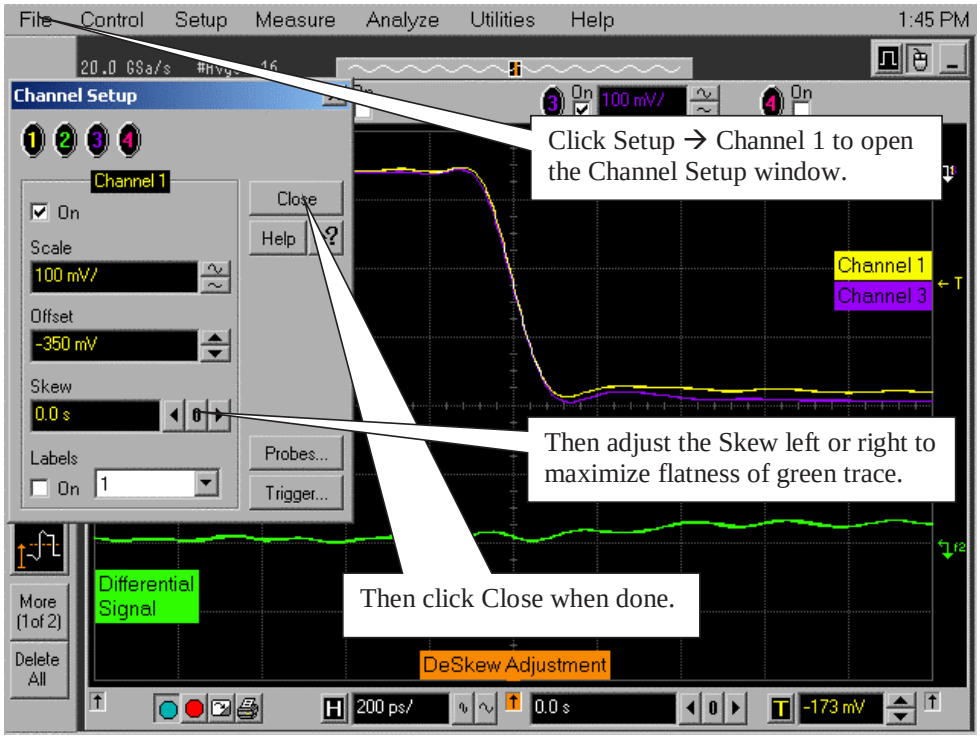

Figure 305 De-skewing Procedure.

NOTE

Each cable is now calibrated for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the cables be labeled with the channel they were calibrated for.

B
InfiniiMax Probing Options

Figure 306 1134A InfiniiMax Probe Amplifier

Figure 307 1134A Probe Amplifier and E2675A Differential Browser Probe Head

Agilent recommends 1169A or 1134A probe amplifiers. PCI Express 2.0 requires minimum of 1169A probe amplifiers. Agilent also recommends either the E2677A differential solder-in probe head or the E2675A differential browser probe head.

The differential solder-in probe head (E2677A) is recommended for highest signal fidelity while the differential browser probe head (E2675A) may be used for probing convenience.

Figure 308 Recommended Probe Heads for the PCI Express Testing

Table 195 Probe Head Characteristics

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential browser	E2675A	6 GHz, 0.32 pF, 50 kOhm	6 GHz, 0.57 pF, 25 kOhm
Differential solder-in	E2677A	7 GHz, 0.27 pF, 50 kOhm	7 GHz, 0.44 pF, 25 kOhm
Differential socket	E2678A	7 GHz, 0.34 pF, 50 kOhm	7 GHz, 0.56 pF, 25 kOhm

C
INF_SMA_Deskew.set Setup File Details

If the INF_SMA_Deskew.set file is not available, you can create it by following these instructions.

1 Start from a default setup by pressing the Default Setup key on the front panel. Then configure the following settings:

Acquisition	Averaging on number of averages 16 Interpolation on
Channel 1	Scale 100.0 mV/ Offset –350mV Coupling DC Impedance 50 Ohms
Channel 3	Turn Channel On; Scale 100.0 mV/ Offset –350m V Coupling DC Impedance 50 Ohms
Time base	Scale 200 ps/sec
Trigger	Trigger level –173mV Slope falling
Function 2	Turn on and configure for channel 1 subtract channel 3, Vertical scale 50 mV/ Offset 100.000 mV

C INF_SMA_Deskew.set Setup File Details

Index

S

T